



Solid State Devices, Inc.

14701 Firestone Blvd * La Mirada, Ca 90638
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SFF60N90E

60 AMP , 900 Volts, 0.22 Ω Avalanche Rated N-channel HiPower MOSFET

DESIGNER'S DATA SHEET

Part Number / Ordering Information ^{1/}

SFF 60 N 90 E

Screening ^{2/}
 — = Not Screened
 TX = TX Level
 TXV = TXV Level
 S = S Level

Package ^{3/ 4/}
 12 pin package

Voltage
 90 = 900V

Drain Current
 60 = 60A

Features:

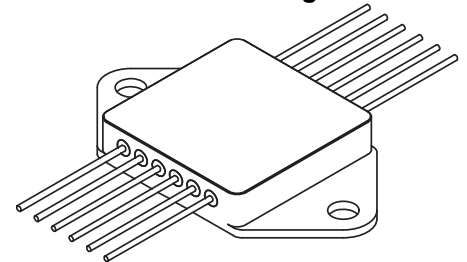
- Rugged poly-Si gate
- Lowest ON-resistance in the industry
- Avalanche rated
- Hermetically Sealed, Isolated Package
- Low Total Gate Charge
- Fast Switching
- TX, TXV, S-Level screening available
- Improved ($R_{DS(ON)}$) Q_G figure of merit

Maximum Ratings ^{5/}		Symbol	Value	Units
Drain - Source Voltage		V_{DSS}	900	V
Gate - Source Voltage	continuous transient	V_{GS}	± 20 ± 30	V
Max. Continuous Drain Current (package limited)	@ $T_C = 25^\circ C$	I_{D1}	60	A
Max. Instantaneous Drain Current (Tj limited)	@ $T_C = 25^\circ C$	I_{D2}	150	A
Max. Avalanche current	@ L= 0.1 mH	I_{AR}	60	A
Single and Repetitive Avalanche Energy	@ L= 0.1 mH	E_{AS} E_{AR}	4000 64	mJ
Total Power Dissipation	@ $T_C = 25^\circ C$	P_D	825	W
Operating & Storage Temperature		T_{OP} & T_{STG}	-55 to +150	$^\circ C$
Maximum Thermal Resistance (Junction to Case)		$R_{\theta JC}$	0.15	$^\circ C/W$

NOTES:

- *Pulse Test: Pulse Width = 300 μ sec, Duty Cycle = 2%.
- 1/ For ordering information, price, and availability – contact factory.
- 2/ Screening based on MIL-PRF-19500. Screening flows available on request.
- 3/ For lead bending options / pinout configurations – contact factory.
- 4/ Maximum current limited by package configuration
- 5/ Unless otherwise specified, all electrical characteristics @25 $^\circ C$.

12 Pin Package



NOTE: All specifications are subject to change without notification.
SCD's for these devices should be reviewed by SSDI prior to release.

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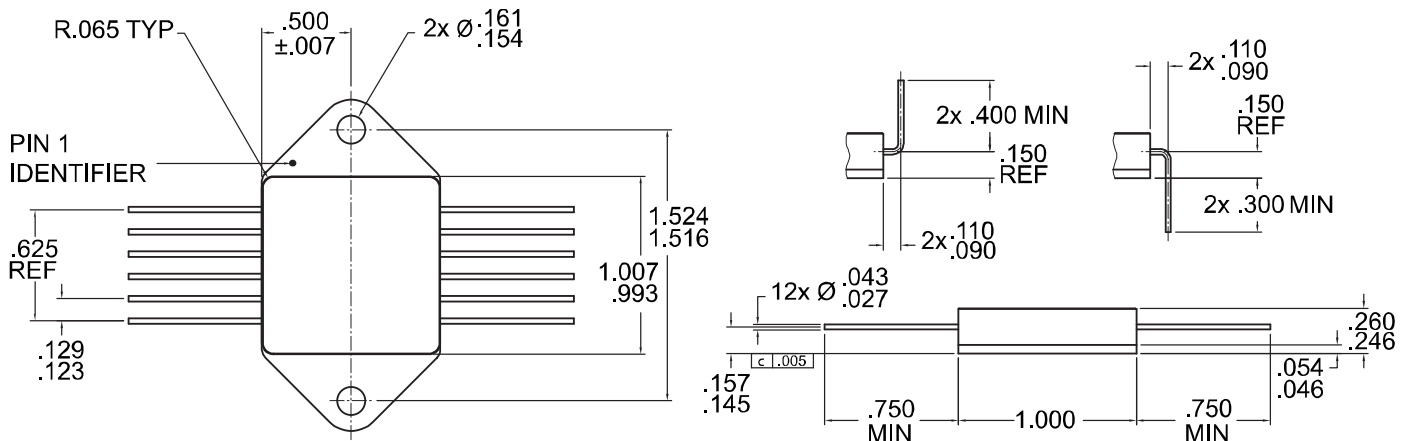
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SFF60N90E

Electrical Characteristics ^{5/}	Symbol	Min	Typ	Max	Units
Drain to Source Breakdown Voltage $V_{GS} = 0V, I_D = 1 \text{ mA}$	BV_{DSS}	900	960	—	V
Drain to Source On State Resistance $V_{GS} = 10V, I_D = 18A, T_j = 25^\circ C$ $V_{GS} = 10V, I_D = 55A, T_j = 25^\circ C$ $V_{GS} = 10V, I_D = 18A, T_j = 125^\circ C$	$R_{DS(on)}$	—	155	200	mΩ
		—	175	220	
		—	300	—	
Gate Threshold Voltage $V_{DS} = V_{GS}, I_D = 1.0mA, T_j = 25^\circ C$ $V_{DS} = V_{GS}, I_D = 1.0mA, T_j = 125^\circ C$ $V_{DS} = V_{GS}, I_D = 1.0mA, T_j = -55^\circ C$	$V_{GS(th)}$	2.5	5.0	6.0	V
		1.5	4.0	—	
		—	5.6	7.0	
Gate to Source Leakage $V_{GS} = \pm 20V, T_j = 25^\circ C$ $V_{GS} = \pm 20V, T_j = 125^\circ C$	I_{GSS}	—	10	±100	nA
		—	30	—	
Zero Gate Voltage Drain Current $V_{DS} = 720V, V_{GS} = 0V, T_j = 25^\circ C$ $V_{DS} = 900V, V_{GS} = 0V, T_j = 25^\circ C$ $V_{DS} = 720V, V_{GS} = 0V, T_j = 125^\circ C$	I_{DSS}	—	0.5	-	μA
		—	10	100	
		—	350	2000	
Forward Transconductance $V_{DS} = 15V, I_D = 20A, T_j = 25^\circ C$	g_{fs}	-	45	—	Mho
Total Gate Charge $V_{GS} = 10V$	Q_g	—	390	—	nC
Gate to Source Charge $V_{DS} = 500V$	Q_{GS}	—	135	—	
Gate to Drain Charge $I_D = 20A$	Q_{gd}	—	200	—	
Turn on Delay Time Rise Time Turn off Delay Time Fall Time $V_{GS} = 10V$ $V_{DS} = 450V$ $I_D = 10A$	$t_{d(on)}$	—	90	—	nsec
	t_r	—	80	—	
	$t_{d(off)}$	—	170	—	
	t_f	—	110	—	
Diode Forward Voltage $I_F = 60A, V_{GS} = 0V$	V_{SD}	—	0.80	1.2	V
Diode Reverse Recovery Time Reverse Recovery Charge $I_F = 36A, di/dt = 100A/\mu sec$	t_{rr1}	—	380	—	nsec
	I_{rm1}	—	9	—	A
	Q_{rr1}	—	2000	—	nC
Input Capacitance Output Capacitance Reverse Transfer Capacitance $V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1 \text{ MHz}$	C_{iss}	—	9.2	—	nF
	C_{oss}	—	1.4	—	nF
	C_{rss}	—	380	—	pF

CASE OUTLINE: 12 Pin Package



Gate: pins 1, 12
 Source: pins 2,3,4,9,10,11
 Drain: pins 5,6,7,8

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