AN2985
Application note

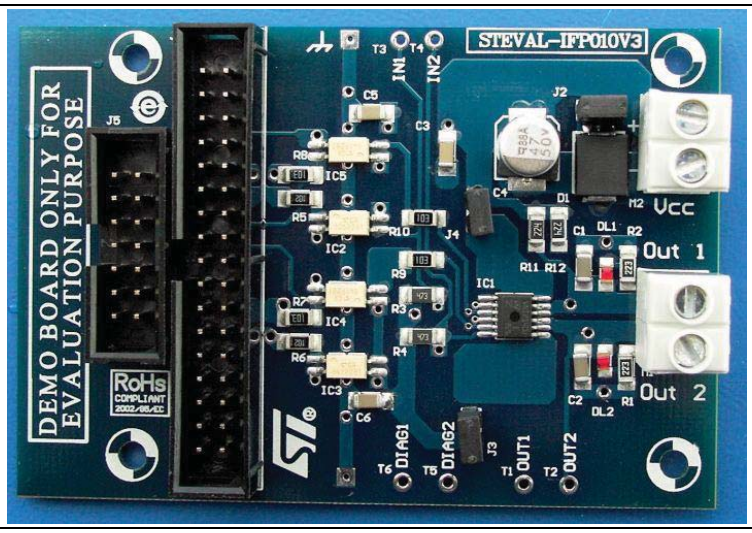
STEVAL-IFP010V3: designing with VNI2140J dual high-side smart power solid-state relay IC

Introduction

The STEVAL-IFP010V3 demonstration board has been developed to show the VNI2140J device functionalities within industrial applications such as PLCs (programmable logic controllers) which drive lamps, valves, relays, and similar loads.

This tool allows evaluating VNI2140J features, in particular embedded self-protection, power-handling capabilities, operation and diagnostic feedback, thermal behavior and conformity to EMC immunity standards.

Figure 1. STEVAL-IFP010V3



A double-sided PCB allows obtaining the best trade-off between a routing solution and thermal management results.

The main features of the demonstration board are:

- Two output channels (2 x 1 A)
- Two input channels
- Two feedback channels for fault and open load diagnostics
- Bidirectional opto-isolated interface for MCU safe connection
- TTL/CMOS compatible signals for MCU direct connection
- LEDs to indicate outputs
- Compliance to IEC61000-4-4 and IEC61000-4-5 standards
- Compatibility with existing STMicroelectronics tools (IBU communication board, CANIC10, for example) 10.5 V to 36 V DC power supply voltage range demonstration board description

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1 STEVAL-IFP010V3 demonstration board

1.1 Safety precautions

The board must be used only by expert technicians. The copper areas around the VNI2140J device have a heat sink function, visible in the top layer layout view, refer to *Figure 8*. In case of short-circuit, current limitation or hard demagnetization, the STEVAL-IFP010V3 board, or part of it, might reach a very high temperature with consequent danger.

No specific protections are implemented for a reverse DC accidental connection. Remember that an electrolytic capacitor is connected to the supply bus, therefore a reverse continuous DC voltage applied to it may produce a dangerous explosion.

Warning: ST assumes no responsibility for any consequences which may result from the improper use of this tool.

1.2 Description

The STEVAL-IFP010V3 demonstration board is composed of two main sections:

- An opto-isolated interface for input and status signals
- A two-channel self-protected power stage section with STMicroelectronics Transil™ diode protection.

The demonstration board consists of a double-sided FR4 printed circuit board with 35 µm copper plating. The PCB dimensions are 52 mm X 68 mm. The top and bottom view are shown in *Figure 3* and *4*, respectively.

1.3 VNI2140J - device overview

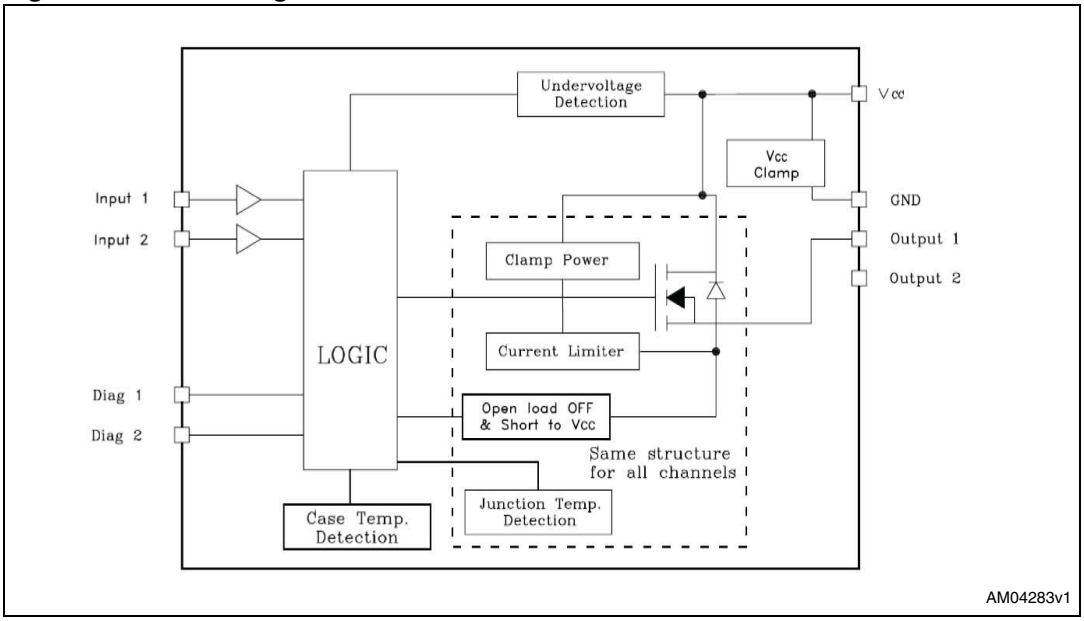
The VNI2140J is a monolithic two-channel driver featuring a very low supply current. The IC, which uses STMicroelectronics VIPower technology, is intended for driving loads with one side connected to ground. Active channel current limitation, combined with thermal shutdown (independent for each channel) and automatic restart, protect the device against overload.

The main features of the VNI2140J IC are:

- Output current: 1 A per channel
- Shorted load protections for each channel
- Junction overtemperature protection for thermal independence of the channels
- Case overtemperature protection and restart are not simultaneous for the two channels
- Protection against ground disconnection
- Current limitation
- Undervoltage shutdown

- Open load in off state and short to Vcc detection
- Open drain diagnostic outputs
- 3.3 V CMOS/TTL compatible inputs
- Fast demagnetization of inductive loads
- Conforms to IEC 61131-2

Figure 2. Block diagram



Active current limitation avoids that the system power supply drops in case of a shorted load. In overload condition, the channel turns off and back on automatically after the IC temperatures decreases below a threshold set by a temperature hysteresis so that junction temperature is controlled.

If this condition makes the case temperature reach the case temperature limit (T_{CSD}), overloaded channels are turned off (i.e. the channels for which junction temperature has exceeded the junction protection threshold, T_{jSD}, and has not fallen below the junction protection reset threshold, T_{jR}). These channels restart, non-simultaneously, only when the case temperature decreases below the case protection reset threshold (T_{CR}). Non-overloaded channels continue to operate normally.

The open drain diagnostic outputs indicate related channel overtemperature conditions.

1.4 Electrical characteristics

The electrical characteristics of the VNI2140J demonstration board (STEVAL-IFP010V3) are given in *Table 1*.

Table 1. STEVAL-IFP010V3 electrical characteristics

Parameter	Value			Comments
	Min	Typ	Max	
Operating condition				
Ambient operating temperature			85 °C	If the VNI2140J junction temperature exceeds 180 °C, the device shuts down
Power supply				
DC mains voltage range	10.5 V		36 V	
DC insulated voltage		5 V		From Eval communication board
Supply current on Vdd		300 µA		All channels are OFF
		1.9 mA	3.8 mA	All channels are ON, VIN = 5 V
Output stage				
Output channel (on) current limitation	1 A		2 A	Internally limited V_{CC} = 24 V; R_{LOAD} < 10 mΩ
dV/dt (on) Turn-on voltage slope		3 V/µs		I_{OUT} = 0.5 A, resistive load
dV/dt (off) Turn-off voltage slope		4 V/µs		I_{OUT} = 0.5 A, resistive load
Demagnetization protection				
Output voltage on inductive turn-off	V_{CC}-45	V_{CC}-50	V_{CC}-52	I_{OUT} = 0.5 A; L_{LOAD} >= 1 mH

1.5 Circuit description

The main components and functions of the module are indicated below:

- Power section
- L6562A controller
- FOT delay
- Current setting
- LEDs
- Dimming
- Auxiliary power
- Open / short-circuit protection

Figure 3. STEVAL-IFP010V3 top view

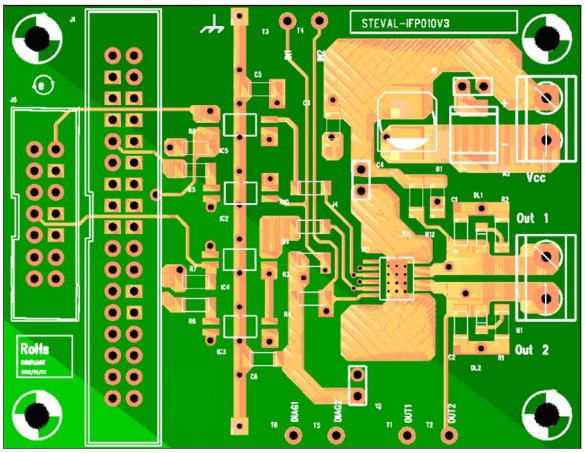
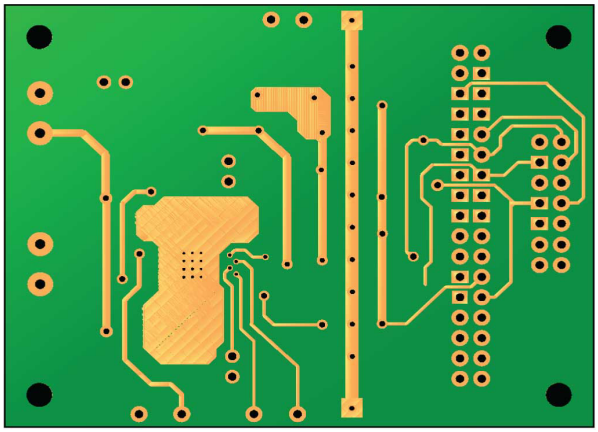
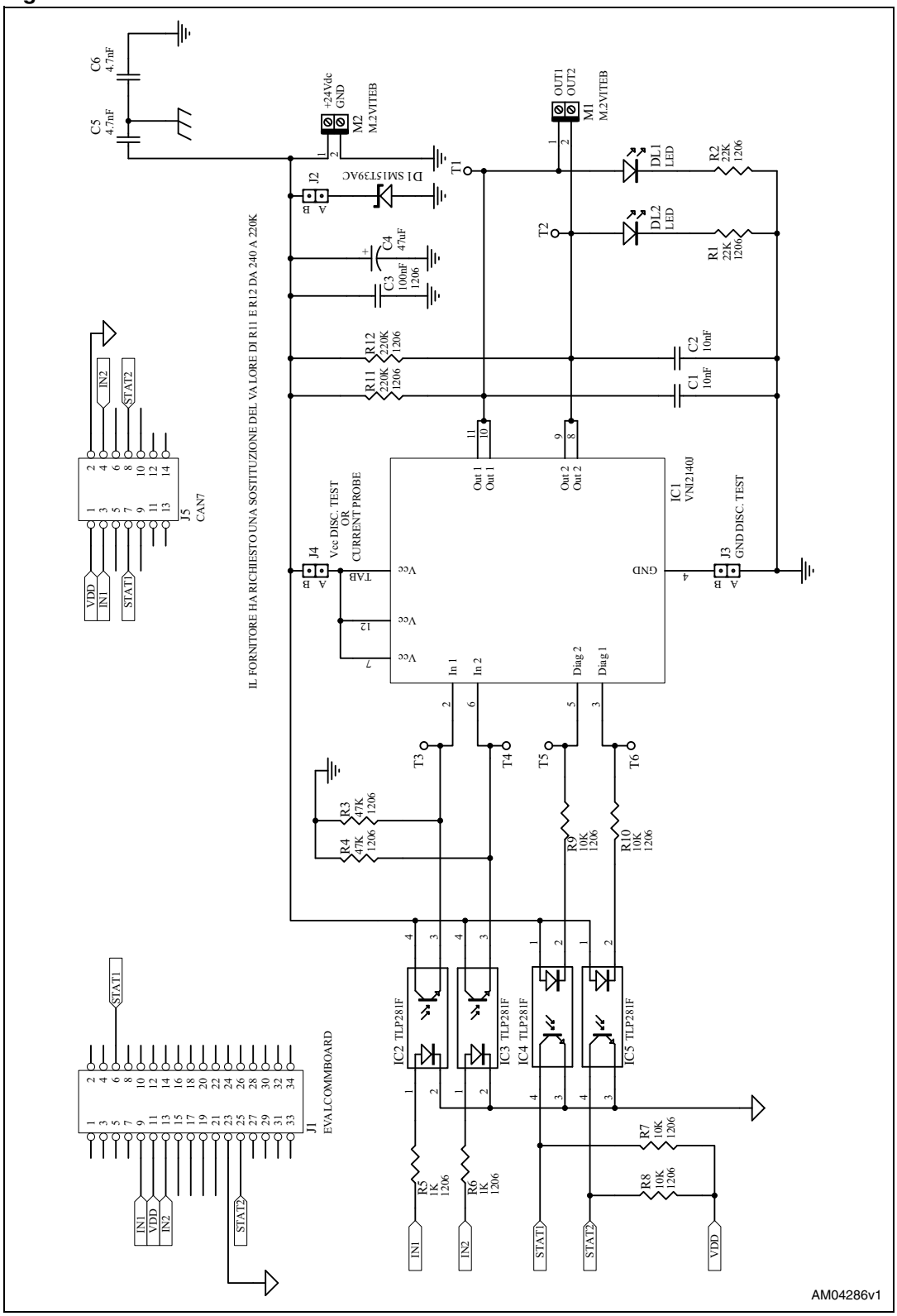


Figure 4. STEVAL-IFP010V3 bottom view



1.5.1 STEVAL-IFP010V3 electrical schematic

Figure 5. STEVAL-IFP010V3 schematic



1.5.2 STEVAL-IFP010V3 connectors

The demonstration board is equipped with input and output connectors. Specifically, there are two input header connectors (J5 and J1), one two-channel output channel connector (M1) and a supply voltage connector (M2).

Both input connectors, J5 and J1, provide the same bidirectional signals guaranteeing the maximum compatibility with existing STMicroelectronics tools such as the industrial communication board (see AN2451) and similar products.

Figure 6. J1 connector pinout

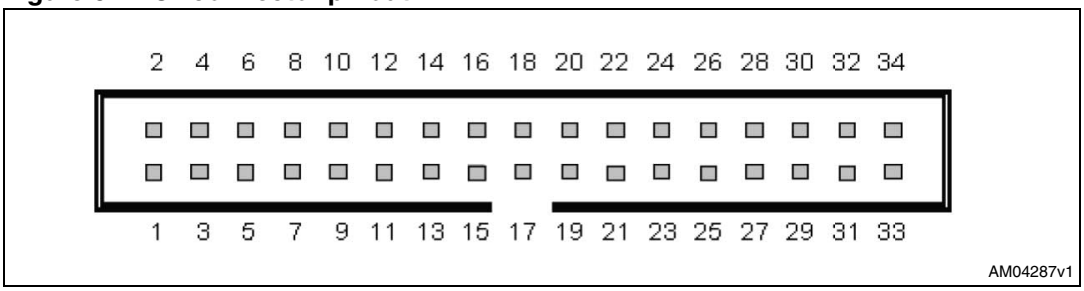


Figure 7. J5 connector pinout

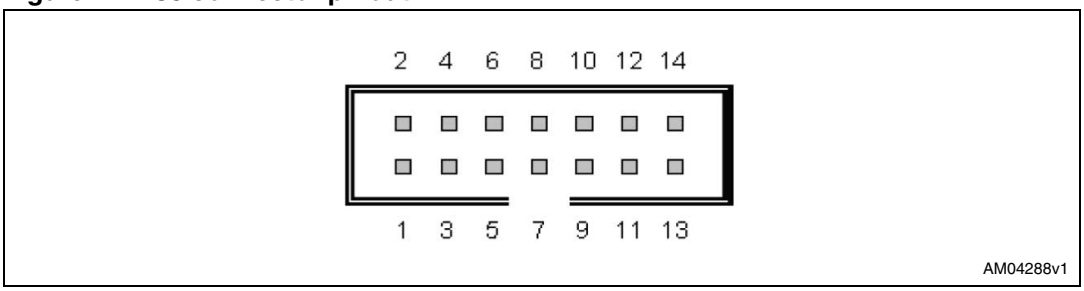


Table 2. J1 and J5 pin descriptions

J1 - pin number	J5 - pin number	Signal	Type
11	1	Vdd	5/3.3 V supply voltage
23	2	GND	Signal ground
9	3	IN1	Input channel 1
13	4	IN2	Input channel 2
6	7	STAT1	Status channel 1
25	8	STAT2	Status channel 2

1.5.3 STEVAL-IFP010V3 thermal management

The STEVAL-IFP010V3 PCB has two heatsinks: approximately 2 sq. cm on the top layer and 3 sq.cm on the bottom layer, thermally interconnected through 9 vias, as shown in *Figure 8*. In a steady-state condition low $R_{DS(on)}$ ensures a very low dissipation but, in current limitation and in fast demagnetization, the power dissipation is much higher, requiring a low thermal resistance through the device exposed tab, soldering space, top layer, vias and bottom layer path. A 25 µm copper (10 oz/sq. ft) thickness and 0.3 mm diameter for the vias are used according to EIA/JESd51-5.

Figure 8. STEVAL-IFP010V3 PCB copper heatsink

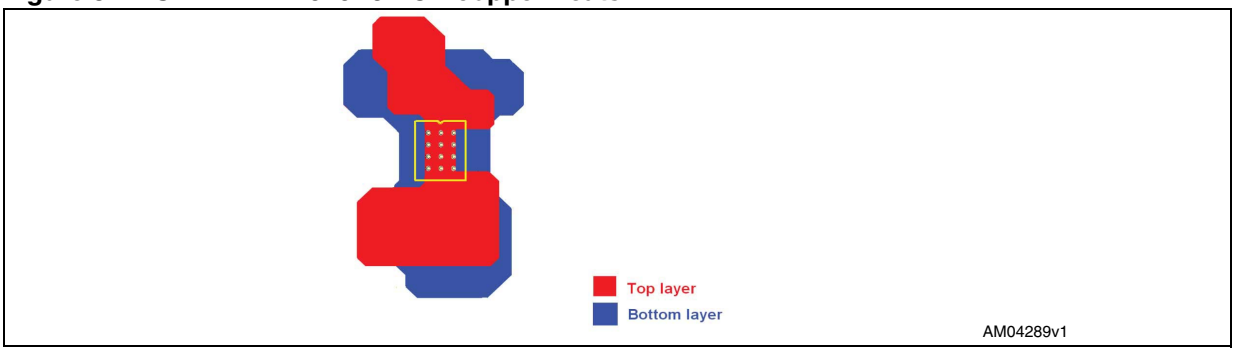


Figure 9 and *11* show the STEVAL-IFP010V3 temperature map with all channels permanently switched ON, 48 Ω loads, 24 V supply voltage and ambient temperature of 25 °C.

The IC temperature increase is only about a few degrees. *Figure 10* and *12* show a similar map when the IC is cycling at 1 Hz, 50% duty cycle, 48 Ω, 1.2 H loads, 24 V supply voltage and ambient temperature of 25 °C.

Figure 9. Thermal map in steady-state condition

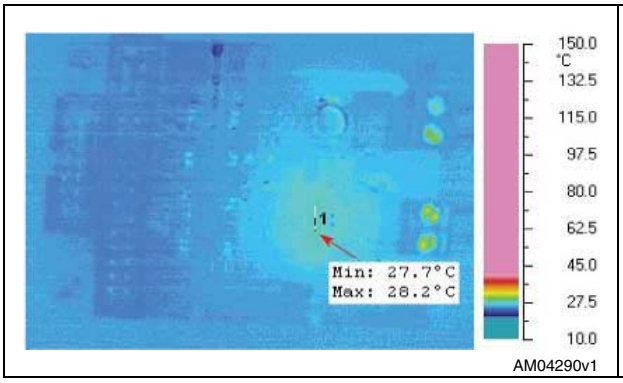


Figure 10. Thermal map in demagnetization condition (1 Hz repetitive cycling on 1.2 H 48 Ω load)

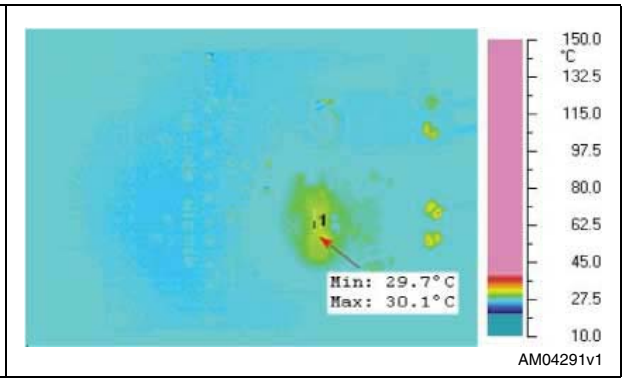


Figure 11. Steady-state thermal behavior, 3D simulation

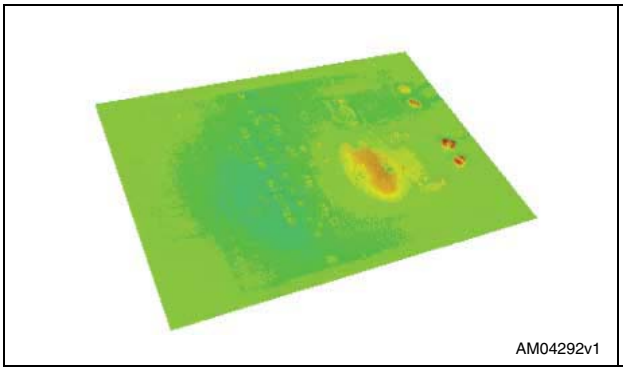
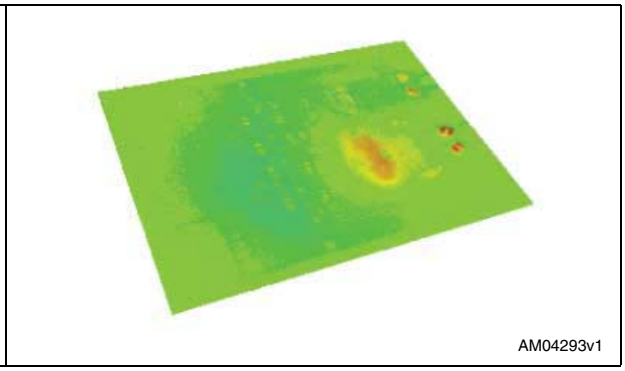


Figure 12. Repetitive demagnetization thermal behavior, 3D simulation (1 Hz repetitive cycling on 48 Ω 1.2 H load)



In particular *Figure 11* and *12* show a 3D thermal modelization of the device.

2 EMC immunity tests

The STEVAL-IFP010V3 has been tested according to EMC immunity standards IEC61000-4-4 (fast transient burst) and IEC61000-4-5 (high energy surge).

A fast transient burst test has been performed all channels.

Each channel under test cycles on and off at 1 Hz, duty cycle 50%, on two 48 Ω load resistors at 24 V_{DC} supply voltage.

A burst signal was applied using an ultra-compact simulator with an internal capacitive coupling clamp tool.

2.1 Test conditions

- Ambient temperature: 25.5 °C
- Ambient humidity: 46%
- Mains voltage power supply: 24 Vdc
- DC insulated voltage: 5 Vdc
- Loads: 4 x 48 Ω power resistor

2.2 Burst immunity test

Table 3 shows the burst setup configuration used to perform this test.

Table 3. Burst setup configuration

Test level	Condition
Pulse time **rt**	5 ns ± 30%
Pulse duration **td**	50 ns ± 30%
Source impedance	Zq = 50 Ω ± 20%
Polarity	Positive / negative
Burst duration (**td**)	15 ms ± 20 % at
Burst frequency (**f**)	5 kHz
Burst period (**tr**)	300 ms ± 20 %
Duration time (T)	5 min

Figure 13 shows the standard timing waveform applied during the burst test.

Figure 13. Burst timing waveform

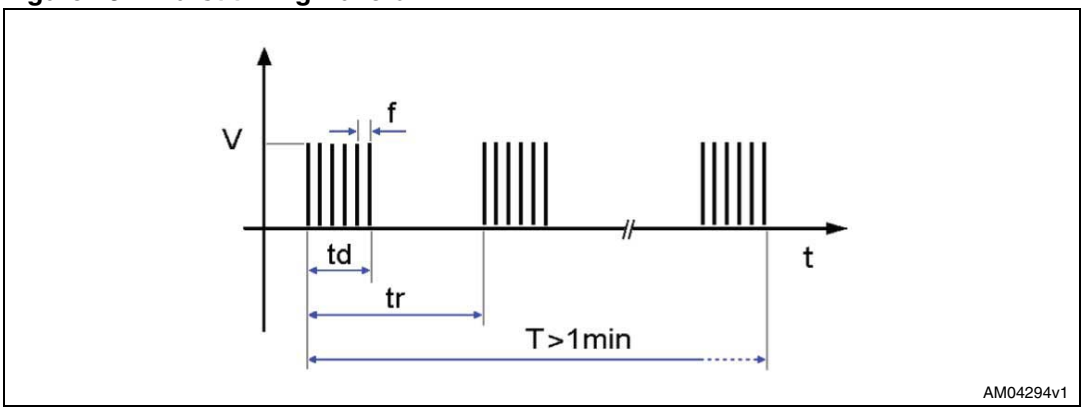


Table 4 shows the results of a burst test. Normal performance has been observed when applying two different disturbance levels on the output ports and Vcc main voltage power supply.

Table 4. Burst test results

Burst standard test routines	Level	Voltage level (kV)	Acceptance criteria(1)
IEC 61000-4-4	Level 1	0.5	A
IEC 61000-4-4	Level 2	1	A
IEC 61000-4-4	Level 3	2	A
IEC 61000-4-4	Level 4	4	A

1. Classification of the test:

(Criteria A): normal performance

(Criteria B): temporary degradation or loss of function or performance with automatic return to normal operation

(Criteria C): temporary degradation or loss of function with external intervention to recover normal operation

(Criteria D): degradation or loss of function, need replacement of damaged components to recover normal operation.

2.3 Surge test

A high energy surge test was performed in differential mode. A high surge signal was injected on the DUT (device under test) through a 42 Ω decoupling resistor. The test consisted of three positive and three negative discharges with a repetition rate of 1 discharge per minute.

Figure 14 shows the standard timing waveform applied on the DUT.

Figure 14. Surge standard timing waveform

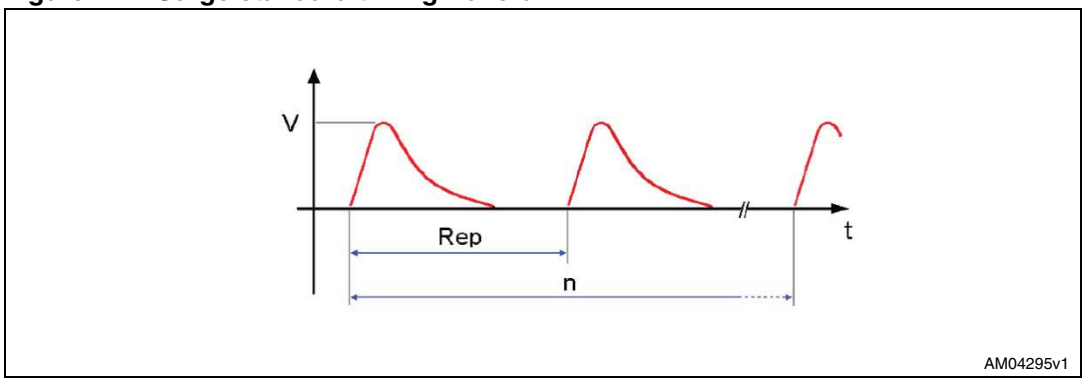


Table 5 below shows normal performance of the device.

Table 5. Surge test results

Surge standard test routines	Level	Voltage level (Kv)	Acceptance criteria(1)
IEC 61000-4-5	Level 1	0.5	A
IEC 61000-4-5	Level 2	1	A
IEC 61000-4-5	Level 3	2	A

1. Classification of the test:

(Criteria A): normal performance

(Criteria B): temporary degradation or loss of function or performance with automatic return to normal operation

(Criteria C): temporary degradation or loss of function with external intervention to recover normal operation

(Criteria D): degradation or loss of function, need substitution of damaged components to recover normal operation.

Appendix A STEVAL-IFP010V3 bill of material

Table 6. STEVAL-IFP010V3 bill of material

Designator	Part type	Description
C1	10 nF	Ceramic capacitor
C2	10 nF	Ceramic capacitor
C3	100 nF	Ceramic capacitor
C4	47 µF 50 V	Electrolytic capacitor
C5	4.7 nF	Ceramic capacitor
C6	4.7 nF	Ceramic capacitor
D1	SM15T39AC	ST Transil™ diode
DL1	LED	LED
DL2	LED	LED
IC1	VNI2140J	ST high-side driver IC
IC2	TLP281F	Opto-coupler
IC3	TLP281F	Opto-coupler
IC4	TLP281F	Opto-coupler
IC5	TLP281F	Opto-coupler
J1	Header 34-pin	EVAL communication board connector
J3	GND disc. test	Jumper
J4	Vcc disc. test	Jumper
J5	Header 34-pin	14.P PLUG
M1	2-way connector	screw drive connector
M2	2-way connector	screw drive connector
R1	22 kΩ	Resistor
R2	22 kΩ	Resistor
R3	47 kΩ	Resistor
R4	47 kΩ	Resistor
R5	1 kΩ	Resistor
R6	1 kΩ	Resistor
R7	10 kΩ	Resistor
R8	10 kΩ	Resistor
R9	10 kΩ	Resistor
R10	10 kΩ	Resistor
R11	220 kΩ	Resistor
R12	220 kΩ	Resistor

Appendix B STEVAL-IFP010V3 PCB layout

Figure 15. STEVAL-IFP010V3 component layer

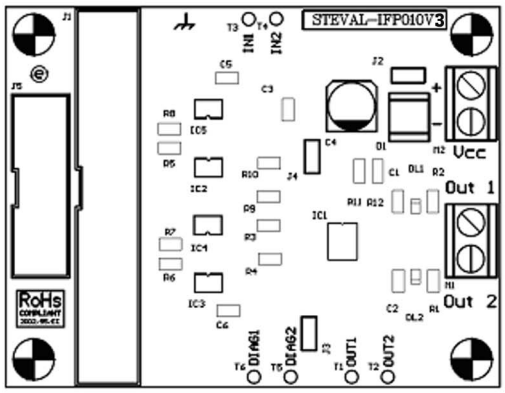


Figure 16. STEVAL-IFP010V3 copper top layer

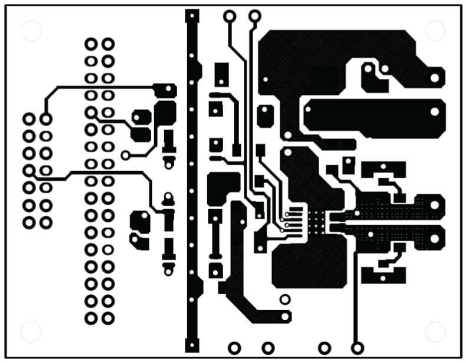
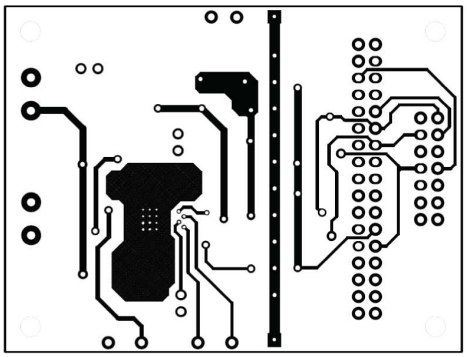


Figure 17. STEVAL-IFP010V3 copper bottom layer



Appendix C Reference documents

1. AN1351
2. AN2684

Revision history

Table 7. Document revision history

Date	Revision	Changes
17-Nov-2009	1	Initial release.
07-Nov-2012	2	Updated STEVAL-IFP010V2 with STEVAL-IFP010V3 and updated figure.

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