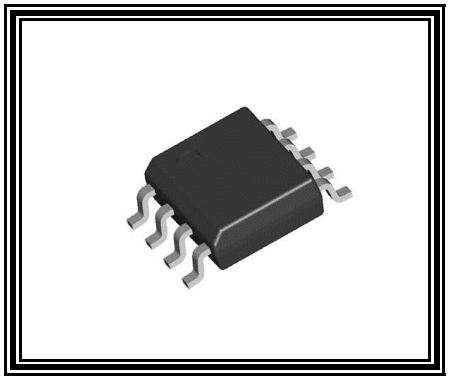
Features

- **Saifun NROM™ NVM Technology**
- **Operating voltage: 2.7V to 3.6V**
- **Clock frequency: 100/400/1700/3400 kHz**
- **Low power consumption**
  - **0.5µA standby current typical (L version)**
  - **<0.2µA standby current typical (LZ version)**
- **Write Modes**
  - **Byte Mode**
  - **Page Mode (128 Bytes/Page)**
- **Schmitt trigger inputs**
- **Hardware and software write protection for entire or partial array**
- **Endurance: up to 1 million data changes**
- **Data Retention: Greater than 40 years**
- **Packages: 8-Pin DIP, 8-Pin SOIC and MLF Leadless**
- **Temperature range**
  - **Commercial: 0°C to +70°C**
  - **Industrial (E): -40°C to +85°C**

SA24C512 Datasheet

512Kb EEPROM IIC



http://www.saifun.com

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Publication# **1907** Rev: **1** **Amendment: 1**
Issue Date: **10 September 2003**

General Description

SA24C512 is a 512-Kbit CMOS non-volatile serial EEPROM organized as 64K x 8 bit memory. This device conforms to Extended IIC 2-wire protocol that allows accessing of memory in excess of 16Kbit on an IIC bus. This serial communication protocol uses a Clock signal (SCL) and a Data signal (SDA) to synchronously clock data between a master (e.g. a microcontroller) and a slave (EEPROM).

SA24C512 offers hardware write protection whereby the entire memory array can be write protected by pulling WP pin to logic HIGH. The entire memory then becomes unalterable until the WP pin is switched to logic LOW. The device also features programmable write protect with options of full, half, or a quadrant of the array.

The “LZ” version of the SA24C512 offers very low standby current, making it suitable for low-power applications. SA24C512 is designed to minimize pin count and simplify PC board layout requirements. This device is offered in SO, DIP and Leadless MLF packages.

Saifun’s EEPROMs are designed and tested for applications requiring high endurance, high reliability and low power consumption.

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Block Diagram

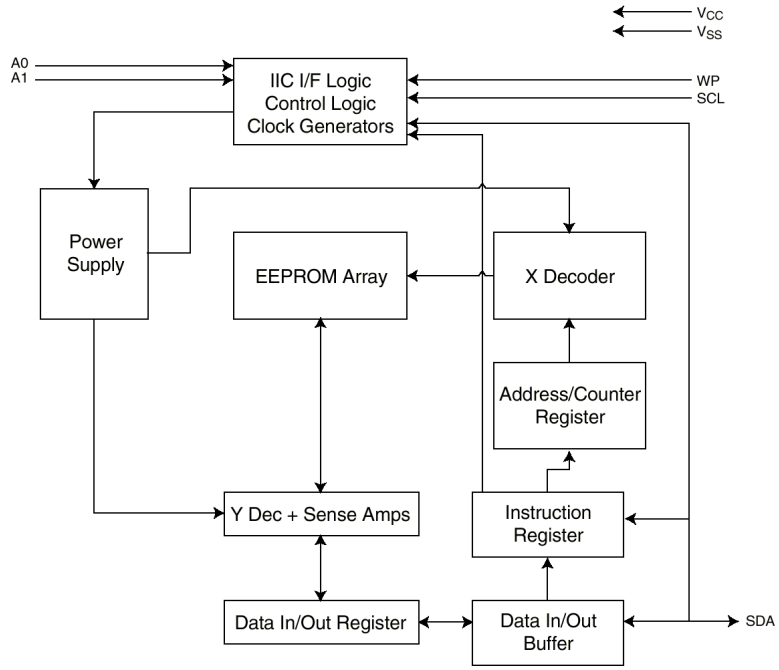


Figure 1. SA24C512 Block Diagram

Connection Diagram

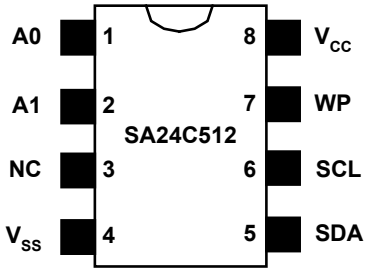


Figure 2. SO, Package (MW), Dual-in-Line Package (N), Top View

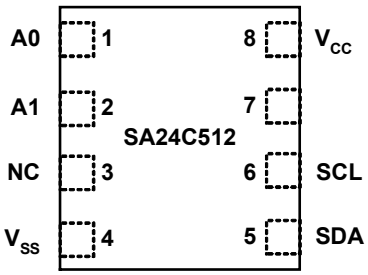


Figure 3. Leadless Package (MLF), Top View

Note:

For more details, see Package Number N08E and M08D.

Table 1. Pin Names

Pin Name	Signal Name	Description
A0	Device Select Address Input	Has an internal "weak" pull down so that when left unconnected assumes logic LOW.
A1	Device Select Address Input	Has an internal "weak" pull down so that when left unconnected assumes logic LOW.
NC	No Connect	
V_{SS}	Device Ground Input	
SDA	IIC Data Input/Output	Open Collector/Drain type
SCL	IIC Clock Input	
WP	Write Protect	Has an internal "weak" pull down so that when left unconnected assumes logic LOW. When LOW, Write is allowed to the memory array. When HIGH, Write is not allowed to the memory array as defined in *Write Protect (WP)*, page 14.
V_{CC}	Device Power Input	2.7 V to 3.6 V

Note:

No A2 pin (Pin 3) is provided. Treated as No Connect. Internal address comparison assumes this pin to be 0 and hence the command code should have corresponding bit set to 0.

Ordering Information

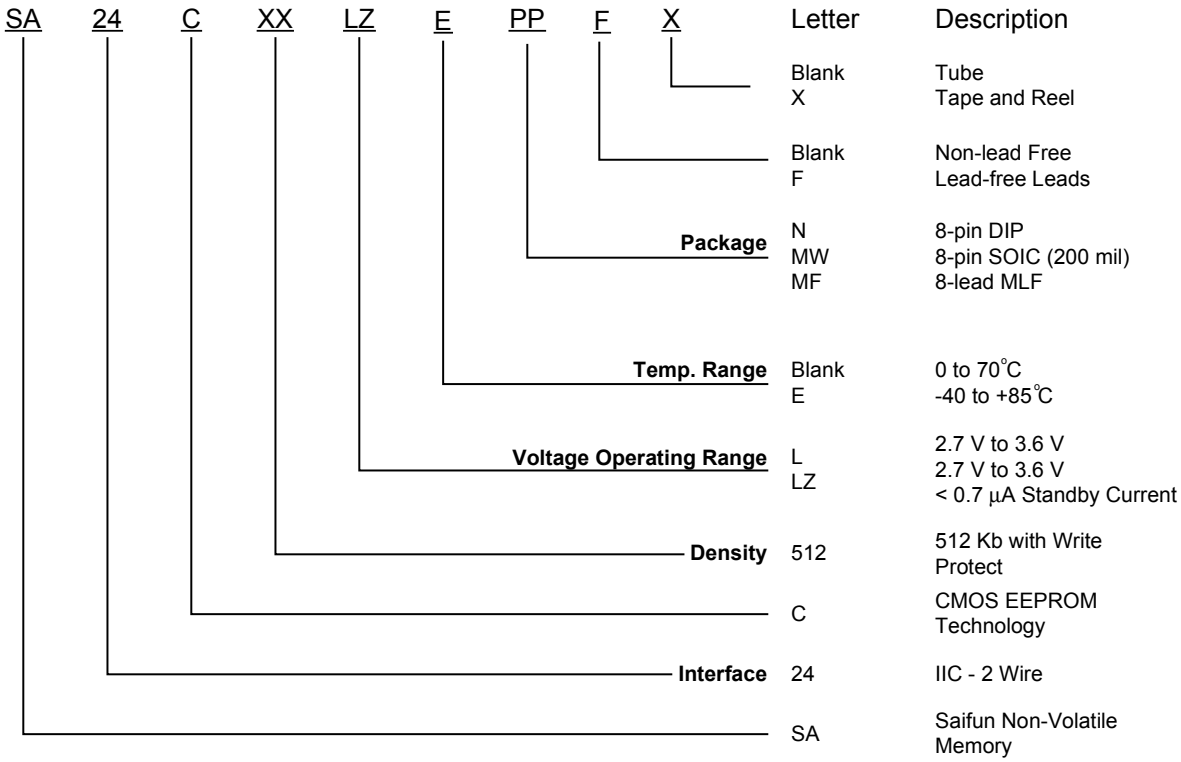


Figure 4. SA24C512 Ordering Information

Product Specifications

Absolute Maximum Ratings Operating Conditions

Ambient Storage Temperature	–65 °C to +150 °C
All Input or Output Voltages with Respect to Ground	4.5 V to -0.3 V
Lead Temperature	+300 °C
(Soldering, 10 seconds)	
ESD Rating	2000 V min.

ESD/Latchup Specification (JEDEC 8 Spec)

Human Body Model	Minimum 2 KV
Machine Model	Minimum 500 V
Latch up:	100 mA on all pins +125 °C

Operating Conditions

Ambient Operating Temperature	
SA24C512	0 °C to +70 °C
SA24C512E	-40 °C to +85 °C

DC Electrical Characteristics (VCC 2.7V to 3.6V)

Symbol	Parameter	Test Conditions	Limits			Units
			Min	Typ (Notes)	Max	
I_{CCA}	Active Power Supply Current	f_{SCL} = 100 kHz (Read)		2	3	mA
		f_{SCL} = 100 kHz (Write)		8	11	mA
		f_{SCL} = 400 KHZ (Read)		2	3	mA
		f_{SCL} = 400 kHz (Write)		8	11	mA
		f_{SCL} = 1.7 MHz (Read)		5	7	mA
		f_{SCL} = 1.7 MHz (Write)		8	11	mA
		f_{SCL} = 3.4 MHz (Read)		5	7	mA
		f_{SCL} = 3.4 MHz (Write)		8	11	mA
I_{SB}	Standby Current (L)	V_{IN} = GND or V_{CC}		0.5	1	µA
	Standby Current (LZ)	V_{IN} = GND or V_{CC}		0.2	0.7	µA
I_{IL}	Input Leakage Current	V_{IN} = GND to V_{CC}		0.1	1	µA
I_{OL}	Output Leakage Current	V_{OUT} = GND to V_{CC}		0.1	1	µA
V_{IL}	Input Low Voltage		-0.3		V_{CC} x 0.3	V
V_{IH}	Input High Voltage		V_{CC} x 0.7		V_{CC} + 0.5	V
V_{OL}	Output Low Voltage	I_{OL} = 3 mA			0.4	V

Notes

(1) Typical values are TA = 25 °C and nominal supply voltage of 3 volts.

(2) Write frequency is 50 Hz.

Capacitance

T_A = +25°C, f = 100/400 kHz/1.7 MHz/3.4 MHz, V_{CC} = 3V (Note 2)

Symbol	Test	Conditions	Max	Units
$C_{I/O}$	Input/Output Capacitance (SDA)	$V_{I/O}$ = 0V	8	pF
C_{IN}	Input Capacitance (A0, A1, A2, SCL)	V_{IN} = 0V	6	pF

Notes:

(1) This parameter is periodically sampled and not 100% tested.

(2) Typical values are T_A = 25°C and nominal supply voltage of 3 volts.

AC Test Conditions

Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input Rise and Fall Times	10 ns
Input & Output Timing Levels	V_{CC} x 0.3 to V_{CC} x 0.7
Output Load	1 TTL Gate and C_L = 100 pF

AC Testing Input/Output Waveforms

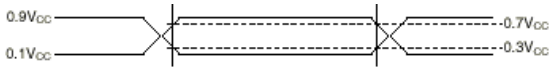


Figure 5. AC Testing Input/Output Waveforms

AC Characteristics (V_{CC} 2.7V to 3.6V)

Symbol	Parameter	100 kHz		400 kHz		1.7 MHz		3.4 MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f_{SCL}	SCL Clock Frequency		100		400		1700		3400	kHz
t_{LOW}	Clock Low Period	4700		1300		320		160		ns
t_{HIGH}	Clock High Period	4000		600		120		60		ns
$t_{SU:STA}$	START Condition Setup Time (for a Repeated START Condition)	4700		600		160		160		ns
$t_{HD:STA}$	START Condition Hold Time (for a Repeated START Condition)	4000		600		160		160		ns
$t_{SU:STO}$	STOP Condition Setup Time	4000		600		160		160		ns
t_{RDA}	SDA Rise Time (depend on external pull-up)		1000		300	20	170	10	85	ns
t_{FDA}	SDA Fall Time		300		300	20	170	10	85	ns
t_{RCL}	SCL Rise Time (depend on external pull-up)		1000		300	20	80	10	40	ns
t_{FCL}	SCL Fall Time		300		300	20	80	10	40	ns
t_{RCL1}	SCL Rise Time after repeated START or after ACK bit		NA	NA	NA	20	160	10	80	ns
$t_{SU:DAT}$	Data in Setup Time	250		100		20		20		ns
$t_{HD:DAT}$	Data in Hold Time	0		0		0		0		ns
t_{DH}	Data Out Hold Time	300		100		0		0		ns

Symbol	Parameter	100 kHz		400 kHz		1.7 MHz		3.4 MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
T_I	Noise Suppression Time Constant at SCL, SDA Inputs (Minimum V_{IN} Pulse width)		50		50		10		10	ns
t_{AA}	SCL Low to SDA Data Out Valid	300[1]	3500	100[1]	900	0	170	0	85	ns
t_{BUF}	Time the Bus Must Be Free Before a New Transmission Can Start	4700		1300		320		160		ns
t_{WR}	Write Cycle Time		10		10		10		10	ms
	Endurance	1 million[2]								Cycles

[1] The minimum value is defined to bridge the undefined part between V_{IH} and V_{IL} of the falling edge of SCL. The standard number is 0 ns.

[2] This parameter is not tested but ensured by characterization.

Bus Timing

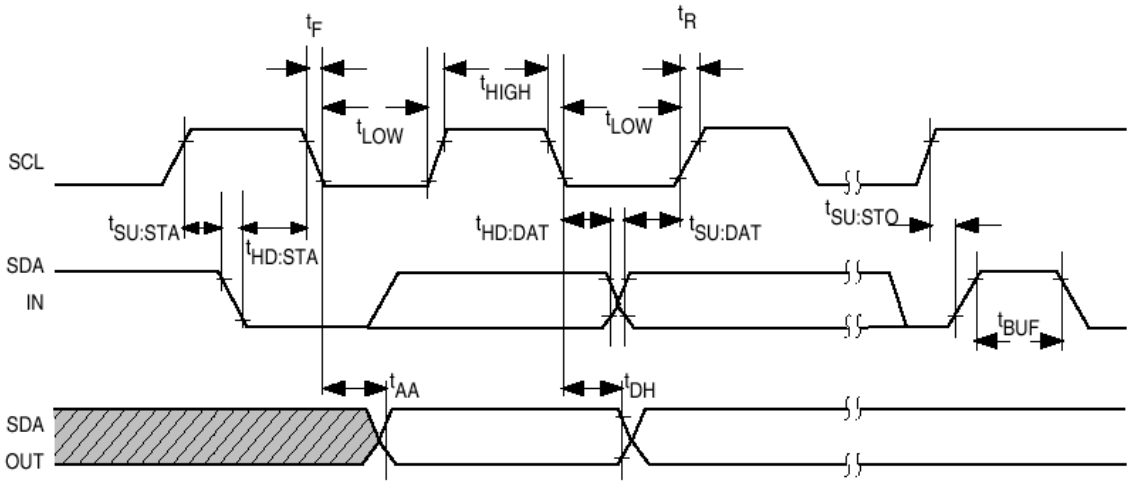


Figure 6. Bus Timing

Write Cycle Timing

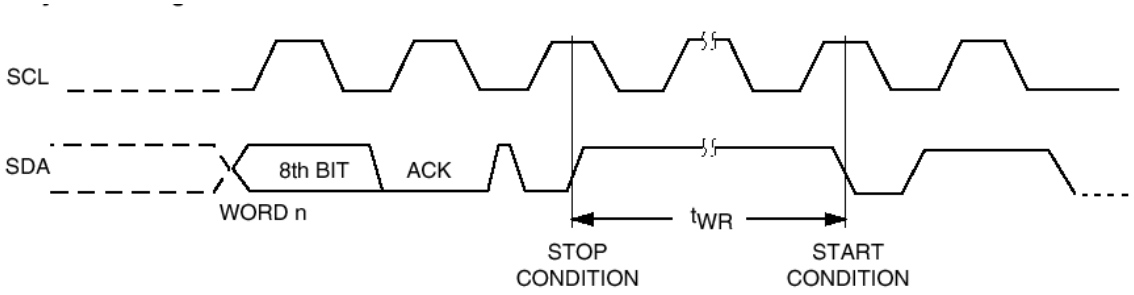


Figure 7. Write Cycle Timing

Note:

The Write cycle time (t_{WR}) is the time from a valid STOP condition of a Write sequence to the end of the internal erase/program cycle.

Typical System Configuration

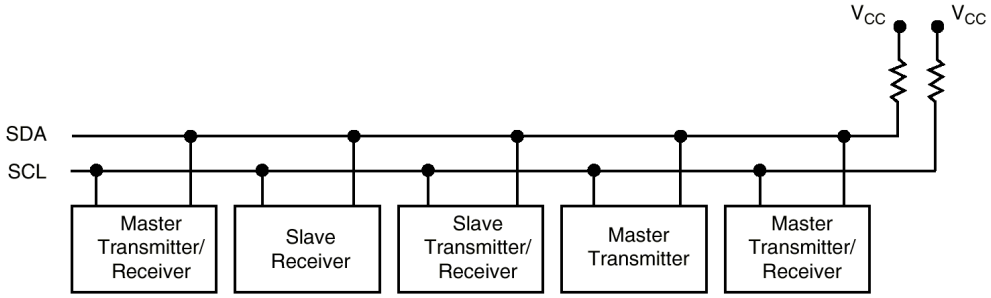


Figure 8. Typical System Configuration

Note:

Due to the open-drain configuration of SDA and SCL, a bus-level pull-up resistor is called for, (typical value = 4.7kΩ).

Background Information (IIC Bus)

Extended IIC specification is an extension of the Standard IIC specification, which enables addressing of EEPROMs with more than 15 Kbits of memory on an IIC bus. The difference between the two specifications is that the Extended IIC specification defines two bytes of "Array Address" information, while the Standard IIC specification defines only one. All other aspects are identical between the two specifications. Using two bytes of Array Address and two address signals (A1 and A0), it is now possible to address up to 4 Mbits ($2^8 \cdot 2^8 \cdot 2^2 \cdot 8 = 2$ Mbits) of memory on an IIC bus.

Note that due to format difference, it is not possible to have both peripherals that follow the Standard IIC specification (e.g., 16-Kbit EEPROM) and peripherals that follow the Extended IIC specification (e.g., 512-Kbit EEPROM) on a common IIC bus.

The IIC bus allows synchronous bidirectional communication between a transmitter and a receiver using a Clock signal (SCL) and a Data signal (SDA). Additionally, there are two Address signals (A1 and A0) that collectively serve as a "chip select signal" to a device (e.g., EEPROM) on the bus.

All communication on the IIC bus must be started with a valid START condition by a master, followed by transmittal by the master of byte(s) of information (Address/Data). For every byte of information received, the addressed receiver provides a valid Acknowledge pulse to further continue the communication unless the receiver intends to discontinue the communication. Depending on the direction of transfer (Write or Read), the receiver can be either a slave or the master. A typical IIC communication concludes with a STOP condition (by the master).

Addressing an EEPROM memory location involves sending a command string with the following information:

[DEVICE TYPE]—[DEVICE/PAGE BLOCK SELECTION]—[R/W BIT]—[ARRAY ADDRESS#1]—[ARRAY ADDRESS#0]

Slave Address

The slave address is an 8-bit information consisting of a Device type field (4 bits), Device/Page block selection field (3 bits) and Read/Write bit (1 bit).

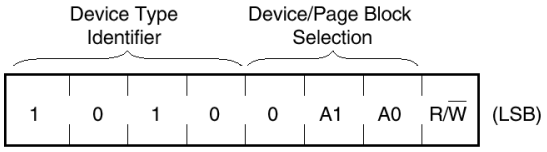


Figure 9 Slave Address

Device Type

The IIC bus is designed to support a variety of devices, such as RAMs, EPROMs, and so on., along with EEPROMS. To properly identify various devices on the IIC bus, a 4-bit “Device Type” identifier string is used. For EEPROMS, this 4-bit string is 1-0-1-0. Every IIC device on the bus internally compares this 4-bit string to its own “Device Type” string to ensure proper device selection.

Device/Page Block Selection

When multiple devices of the same type (e.g., multiple EEPROMS) are present on the IIC bus, the A1 and A0 address information bits are used in device selection. Every IIC device on the bus internally compares this 3-bit string to its own physical configuration (A1 and A0 pins) to ensure proper device selection. This comparison is in addition to the “Device Type” comparison.

In addition to selecting an EEPROM, these 3 bits are also used to select a “page block” within the selected EEPROM. Each page block is 512 Kbits (64 KBytes) in size. If an EEPROM contains more than one page block, the selection of a page block within the EEPROM is by using A1 and A0 bits.

Read/Write Bit

Last bit of the slave address indicates if the intended access is Read or Write. If the bit is 1, the access is Read; if it is 0, the access is Write.

Acknowledge

Acknowledge is an active LOW pulse on the SDA line driven by an addressed receiver to the addressing transmitter to indicate receipt of 8 bits of data. The receiver provides an ACK pulse for every 8 bits of data received. This handshake mechanism is done as follows: After transmitting 8 bits of data, the transmitter releases the SDA line and waits for the ACK pulse. The addressed receiver, if present, drives the ACK pulse on the SDA line during the ninth clock and releases the SDA line back (to the transmitter). Refer to Figure 14.

Array Address#1

This is an 8-bit information containing the most significant 8 bits of the 16-bit memory array address of a location to be selected within a page block of the device.

Array Address#0

This is an 8-bit information containing the least significant 8-bits of 16-bit memory array address of a location to be selected within a page block of the device.

Pin Descriptions

Serial Clock (SCL)

The SCL input is used to clock all data into and out of the device.

Serial Data (SDA)

SDA is a bidirectional pin used to transfer data into and out of the device. It is an open drain output and may be wire–ORed with any number of open drain or open collector outputs.

Write Protect (WP)

Choice 1: Full Array Write Protect

If pulled HIGH, Write operations will not be executed. READ operations are possible. If pulled LOW, normal operation is enabled, READ/WRITE over the entire memory is possible.

This feature allows the user to assign the entire memory as ROM, which can be protected against accidental programming. When Write is disabled, the slave address and word address will be acknowledged but data will not be acknowledged.

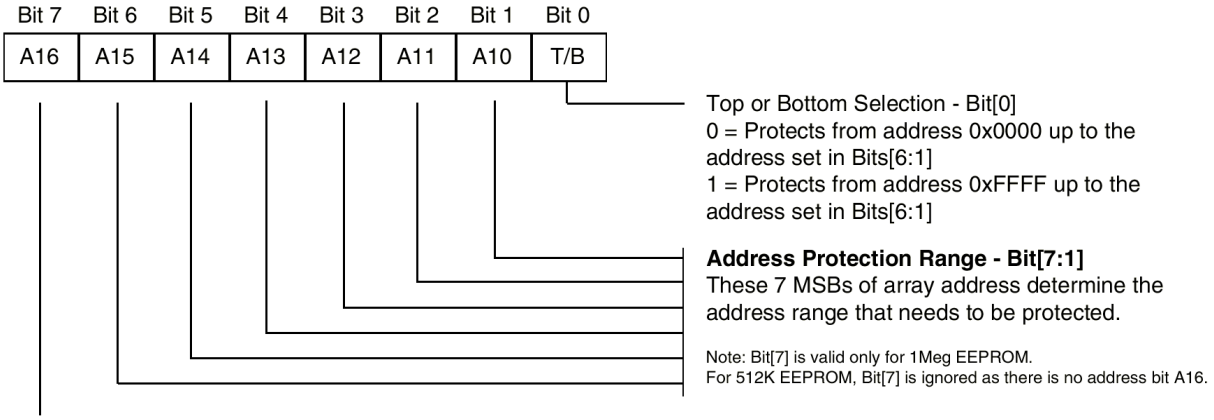
This pin has an internal pull-down circuit. However, on systems where write protection is not required it is recommended that this pin be tied to V_{SS}.

Write Protection Truth Table

WP Pin	"Less Than" Comparison	T/B Bit	Write Allowed
1	YES	0	NO
1	NO	0	YES
1	YES	1	YES
1	NO	1	NO
0	Don't Care	Don't Care	YES

Choice 2: Programmable Write Protect[1]

The Programmable Write protection is available to customers by contacting a Sales Representative. An internal 8-bit wide internal NV-latch is used, with the following definition:



[1] Predefined on Sort. Not a user command.

Example (512K)	Write Protection Area	NV-Latch Bit Setting - Bits [7:0]	Result
1	Full Array (0x0000 - 0xFFFF)	X-0-0-0-0-0-0-1	Address bits (A15:A10) issued during the Write command are compared against bits[6:0] of this NV-Latch. Since bit[0] of this NV-Latch is set to 1, Write is not allowed as long as the comparison results in "greater than or equal to" status.
2	Bottom Half (0x0000 - 0x7FFF)	X-1-0-0-0-0-0-0	Same as example 1.
3	Bottom Quadrant (0x0000 - 0x3FFF)	X-0-1-0-0-0-0-0	Same as example 1.
4	Top Quadrant (0xFFF - oxC000)	X-1-1-0-0-0-0-1	Address bits (A15:A10) issued during the Write command are compared against bits[6:0] of this NV-Latch. Since bit[0] of this NV-Latch is set to 1, Write is allowed as long as the comparison results in "greater than or equal to" status.
5	Top Half (0xFFF - 0x8000)	X-1-0-0-0-0-0-1	Same as example 4.
6	No Write Protection	X-0-0-0-0-0-0-0	Same as example 4.

Device Selection Inputs A1 and A0 (as Appropriate)

These inputs collectively serve as a “chip select” signal to an EEPROM when multiple EEPROMs are present on the same IIC bus. Hence these inputs, if present, should be connected to either V_{CC} or V_{SS} in a unique manner to enable proper selection of an EEPROM among multiple EEPROMs. During a typical addressing sequence, every EEPROM on the IIC bus compares the configuration of these inputs to the respective 3-bit “Device/Page block selection” information (part of the slave address) to determine a valid selection. For example, if the 3-bit “Device/Page block selection” is 1-0-1, the EEPROM whose “Device Selection inputs” (A1 and A0) are connected to V_{CC}-V_{SS}-V_{CC}, respectively, is selected.

Only A1 and A0 are provided on the SA24C512, which means that the corresponding A2 bit in the "Device/Page block selection" should be set to 0 during all access to the device. These two pins have a weak internal pull-down circuit.

Device Operation

The SA24C512 supports a bidirectional bus-oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device that is controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the SA24C512 will be considered a slave in all applications.

Clock and Data Conventions

Data states on the SDA line can change only during SCL LOW. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions. Refer to Figure 12.

START Condition

All commands are preceded by the START condition, which is a HIGH-to-LOW transition of SDA when SCL is HIGH. The SA24C512 continuously monitors the SDA and SCL lines for the START condition and will not respond to any command until this condition has been met. Refer to Figure 13.

STOP Condition

All communications are terminated by a STOP condition, which is a LOW-to-HIGH transition of SDA when SCL is HIGH. The STOP condition is also used by the SA24C512 to place the device in the standby power mode. Refer to Figure 13.

SA24C512 Array Addressing

During Read/Write operations, addressing the EEPROM memory array involves in providing two address bytes, "Word Address 1" and "Word Address 0." The "Word Address 1" byte contains the eight most significant bits of the array address, while "Word Address 0" byte contains the eight least significant bits of the array address.

Switching from F/S to HS Mode and Back

After reset and initialization, the device must be in Fast mode. The master on the bus can choose to switch the connected slave devices to HS mode. The slave device must then recognize the "S 00001XXX A" sequence and switch its internal circuit from Fast mode to HS mode. Each device must recognize the STOP condition and switch back to Fast mode Timings and flow are shown in the figures below.

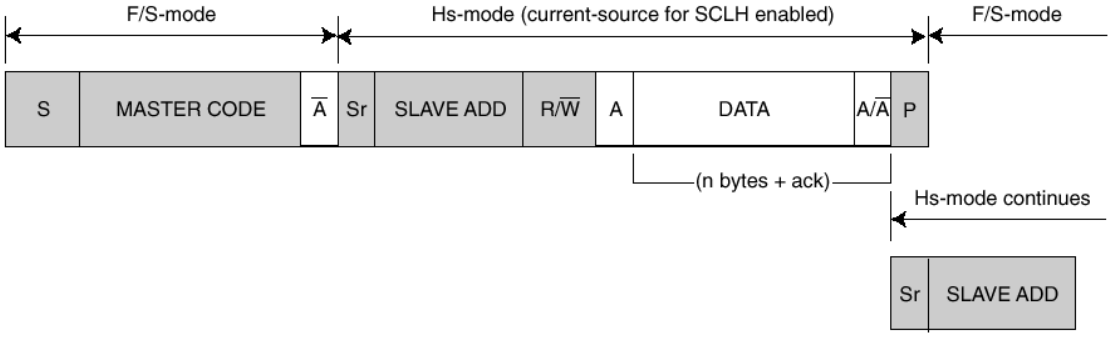


Figure 10. Data Transfer in Hs-mode

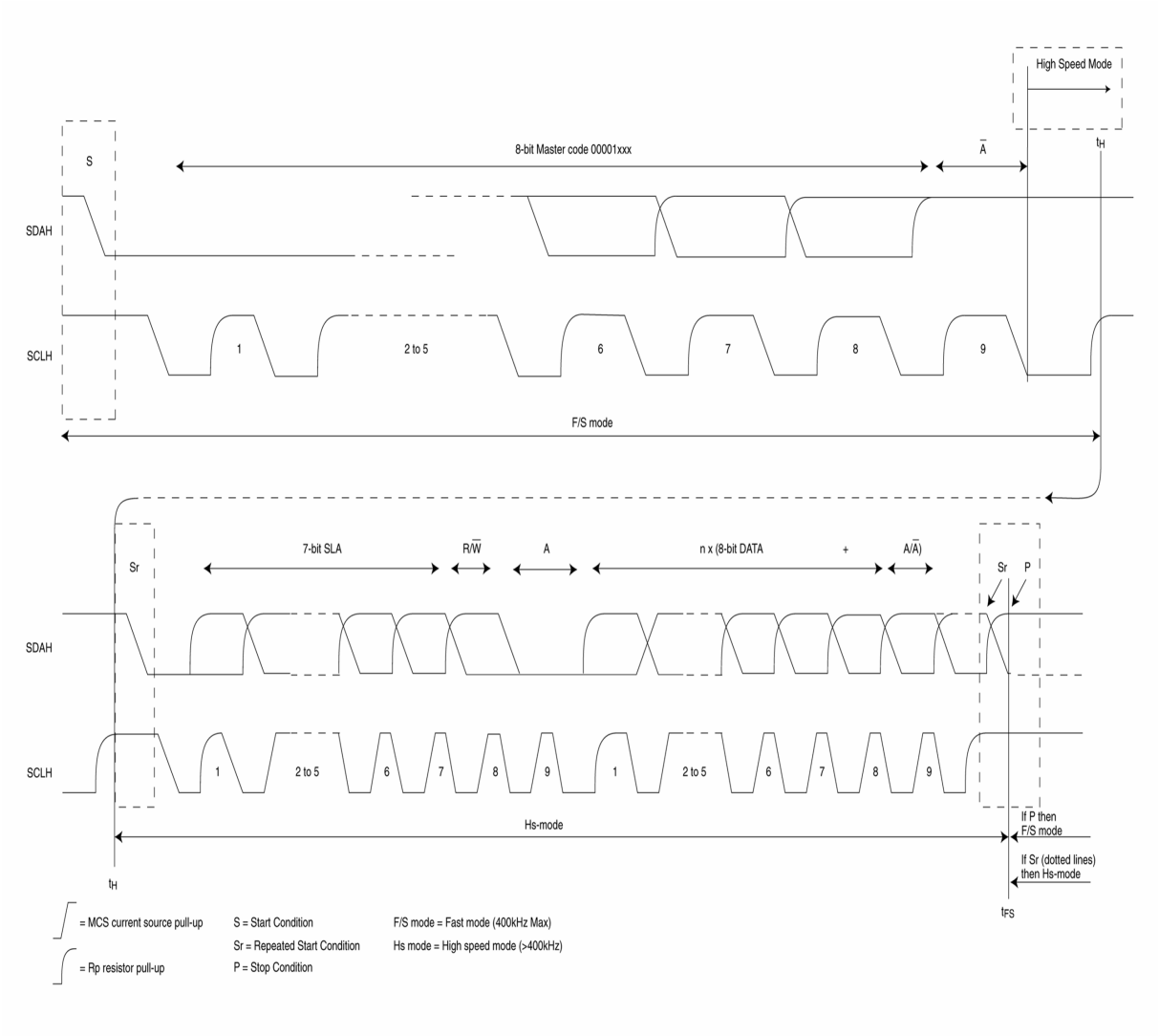


Figure 11. A Complete Hs-mode Transfer

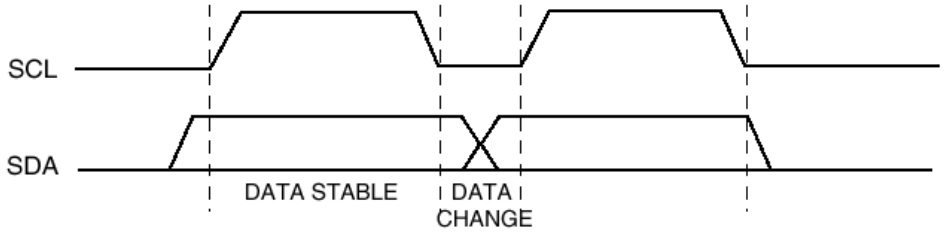


Figure 12. Data Validity

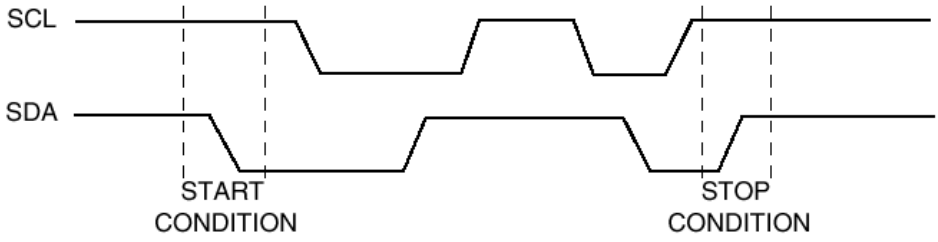


Figure 13. START and STOP Definition

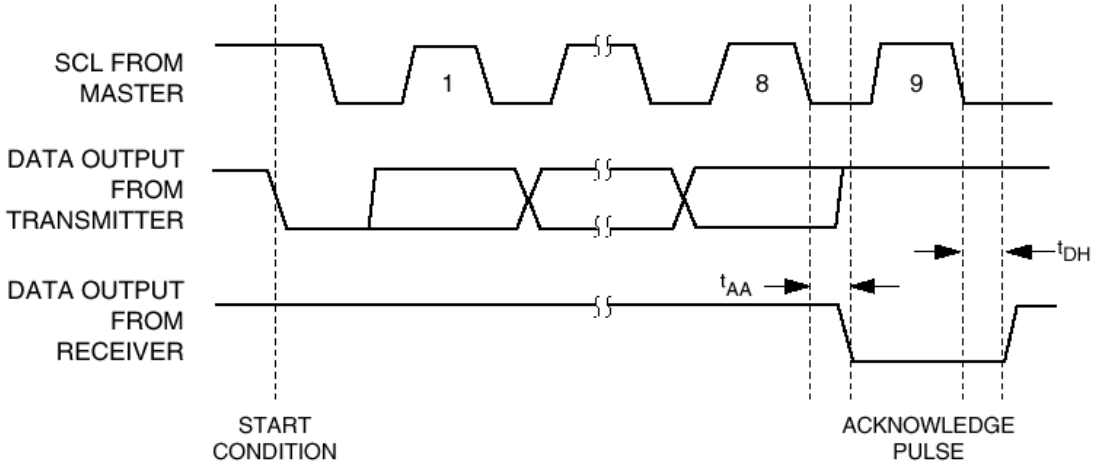


Figure 14. Acknowledge Response from Receiver

Write Operations

Byte Write

Two bytes of address are required after the slave address for a Byte Write operation. These two bytes select one out of the 64K locations in the memory. The master provides these two address bytes and for each address byte received, SA24C512 responds with an Acknowledge pulse. The master then provides a byte of data to be written into the memory. Upon receipt of this data, the SA24C512 responds with an Acknowledge pulse. The master then terminates the transfer by generating a STOP condition, at which time the SA24C512 begins the internal Write cycle to the memory. While the internal Write cycle is in progress, the SA24C512 inputs are disabled, and the device will not respond to any requests from the master for the duration of t_{WR}. Refer to Figure 15 for the address, acknowledge and data transfer sequence.

Page Write

To minimize Write cycle time, the SA24C512 offers a Page Write feature, which allows simultaneous programming of up to 128 contiguous bytes. To facilitate this feature, the memory array is organized in terms of “pages.” A page consists of 128 contiguous byte locations starting at every 128-Byte address boundary (for example, starting at array address 0x0000, 0x0080, 0x0100, and so on).

The Page Write operation is confined to a single page, which means that it will not cross over to locations on the next page but instead “rolls over” to the beginning of the page whenever the end of a page is reached and additional data bytes continue to be provided. A Page Write operation can be initiated to begin at any location within a page (the starting address of the Page Write operation need not be the starting address of a page).

Page Write is initiated in the same manner as the Byte Write operation, but instead of terminating the cycle after transmitting the first data byte, the master can further transmit up to 127 more bytes. After the receipt of each byte, the SA24C512 will respond with an Acknowledge pulse, increment the internal address counter to the next address, and becomes ready to accept the next data. If the master should transmit more than 128 bytes prior to generating the STOP condition, the address counter will “roll over” and previously loaded data will be re-loaded. As with the Byte Write operation, all inputs are disabled until completion of the internal Write cycle. Refer to Figure 16 for the address, acknowledge, and data transfer sequence.

Acknowledge Polling

Once the STOP condition is issued to indicate the end of the host's Write operation, the SA24C512 initiates the internal Write cycle. ACK polling can be initiated immediately, which involves issuing the START condition followed by the slave address for a Write operation. If the SA24C512 is still busy with the Write operation, no ACK will be returned. If the SA24C512 has completed the Write operation, an ACK will be returned and the host can then proceed with the next Read or Write operation.

Write Protection

Programming the memory will not take place if the WP pin of the SA24C512 is pulled HIGH. The SA24C512 will respond to the slave and byte addresses, but will not generate an Acknowledge after the first byte of data has been received. Thus, the program cycle will not be started when the STOP condition is asserted.

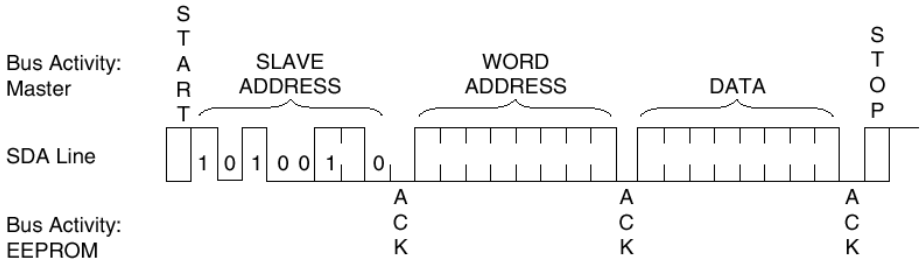


Figure 15. Byte Write

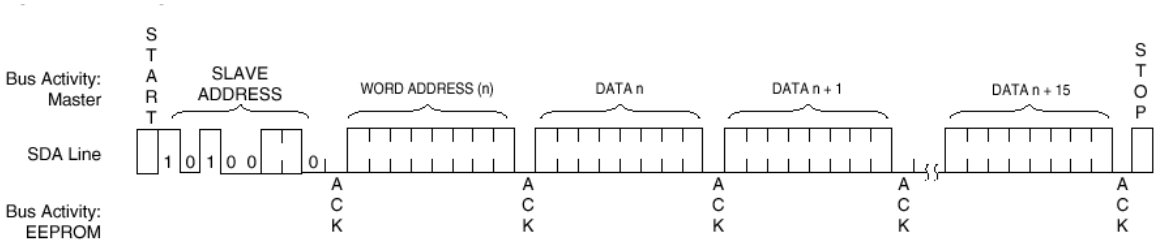


Figure 16. Page Write

Read Operations

Read operations are initiated in the same manner as Write operations, with the exception that the R/$\overline{W}$ bit of the slave address is set to 1. There are three basic Read operations: current address Read, random Read and sequential Read.

Current Address Read

Internally, the SA24C512 contains an address counter that maintains the address of the last byte accessed, incremented by 1. Therefore, if the last access (either a Read or Write) was to address n, the next Read operation would access data from address n + 1. Upon receipt of the slave address with R/$\overline{W}$ set to 1, the SA24C512 issues an Acknowledge and transmits the 8-bit word. The master will not acknowledge the transfer but does generate a STOP condition, and therefore the SA24C512 discontinues transmission. Refer to Figure 17 for the address, acknowledge and data transfer sequence.

Random Read

Random Read operations enable the master to access any memory location in a random manner. Prior to issuing the slave address with the R/$\overline{W}$ bit set to 1, the master must first perform a “dummy” Write operation. The master issues the START condition, the slave address with the R/$\overline{W}$ bit set to 0 and then the byte address is read.

After the byte address is acknowledged, the master immediately issues another START condition and the slave address with the R/$\overline{W}$ bit set to 1. This will be followed by an Acknowledge from the SA24C512 and then by the 8-bit word. The master will not acknowledge the transfer but does generate the STOP condition, and therefore the SA24C512 discontinues transmission. Refer to Figure 18 for the address, acknowledge, and data transfer sequence.

Sequential Read

Sequential Reads can be initiated as either a current address Read or random access Read. The first word is transmitted in the same manner as the other Read modes; however, the master now responds with an Acknowledge, indicating it requires additional data. The SA24C512 continues to output data for each Acknowledge received. The Read operation is terminated by the master not responding with an Acknowledge or by generating a STOP condition.

The data output is sequential with the data from address n followed by the data from n + 1. The address counter for Read operations increments all word address bits, allowing the entire memory contents to be serially read during one operation. After the entire memory has been read, the counter "rolls over" to the beginning of the memory. The SA24C512 continues to output data for each Acknowledge received. Refer to Figure 19 for the address, acknowledge, and data transfer sequence.

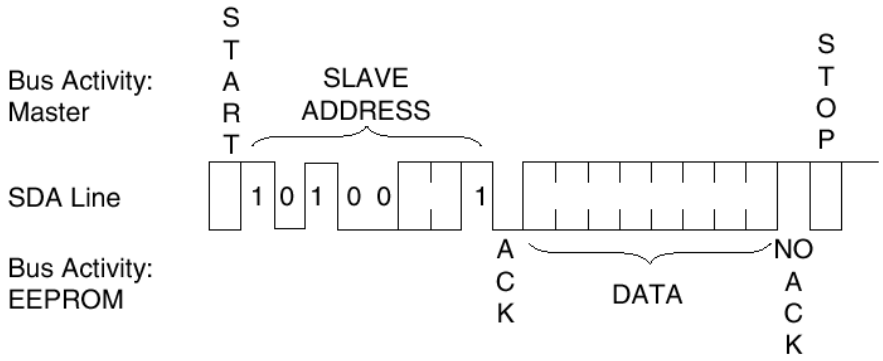


Figure 17. Current Address Read

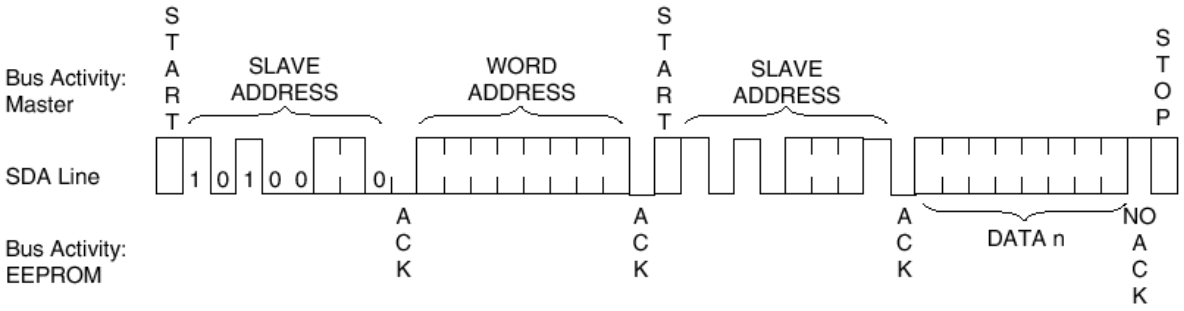


Figure 18. Random Read

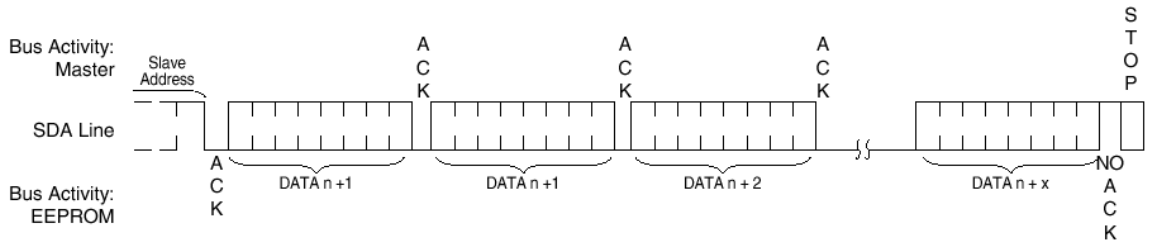
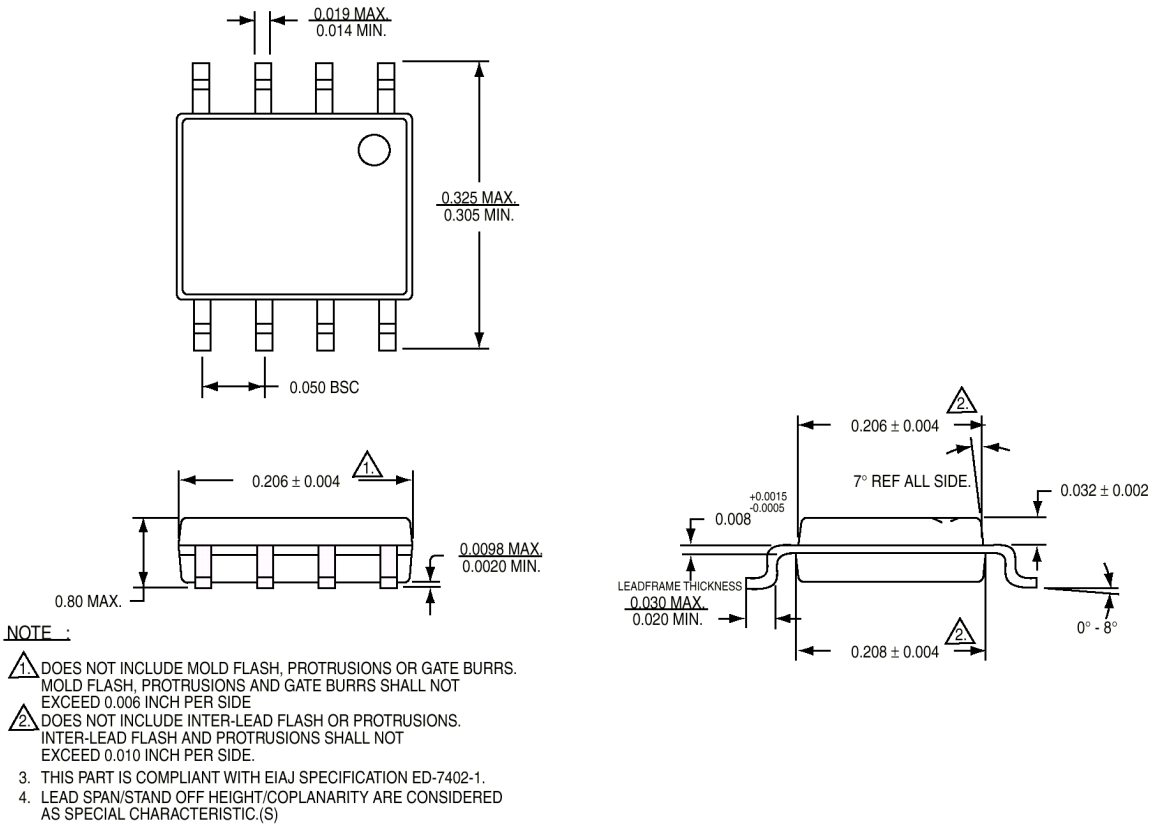


Figure 19. Sequential Read

Physical Dimensions

All measurements are in inches (millimeters), unless otherwise specified.



NOTE :

1. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.006 INCH PER SIDE
2. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.010 INCH PER SIDE.
3. THIS PART IS COMPLIANT WITH EIAJ SPECIFICATION ED-7402-1.
4. LEAD SPAN/STAND OFF HEIGHT/COPLANARITY ARE CONSIDERED AS SPECIAL CHARACTERISTIC.(S)

Figure 20. 8-Pin Molded Small Outline Package (MW) Package Number M08D

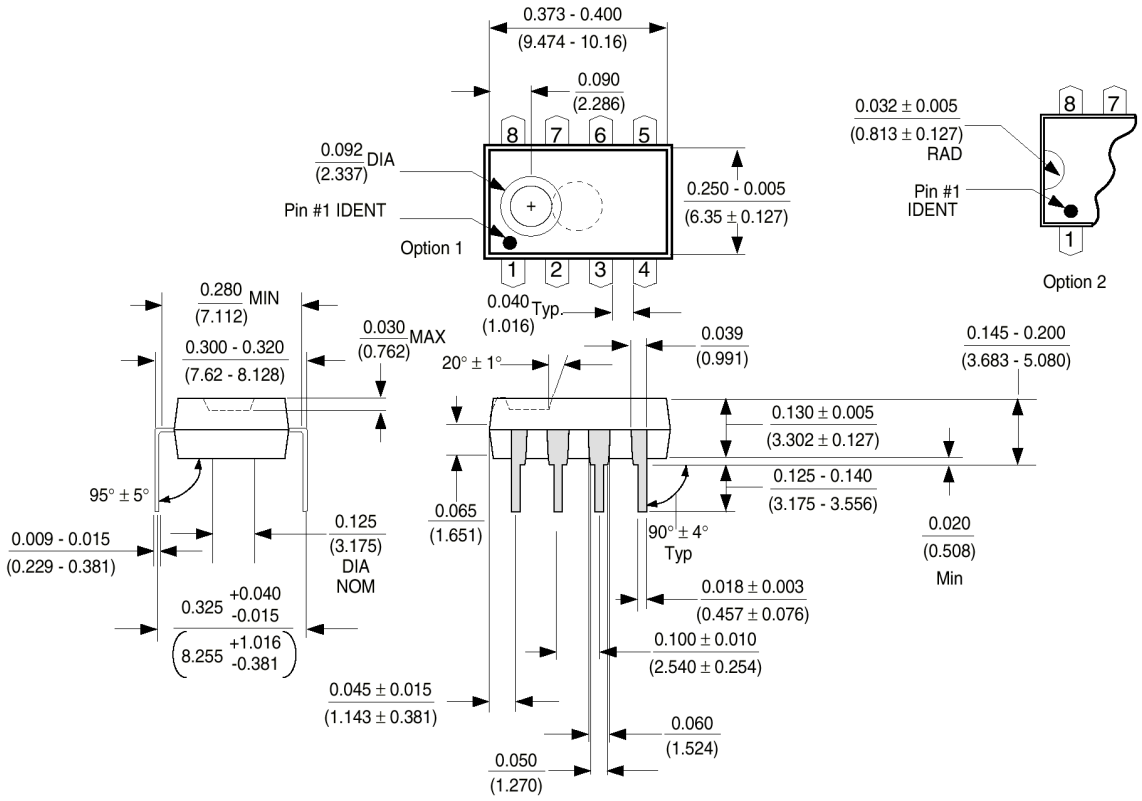
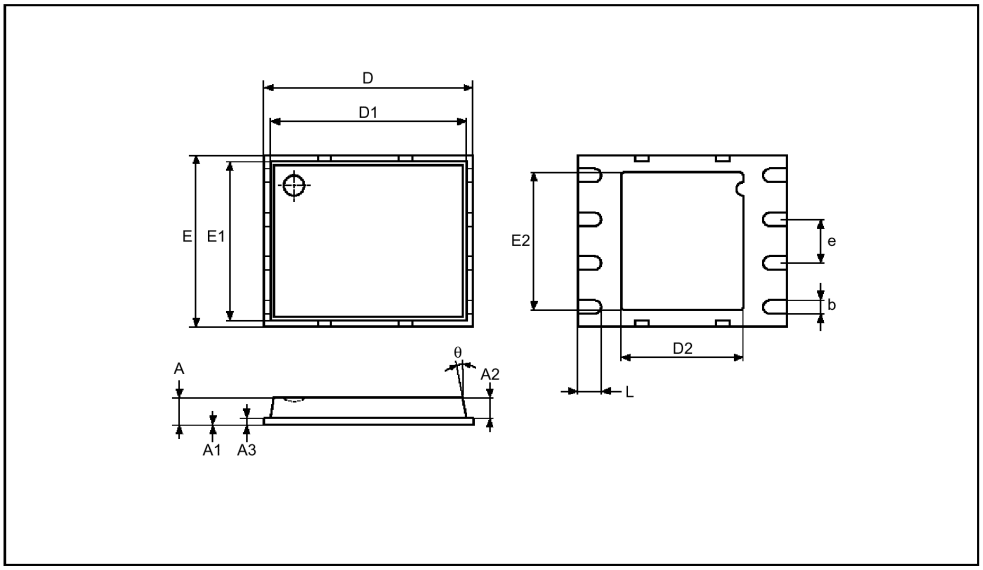


Figure 21. Molded Dual-in-Line Package (N) Package Number N08E



Note: Drawing is not to scale.

Symb.	mm			inches		
	Typ.	Min.	Max.	Typ.	Min.	Max.
A	0.85		1.00	0.0335		0.0394
A1		0.00	0.05		0.0000	0.0020
A2	0.65			0.0256		
A3	0.20			0.0079		
b	0.40	0.35	0.48	0.0157	0.0138	0.0189
D	6.20			0.2400		
D1	5.75			0.2264		
D2	3.40	3.20	3.60	0.1339	0.1260	0.1417
E	5.00			0.1969		
E1	4.75			0.1870		
E2	4.00	3.80	4.20	0.1575	0.1496	0.1654
e	1.27			0.0500		
L	0.60	0.50	0.75	0.0236	0.0197	0.0295
θ			12°			12°

Figure 22. 8-pin MLF Leadless Package

Contact Information

International Headquarters
Saifun Semiconductors Ltd.
ELROD Building
45 Hamelach St.
Sappir Industrial Park
Netanya 42504
Israel

Tel.: +972-9-892-8444
Fax: +972-9-892-8445

United States
Saifun Semiconductors Inc.
2350 Mission College Blvd.
Suite 1070
Santa Clara, CA 95054
U.S.A.

Tel: +1-408-982-5888
Fax: +1-408-982-5890

Email: tech_support@saifun.com
http://www.saifun.com

Revision History

Rev.	Date	Description of Change
0.0	5 Sept 2002	Initial Release
1.0	4-Aug-2003	Added MLF Package and minor format improvements
1.1	10-Sept 2003	Changed Endurance to 1 million cycles

Life Support Policy

Saifun's products are not authorized for use as critical components in life support devices or systems without the express written approval of the President of Saifun Semiconductors Ltd. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.