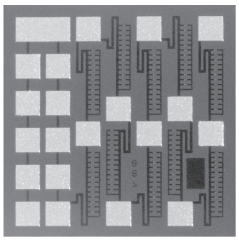
Thin Film Multi-Tap Resistors



Product may not be to scale

The MTT multi-tap resistors offer nineteen taps allowing the user to select specified increments and a wide range of values. The desired resistance value is obtained by bonding the wires to the appropriate pads.
These chips are manufactured using Vishay Electro-Films (EFI) sophisticated Thin Film equipment and manufacturing technology. The MTT's are 100% electrically tested and visually inspected to MIL-STD-883.

FEATURES

- Selectable values by wire bonding
- Resistance range: 1.1kΩ to 275kΩ
- Chip size: 0.038 inches square
- Resistor material tantalum nitride, self-passivating
- Oxidized silicon substrate for good power dissipation
- Ideally suited for hybrid prototyping

APPLICATIONS

The MTT series of multi-tap resistor chips are designed to satisfy the requirements of prototype development and circuit trimming in hybrid packages through selective wire-bonding.

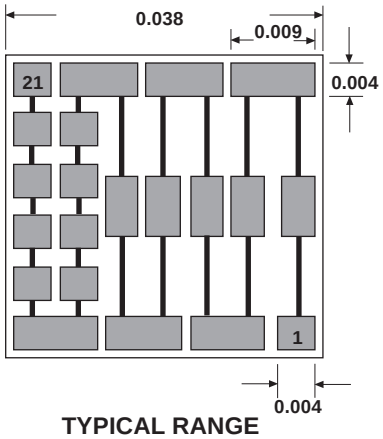
TEMPERATURE COEFFICIENT OF RESISTANCE, VALUE AND TOLERANCES	
Total resistance range	1.1kΩ, 2.75kΩ, 5.5kΩ, 11kΩ, 27.5kΩ, 55kΩ, 110kΩ, 275kΩ
10 resistors between Pads 1 and 11 10 resistors between Pads 11 and 21	Each 9.1% of total resistance Each 0.91% of total resistance
Standard tolerances	± 1%, ± 5%, ± 10%, ± 20% of total resistance of all 20 resistors
TCR	± 250ppm/°C

EXAMPLE: When the total resistance value is 55kΩ, the resistors between pads 11 and 21 are 500Ω each, and the resistors between Pads 1 and 11 are 5kΩ each.

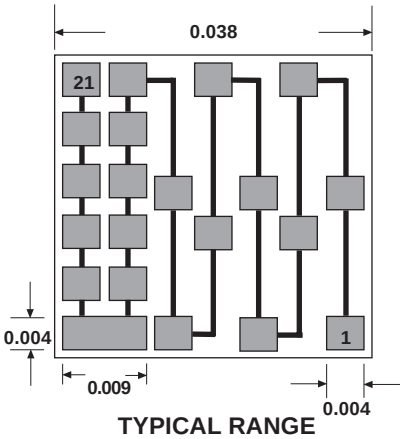
STANDARD ELECTRICAL SPECIFICATIONS	
PARAMETER	
TCR tracking between elements	± 5ppm/°C
Noise, MIL-STD-202, Method 308	- 30dB typical
Moisture resistance, MIL-STD-202, Method 106	± 0.5% maximum ΔR/R
Stability, 1000 hours, + 125°C, 125mW	± 0.5% maximum ΔR/R
Operating temperature range	- 55°C to + 125°C
Thermal shock, MIL-STD-202 Method 107, Test condition F	± 0.25% maximum ΔR/R
High temperature exposure ± 150°C, 100 hours	± 0.5% maximum ΔR/R
Dielectric voltage breakdown	200V
Insulation resistance	10^{12} minimum
Operating voltage	100V maximum
DC power rating at + 70°C, (derated to zero at 175°C)	250mW, total R
5 x rated power short-time overload, + 25°C, 5 seconds	± 0.25% maximum ΔR/R

VISHAY ELECTRO-FILMS • FRANCE +33.4.93.37.28.24 FAX: +33.4.93.37.27.31 • GERMANY +49.9287.710 FAX: +49 9287.70435 • ISRAEL +972.3.557.0945 FAX: +972.3.558.9121 • ITALY + 39.2.300.11911 FAX: +39.2.300.11999 • JAPAN +81.3.5464.6411 FAX: +81.3.5464.6433 • SINGAPORE +65.788.6668 FAX: +65.788.0988 • SWEDEN +46.8.594.70590 FAX: +46.8.594.70581 • UK +44 191 514 8237 FAX: +44 1953 457 722 • USA: (401) 738-9150 FAX: (401) 738-4389

DIMENSIONS in inches

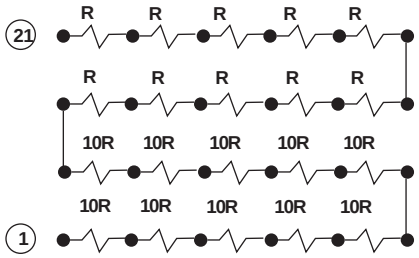


TYPICAL RANGE
1.0kΩ - 5.5kΩ



TYPICAL RANGE
11kΩ - 275kΩ

SCHEMATIC



R_T = 110R

MECHANICAL SPECIFICATIONS in inches

PARAMETER	
Chip size	0.038 x 0.038 ± 0.002 (0.762 x 0.762mm)
Chip thickness	0.010 ± 0.002 (0.254 ± 0.05mm)
Chip substrate material	Oxidized silicon, 10kÅ minimum SiO_2
Resistor material	Tantalum nitride, self-passivating
Bonding pads	0.004 x 0.004 (0.10 x 0.10mm)
Number of pads	21
Pad material	10kÅ minimum aluminum
Backing	None, lapped semiconductor silicon

OPTIONS: Gold back for eutectic die attach
Gold bonding pads 15kÅ minimum thickness
Other values available on request, Consult Application Engineer

ORDERING INFORMATION

Example: 100% visualled, 55kΩ, ± 10%, ± 250ppm/°C TCR, Aluminum Pads, Class H

P/N:	**W**	**MTT**	**002**	**5500**	**1**	**K**
	INSPECTION /PACKAGING	PRODUCT FAMILY	PROCESS CODE	RESISTANCE VALUE	MULTIPLIER CODE	TOLERANCE CODE
	W = 100% visually inspected parts in matrix tray per MIL-STD-883 **X** = Sample, commercial visually inspected parts in matrix trays (4% AQL)		002 = Class H 008 = Class K See Process Code table	Use first 4 significant digits of the resistance (R_T)	**A** = 0.1 **0** = 1 **1** = 10 **2** = 100	**K** = 10% **M** = 20% **L** = 25% **N** = 50%