

74VHC125FT,74VHC126FT

1. Functional Description

- Quad Bus Buffer, Non-Inverted 3-State Outputs
74VHC125FT: Quad Bus Buffer
74VHC126FT: Quad Bus Buffer

2. General

The 74VHC125FT/126FT are high speed CMOS QUAD BUS BUFFERS fabricated with silicon gate C²MOS technology.

They achieve the high speed operation similar to equivalent Bipolar Shottky TTL while maintaining the CMOS low power dissipation.

The 74VHC125FT requires the 3-state control input \bar{G} to be set high to place the output into the high impedance state, whereas the 74VHC126FT requires the control input G to be set low to place the output into high impedance.

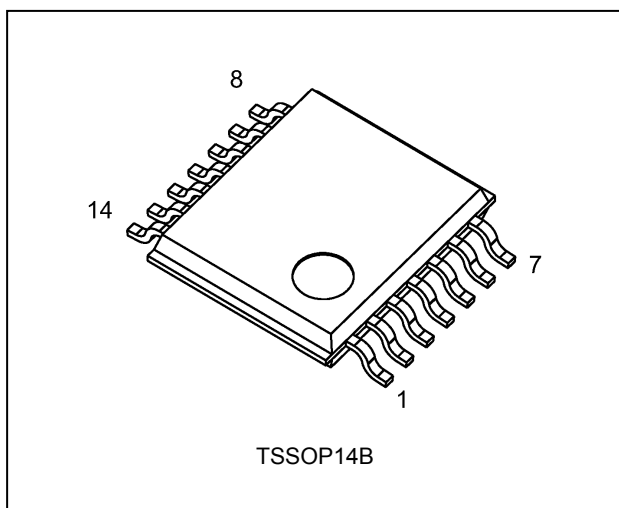
An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up.

This circuit prevents device destruction due to mismatched supply and input voltages.

3. Features

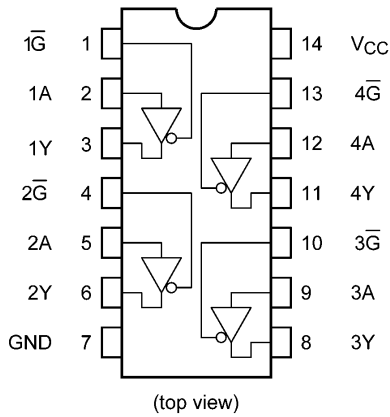
- (1) High speed: Propagation delay time = 3.8 ns (typ.) at $V_{CC} = 5$ V
- (2) Low power dissipation: $I_{CC} = 4$ μ A (max) at $T_a = 25$ °C
- (3) High noise immunity: $V_{NIH} = V_{NIL} = 28\%$ V_{CC} (min)
- (4) Power down protection is provided on all inputs.
- (5) Balanced propagation delays: $t_{PLH} \approx t_{PHL}$
- (6) Wide operating voltage range: $V_{CC(opr)} = 2$ V to 5.5 V
- (7) Low noise: $V_{OLP} = 0.8$ V (max)
- (8) Pin and function compatible with 74 series (74AC/HC/AHC/LV etc.) 125 or 126 type.

4. Packaging

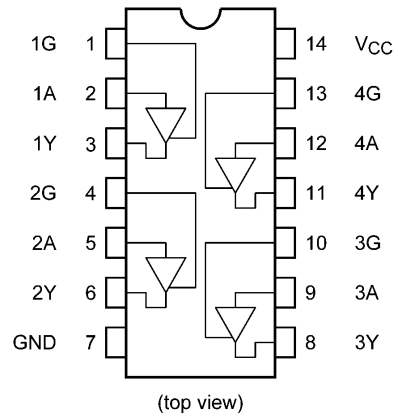


5. Pin Assignment

74VHC125FT

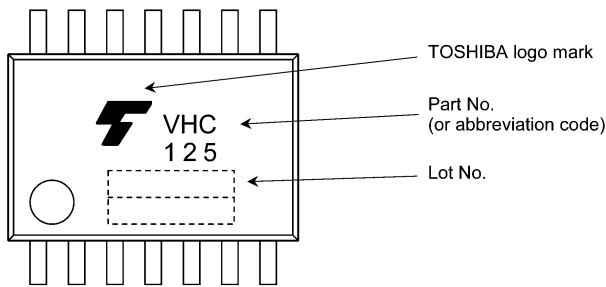


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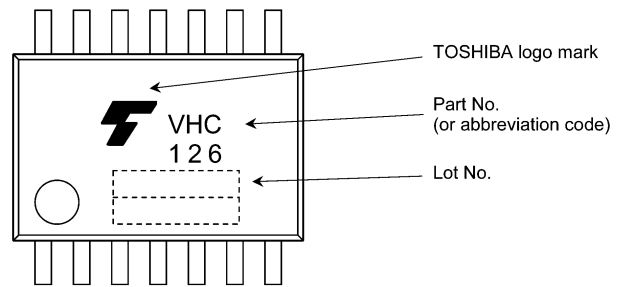


6. Marking

74VHC125FT

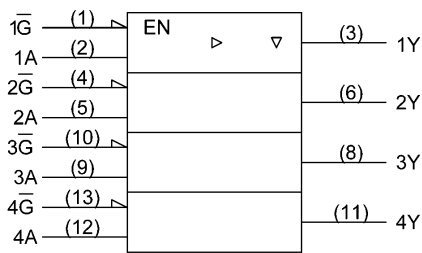


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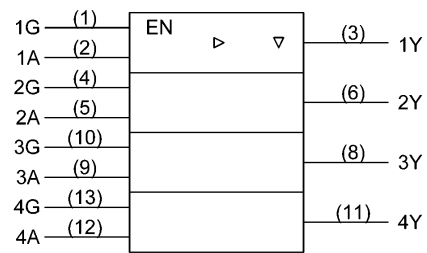


7. IEC Logic Symbol

74VHC125FT



74VHC126FT



8. Truth Table

Input \bar{G} (74VHC125)	Input G (74VHC126)	Input A_n	Output Y_n
H	L	X	Z
L	H	L	L
L	H	H	H

X: Don't care
Z: High impedance

9. Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	V_{CC}	-0.5 to 7.0	V
Input voltage	V_{IN}	-0.5 to 7.0	
Output voltage	V_{OUT}	-0.5 to $V_{CC} + 0.5$	
Input diode current	I_{IK}	-20	mA
Output diode current	I_{OK}	± 20	
Output current	I_{OUT}	± 25	
V_{CC} /ground current	I_{CC}	± 50	
Power dissipation	P_D	180	mW
Storage temperature	T_{stg}	-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

10. Operating Ranges (Note)

Characteristics	Symbol	Test Condition	Rating	Unit
Supply voltage	V_{CC}		2.0 to 5.5	V
Input voltage	V_{IN}		0 to 5.5	
Output voltage	V_{OUT}		0 to V_{CC}	
Operating temperature	T_{opr}		-40 to 85	$^{\circ}C$
Input rise and fall times	dt/dv	$V_{CC} = 3.3 \pm 0.3 V$	0 to 100	ns/V
		$V_{CC} = 5 \pm 0.5 V$	0 to 20	

Note: The operating ranges must be maintained to ensure the normal operation of the device.
Unused inputs and bus inputs must be tied to either V_{CC} or GND.

11. Electrical Characteristics

11.1. DC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Typ.	Max	Unit	
High-level input voltage	V_{IH}	—	2.0	1.50	—	—	V	
			3.0 to 5.5	$V_{CC} \times 0.7$	—	—		
Low-level input voltage	V_{IL}	—	2.0	—	—	0.50	V	
			3.0 to 5.5	—	—	$V_{CC} \times 0.3$		
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	2.0	—	V
				3.0	2.9	3.0	—	
				4.5	4.4	4.5	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.58	—	—	
4.5	3.94	—		—				
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.0	0.1	V
				3.0	—	0.0	0.1	
				4.5	—	0.0	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	—	0.36	
				4.5	—	—	0.36	
3-state output OFF-state leakage current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5	—	—	± 0.25	μA	
Input leakage current	I_{IN}	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	—	± 0.1	μA	
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	μA	

11.2. DC Characteristics (Unless otherwise specified, $T_a = -40$ to $85\text{ }^\circ\text{C}$)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Min	Max	Unit	
High-level input voltage	V_{IH}	—	2.0	1.50	—	V	
			3.0 to 5.5	$V_{CC} \times 0.7$	—		
Low-level input voltage	V_{IL}	—	2.0	—	0.50	V	
			3.0 to 5.5	—	$V_{CC} \times 0.3$		
High-level output voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -50\text{ }\mu\text{A}$	2.0	1.9	—	V
				3.0	2.9	—	
				4.5	4.4	—	
			$I_{OH} = -4\text{ mA}$	3.0	2.48	—	
4.5	3.80	—					
Low-level output voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 50\text{ }\mu\text{A}$	2.0	—	0.1	V
				3.0	—	0.1	
				4.5	—	0.1	
			$I_{OL} = 4\text{ mA}$	3.0	—	0.44	
				4.5	—	0.44	
3-state output OFF-state leakage current	I_{OZ}	$V_{IN} = V_{IH}$ or V_{IL} $V_{OUT} = V_{CC}$ or GND	5.5	—	—	± 2.50	μA
Input leakage current	I_{IN}	$V_{IN} = 5.5\text{ V}$ or GND	0 to 5.5	—	—	± 1.0	μA
Quiescent supply current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	40.0	μA

11.3. AC Characteristics (Unless otherwise specified, $T_a = 25\text{ }^\circ\text{C}$, Input: $t_r = t_f = 3\text{ ns}$)

Characteristics	Part Number	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Typ.	Max	Unit
Propagation delay time	74VHC125FT	t_{PLH}, t_{PHL}		—	3.3 ± 0.3	15	—	5.6	8.0	ns
						50	—	8.1	11.5	
					5.0 ± 0.5	15	—	3.8	5.5	
						50	—	5.3	7.5	
	74VHC126FT	t_{PLH}, t_{PHL}		—	3.3 ± 0.3	15	—	5.6	8.0	
						50	—	8.1	11.5	
					5.0 ± 0.5	15	—	3.8	5.5	
						50	—	5.3	7.5	
3-state output enable time		t_{PZL}, t_{PZH}		$R_L = 1\text{ k}\Omega$	3.3 ± 0.3	15	—	5.4	8.0	ns
						50	—	7.9	11.5	
					5.0 ± 0.5	15	—	3.6	5.1	
						50	—	5.1	7.1	
3-state output disable time		t_{PLZ}, t_{PHZ}		$R_L = 1\text{ k}\Omega$	3.3 ± 0.3	50	—	9.5	13.2	ns
					5.0 ± 0.5	50	—	6.1	8.8	
Output skew		t_{osLH}, t_{osHL}	(Note 1)	—	3.3 ± 0.3	50	—	—	1.5	ns
					5.0 ± 0.5	50	—	—	1.0	
Input capacitance		C_{IN}		—			—	4	10	pF
Output capacitance		C_{OUT}		—			—	6	—	pF
Power dissipation capacitance	74VHC125FT	C_{PD}	(Note 2)	—			—	14	—	pF
	74VHC126FT						—	15	—	

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

Note 2: C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation.

$$I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/4 \text{ (per gate)}$$

11.4. AC Characteristics
 (Unless otherwise specified, $T_a = -40$ to 85 °C, Input: $t_r = t_f = 3$ ns)

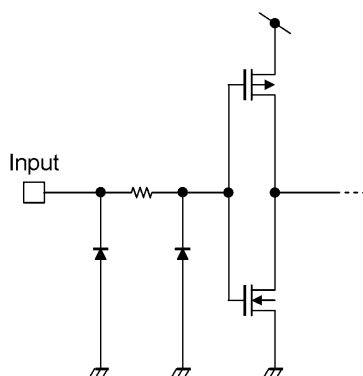
Characteristics	Part Number	Symbol	Note	Test Condition	V_{CC} (V)	C_L (pF)	Min	Max	Unit
Propagation delay time	74VHC125FT	t_{PLH}, t_{PHL}		—	3.3 ± 0.3	15	1.0	9.5	ns
						50	1.0	13.0	
					5.0 ± 0.5	15	1.0	6.5	
						50	1.0	8.5	
	74VHC126FT	t_{PLH}, t_{PHL}		—	3.3 ± 0.3	15	1.0	9.5	
						50	1.0	13.0	
5.0 ± 0.5					15	1.0	6.5		
					50	1.0	8.5		
3-state output enable time		t_{PZL}, t_{PZH}		$R_L = 1$ k Ω	3.3 ± 0.3	15	1.0	9.5	ns
						50	1.0	13.0	
					5.0 ± 0.5	15	1.0	6.0	
						50	1.0	8.0	
3-state output disable time		t_{PLZ}, t_{PHZ}		$R_L = 1$ k Ω	3.3 ± 0.3	50	1.0	15.0	ns
					5.0 ± 0.5	50	1.0	10.0	
Output skew		t_{osLH}, t_{osHL}	(Note 1)	—	3.3 ± 0.3	50	—	1.5	ns
					5.0 ± 0.5	50	—	1.0	
Input capacitance		C_{IN}		—			—	10	pF

Note 1: Parameter guaranteed by design. ($t_{osLH} = |t_{PLHm} - t_{PLHn}|$, $t_{osHL} = |t_{PHLm} - t_{PHLn}|$)

11.5. Noise Characteristics (Unless otherwise specified, $T_a = 25$ °C, Input: $t_r = t_f = 3$ ns)

Characteristics	Symbol	Test Condition	V_{CC} (V)	Typ.	Limit	Unit
Quiet output maximum dynamic V_{OL}	V_{OLP}	$C_L = 50$ pF	5.0	0.3	0.8	V
Quiet output minimum dynamic V_{OL}	V_{OLV}	$C_L = 50$ pF	5.0	-0.3	-0.8	
Minimum high-level dynamic input voltage	V_{IHD}	$C_L = 50$ pF	5.0	—	3.5	
Maximum low-level dynamic input voltage	V_{ILD}	$C_L = 50$ pF	5.0	—	1.5	

11.6. Internal Equivalent Circuit



Package Dimensions

Unit: mm



Weight: 0.054 g (typ.)

Package Name(s)
Nickname: TSSOP14B

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