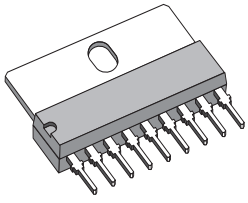
STV8130A/STV8130B

3.3V AND ADJUSTABLE VOLTAGE REGULATORS WITH DISABLE AND RESET

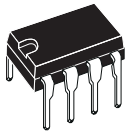
FEATURES

- Output currents up to 750mA for STV8130A and up to 200mA for STV8130B
- Fixed precision output 1 voltage 3.3V ± 2%
- Output 2 voltage programmable from 2.8V to 16V
- Output 1 with reset facility
- Output 2 with disable by TTL input
- Short circuit protection at both outputs
- Thermal protection
- Lowdrop output voltage



SIP9
(Plastic Package)

ORDER CODE: STV8130A



PDIP8
(Plastic Package)

ORDER CODE: STV8130B

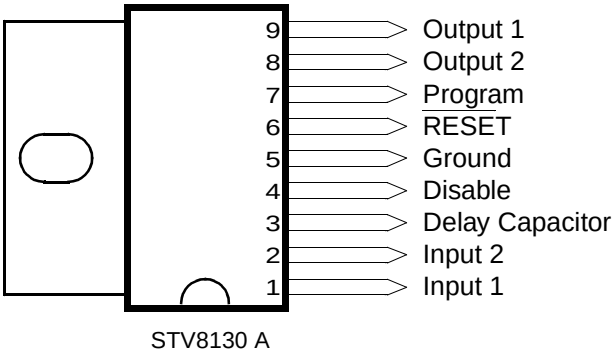
DESCRIPTION

The STV8130A and STV8130B are monolithic dual positive voltage regulators, designed to provide precision output voltages of 3.3V and adjustable, at currents up to 750mA for STV8130A and 200mA for STV8130B. The ability to deliver currents is the same for the two ICs, but the higher thermal resistor of PDIP8 does not allow to overpass 200mA for the STV8130B.

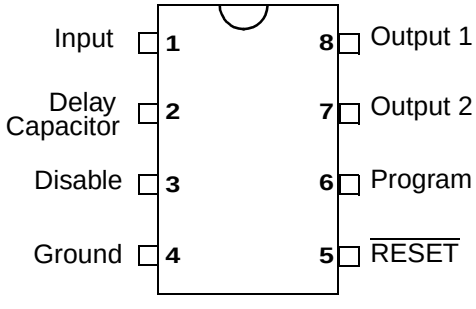
An internal reset circuit generates a reset pulse if Output 1 drops below the regulated voltage value.

Output 2 can be disabled by TTL input. Short circuit and thermal protections are included.

PIN CONNECTIONS



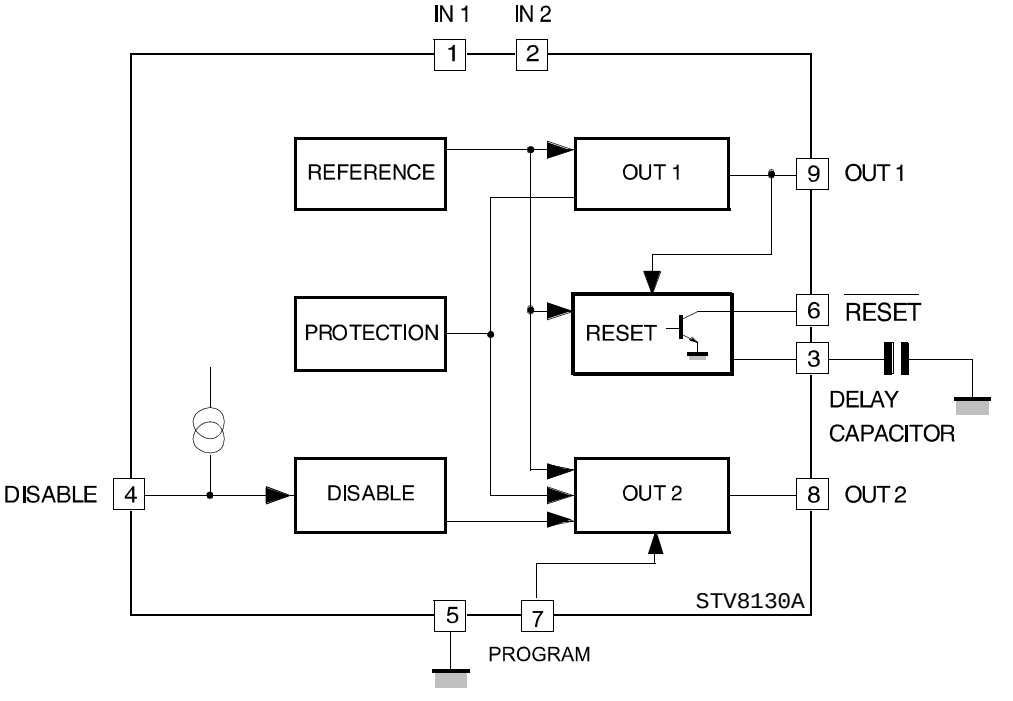
STV8130 A

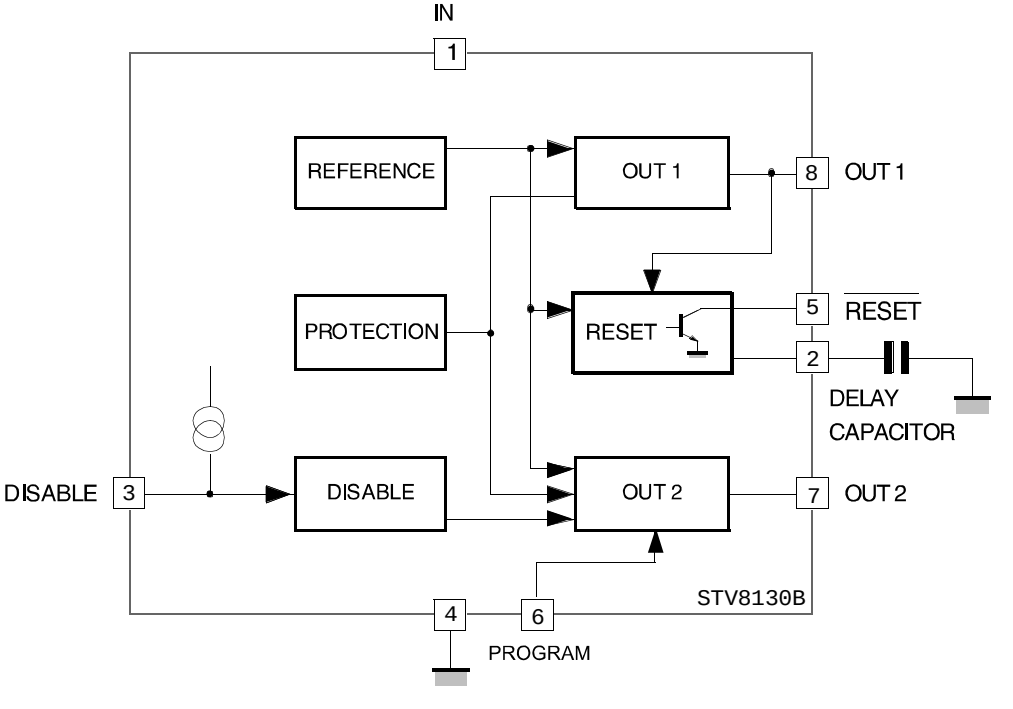


STV8130 B

Rev. 1.7

BLOCK DIAGRAMS





ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage Pin 1, 2 (STV8130A) or Pin 1 (STV8130B)	20	V
V_{DIS}	Disable Input Voltage Pin 4 (STV8130A) or Pin 3 (STV8130B)	20	V
V_{RST}	Output Voltage at Pin 6 (STV8130A) or Pin 5 (STV8130B)	20	V
$I_{O1, 2}$	Output Currents	Internally Limited	
P_t	Power Dissipation	Internally Limited	
T_{STG}	Storage Temperature	-65 to +150	°C
T_J	Junction Temperature	0 to +150	°C

THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{TH(l-c)}$	Thermal Resistance Junction Case of STV8130A	8	°C/W
	Thermal Resistance Junction Case of STV8130B	45	
T_J	Maximum Recommended Junction Temperature	130	°C
T_{OPER}	Operating Free Air Temperature Range	0 to 70	°C

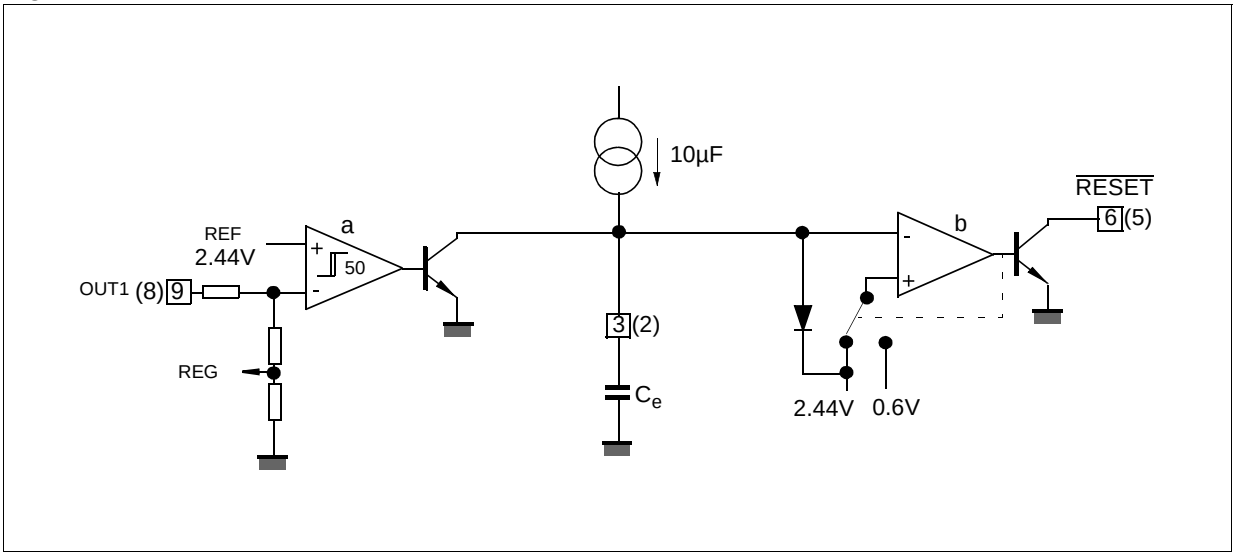
ELECTRICAL CHARACTERISTICS

(V_{IN} = 7V; T_J = 25°C unless otherwise specified)

Symbol	Parameter	Value	Min.	Typ.	Max.	Unit
V_{O1}	Output Voltage	I_{O1} = 10mA	3.23	3.30	3.37	V
V_{O2}	Output Voltage	I_{O2} = 10mA	2.8		16	V
$V_{O1, 2}$	Dropout Voltage	$I_{O1, 2}$ = 750mA (STV8130A)			1.4	V
		$I_{O1, 2}$ = 200mA (STV8130B)				
V_{O1}	Line Regulation 1	6V < V_{IN1} < 12V, 12V < V_{IN2} < 18V for STV 8130A and 7V < V_{IN} < 12V for STV8130B (@ V_{O2} : 10V, $I_{O1, 2}$ = 200mA)			50	mV
V_{O2}	Line Regulation 2				100	mV
V_{O1}	Load Regulation 1	5mA < $I_{O1, 2}$ < 0.6A, @ V_{O2} = 10V			100	mV
V_{O2}	Load Regulation 2				200	mV
I_Q	Quiescent Current	I_{O1} = 10mA, Output 2 Disabled			2	mA
V_{Q1RST}	Reset Threshold Voltage	(K = V_{O1})	K-0.4	K-.25	K-0.1	V
V_{RTH}	Reset Threshold Hysteresis	(see circuit description)	20	50	75	V
t_{RD}	Reset Pulse delay at Pin 6 (STV8130A) or pin 5 (STV8130B)	C_0 = 100nF (see circuit description)		25		ms
V_{RL}	Saturation Volt. at Pin 6 in Reset Condition for STV8130A	I_6 = 5mA			0.4	V
	Saturation Volt. at Pin 5 in Reset Condition for STV8130B	I_5 = 5mA				
I_{RH}	Leakage Current at Pin 6 in Normal Condition for STV8130A	V_6 = 10V			10	µA
	Leakage Current at Pin 5 in Normal Condition for STV8130A	V_5 = 10V				
$K_{O1, 2}$	Output Volt Thermal Drift	$K_O = \frac{\Delta V_O \cdot 10^6}{\Delta T \cdot V_O}$ T_j = 0 to + 125°C		100		ppm/°C
$I_{O1, 2\ sc}$	Short Circuit Output Current	V_{IN} = 7V			1.6	A
		V_{IN} = 16V (see [1])			1	A
V_{DISH}	Disable Volt. at Pin 4 High (out 2 active) for STV8130A		2			V
	Disable Volt. at Pin 3 High (out 2 active) for STV8130B					
V_{DISL}	Disable Volt. at Pin 4 Low (out 2 disabled) for STV8130A				0.8	V
	Disable Volt. at Pin 3 Low (out 2 disabled) for STV8130B					
I_{DIS}	Disable Bias Current at Pin 4 (STV8130A) or Pin 3 (STV8130B)	0V < V_{DIS} < 7V	-100		2	µA
V_{ref}	Pin 7 (STV8130A)			2.44		V
	Pin 6 (STV8130B)					
T_{JSD}	Junction Temp. for Thermal Shut Down			145		°C

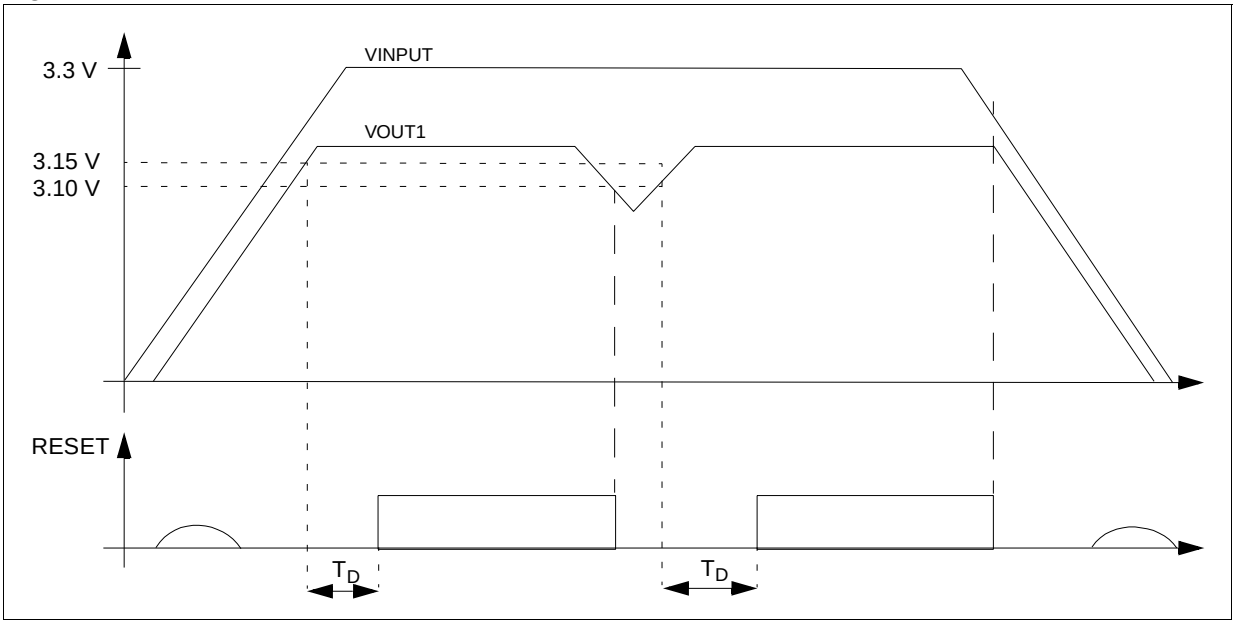
Note 1: The output short circuit currents are tested one channel at a time.
During a short circuit there is heavy consumption of power, but the thermal protection circuit prevents an excessively high temperature level being reached.
Safe permanent short circuits can only be guaranteed for input voltages up to16V.

Figure 1.



Note: Pin numbers are related to STV8130A. Numbers between brackets correspond to the pin numbers of STV8130B.

Figure 2.



CIRCUIT DESCRIPTION

The STV8130A and STV8130B are dual voltage regulators with Reset and Disable.

The two regulation parts are supplied from one voltage reference circuit trimmed by zener zap during EWS testing. Since the supply voltage of this last is connected at Pin 1 (V_{IN1}) in STV8130A, regulator 2 will not work if Pin 1 is not supplied.
In STV8130B, the two regulators are supplied by pin 1.

The output stages have been designed in a darlington configuration with a typical drop of 1.2V. The adjustable voltage of Output 2 is defined by output bridge resistors (R1, R2): the values of these resistors are calculated to obtain, with the targetted value for V02, the Vref voltage (2.44V) on the median point connected to PROGRAM (Pin 7 for STV8130A or Pin 6 for STV8130B).

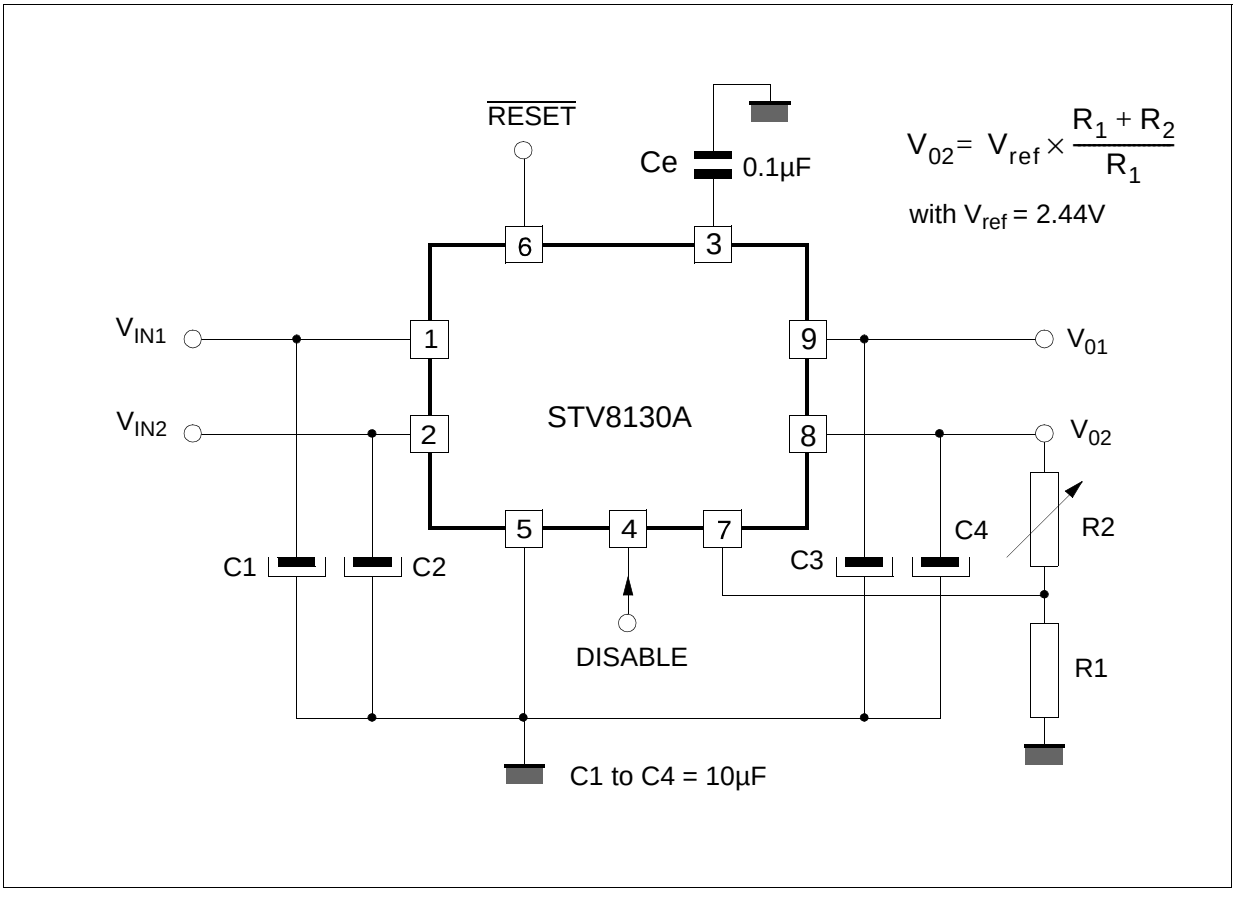
The disable circuit switches off Output 2 if a voltage of less than 0.8V is applied at Pin 4 (STV8130A) or Pin 3 (STV8130B).

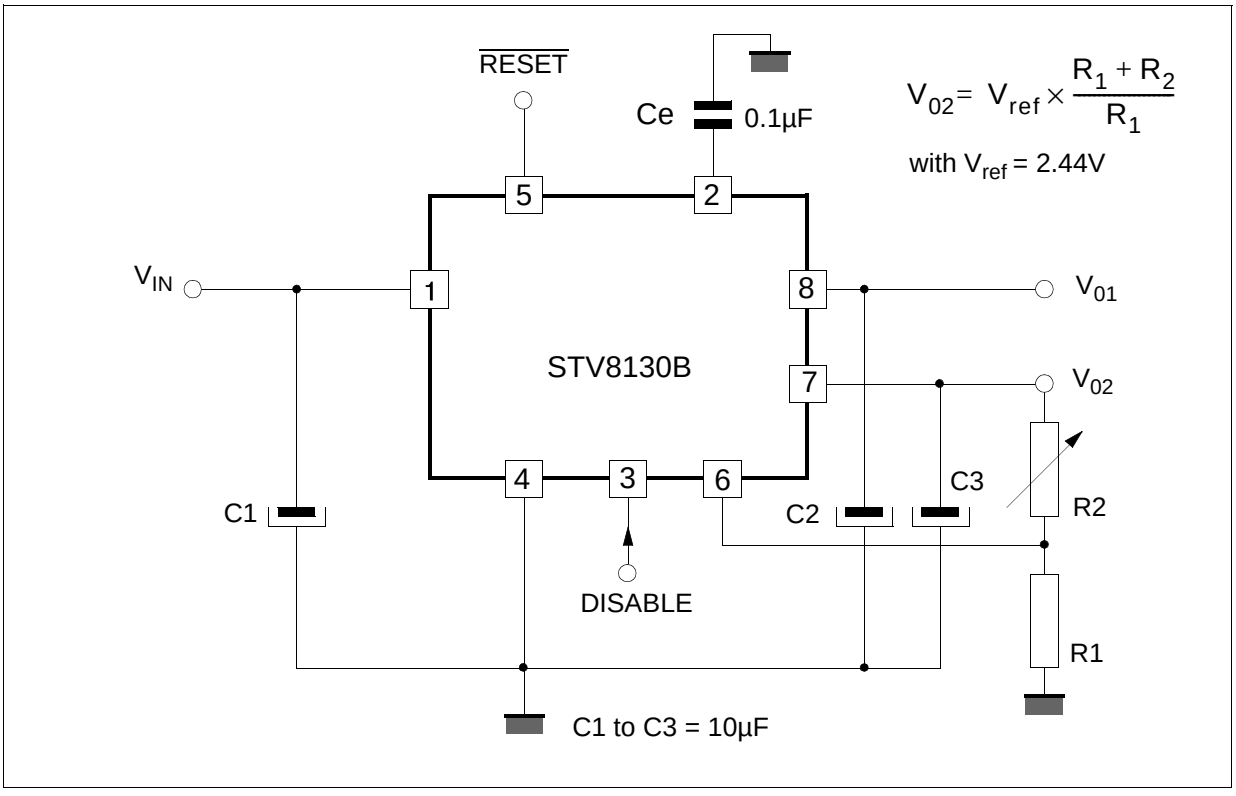
The Reset circuit checks the voltage at Output 1. If this drops below V_{OUT} - 0.20V (3.10V Typ.), then the first comparator “a” (see Figure 1) rapidly discharges the Capacitor Ce and the reset output immediately drops to low. This drop can be caused by a parasitic loading condition on Out 1 or by a too low value of V_{IN} (short powering off). Once the voltage at Out 1 rises above V_{OUT} -0.15V (3.15V Typ.), voltage V_{Ce} increases linearly to 2.44V corresponding to delay t_D following the law below (see Figure 2), then the reset output becomes high again.

$$t_D = \frac{(C_E \times 2.44V)}{10\mu A}$$

To avoid problems with the reset output, the second comparator “b” has a large hysteresis (1.9V).

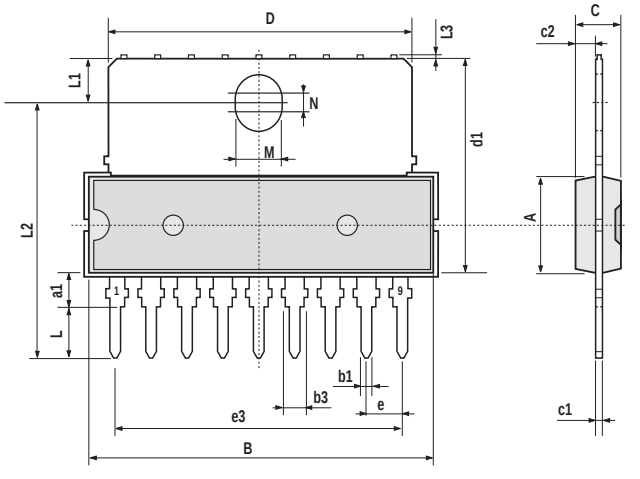
TYPICAL APPLICATION




RESET
Ce
0.1µF
$V_{02} = V_{ref} \times \frac{R_1 + R_2}{R_1}$
with V_{ref} = 2.44V
5
2
V_{IN}
1
8
V_{01}
STV8130B
7
V_{02}
4
3
6
C3
C1
C2
R2
DISABLE
R1
C1 to C3 = 10µF

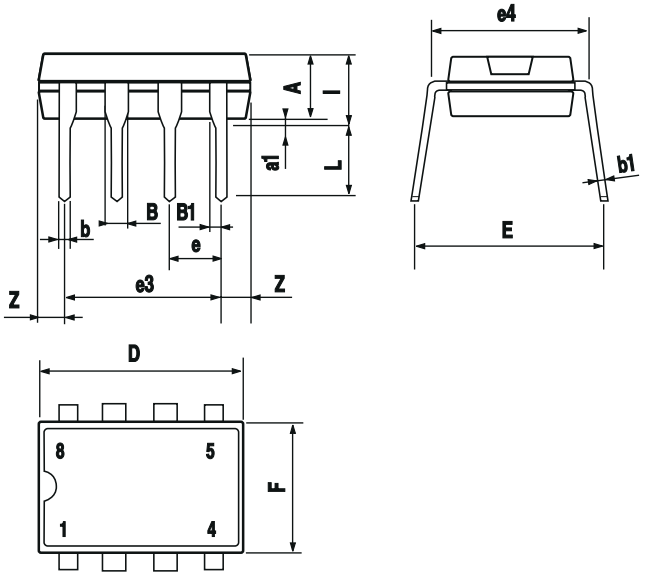
PACKAGE MECHANICAL DATA

Figure 3. 9-Pin Plastic Single In Line Package (STV8130A)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			7.1			0.280
a1	2.7		3	0.106		0.118
B			24.8			0.976
b1		0.5			0.020	
b3	0.85		1.6	0.033		0.063
C		3.3			0.130	
c1		0.43			0.017	
c2		1.32			0.052	
D			21.2			0.835
d1		14.5			0.571	
e		2.54			0.100	
e3		20.32			0.800	
L	3.1			1.122		
L1		3			0.116	
L2		17.6			0.693	
L3			0.25			0.010
M		3.2			0.126	
N		1			0.039	
	Number of Pins					
	9					

Figure 4. 8-Pin Plastic Dual In Line Package (STV8130B)



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060
	Number of Pins					
	8					