NOVATEK

NT6827

I²C Bus Controlled On-Screen Display

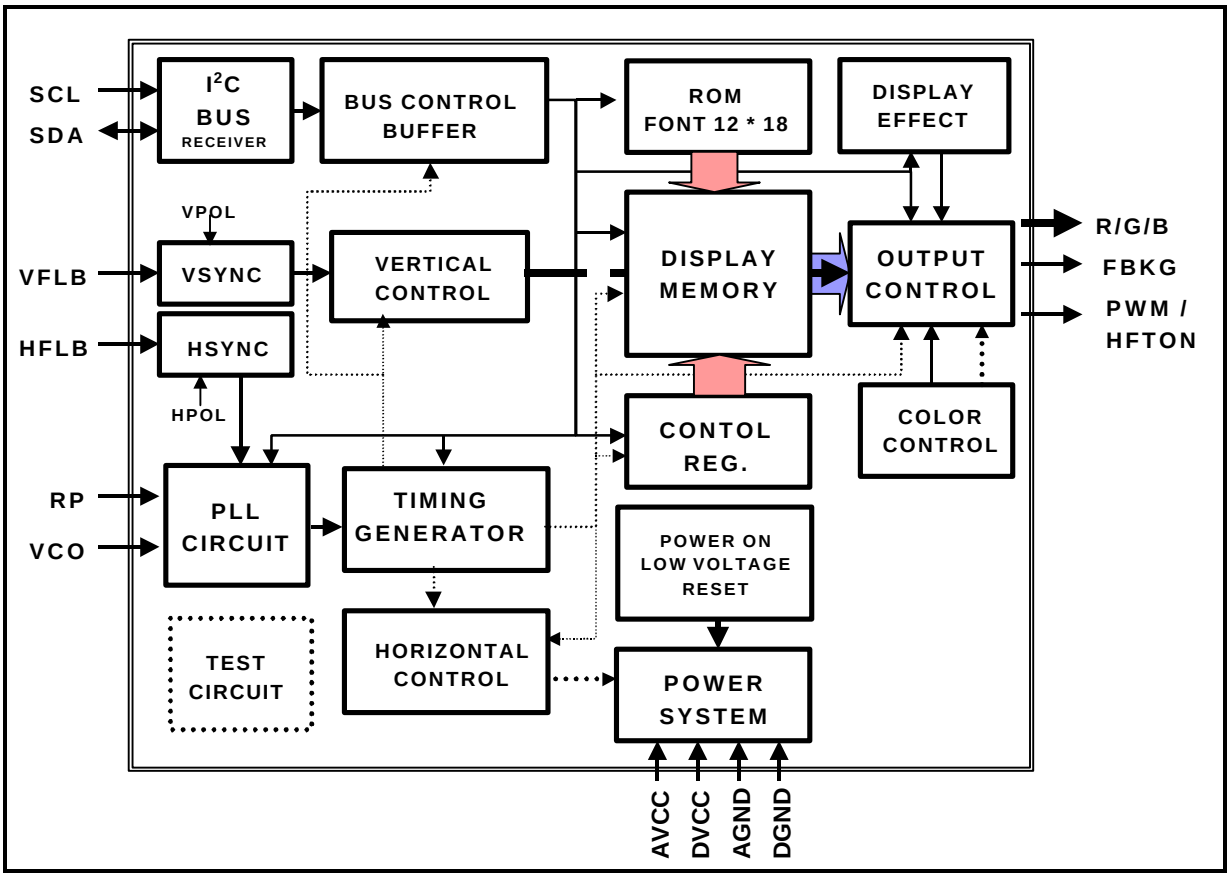
Features

- I²C Bus Interface with Slave Address $7A (Transmitter) & $7B (Receiver)
- Horizontal Frequency Range: 30KHz ~ 120KHz
- Flexible Display Resolution Up to 1524 Dots/Row
- Internal PLL Generates a Stable and Wide-Range System Clock (96MHz)
- OSD Screen Consists of Character Array of 15 Rows by 30 Columns
- Programmable Vertical and Horizontal Positions for OSD Display Center
- Total of 272 ROM Fonts Including 256 standard & 16 Multi-color ROM Fonts.
- 12 X 18 Dot Matrix Per Character
- 8-Color Selection for Each Character
- 7-Color Selection for Each Character Background
- Character/Symbol Blinking, Shadowing & Bordering Display Effect
- Double Character Height and Width for Each Row
- Programmable Height for Character/Symbol Displaying
- Row To Row Spacing Control to Avoid Expansion Distortion
- Four Programmable Windows with Overlapping Capability and Shadowing Effect
- Color Setting for Windows' Background and Characters' Shadowing & Bordering
- Fade-In/Out Effect of OSD Screen Display
- Selectable Hsync & Vsync Input Polarity

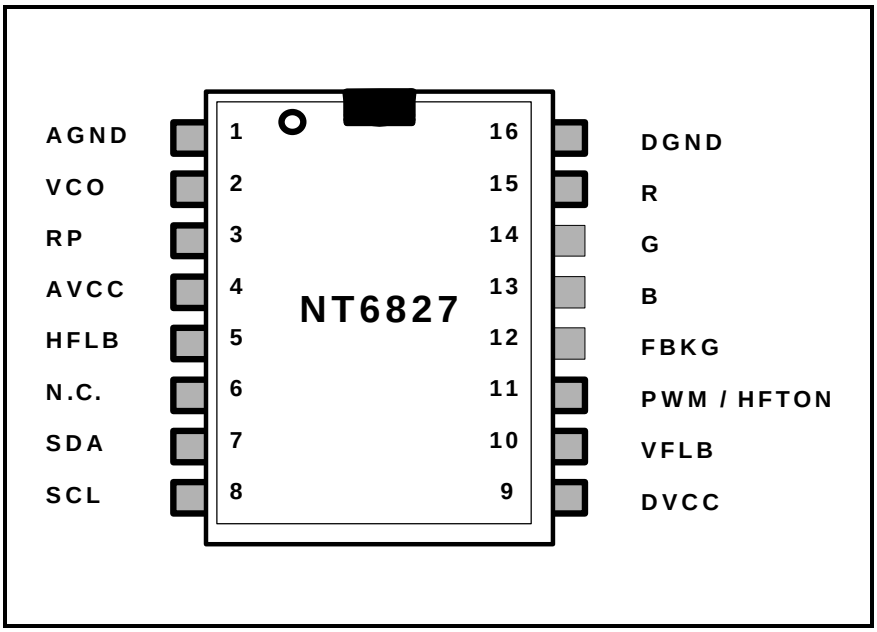
General Description

NT6827 is designed for displaying symbols and characters onto a CRT monitor. Its operation is controlled by a micro-controller with an I²C bus interface. By sending proper data and commands to NT6827, it can carry out the full screen display automatically with the time base being generated by an on-chip PLL circuit. There are many functions provided by this chip to fully support the user applications, such as: adjustment of the OSD windows position, built-in 256 ROM & 16 Multi-color fonts, variable character height with row-to-row spacing adjustment, 8 color selections & 7 background color controls for each character, double height/width controls for each row, 4 overlapping windows available with color & size controls, size controls for each window shadowing, color selection for windows' shadowing & characters' shadowing/ bordering and fade-in/out display effect ,etc.

Block Diagram



Pin Assignment



Pin Description

NT6827	Name	I/O/P/R	Function
1	AGND	P	Analog Ground
2	VCO	-	Voltage I/P to Control Oscillator
3	RP	-	Bias Resistor. It is used to bias internal VCO to resonate at the specific dot frequency.
4	AVCC	P	Analog Power Supply (5V Typ)
5	HFLB	I	Horizontal Fly-back Input (Schmitt Trigger Buffer)
6	N.C.	-	-
7	SDA	I	SDA Pin Of I^2C Bus (Schmitt Trigger Buffer) with internal 100K ohm pulled-high resistance
8	SCL	I	SCL Pin Of I^2C Bus (Schmitt Trigger Buffer) with internal 100K ohm pulled-high resistance
9	DVCC	P	Digital Power Supply (5V Typ)
10	VFLB	I	Vertical Fly-back Input (Schmitt Trigger Buffer)
11	PWM/ HFTON	O	PWM output or gain controller of R, G, B channels.
12	FBKG	O	Fast Blanking Output. It is used to cut off the external R, G, B signals.
13	B	O	Blue Color Output with Push-Pull Output Structure
14	G	O	Green Color Output with Push-Pull Output Structure
15	R	O	Red Color Output with Push-Pull Output Structure
16	DGND	P	Digital Ground

DC/AC Absolute Maximum Ratings*

Recommended Operation Conditions

VCC (measured to GND) . . . . . 4.75V to 5.25V

Operating Temperature . . . . . 0 to +70 ^{0}C

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these, or under any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics (VDD = 5V, Tamb = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
VCC	Supply Voltage	4.75	5	5.25	V	-

DC Characteristic

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
I_{DD}	Operating Current	-	22	25	mA	No loading
VIH1	Input High Voltage	2	-	-	V	VFLB, HFLB with Schmitt Trigger Buffer
VIL1	Input Low Voltage	-	-	0.8	V	VFLB, HFLB Schmitt Trigger Buffer
VIH2	IIC Bus Input High Voltage	3	-	-	V	SCL, SDA
VIL2	IIC Bus Input Low Voltage	-	-	1.5	V	
Idrive1	Driving current of R, G, B, FBKG, HFTON output pins at 2.4V output voltage	80	-	-	mA	-
Isink1	Sinking current of R, G, B, FBKG, HFTON output pins at 0.4V output voltage	20	-	-	mA	-
Ileak	Leakage current of R, G, B, FBKG pins at Hi-Z state	-	-	10	uA	Measured at 2.5V state
Iiicl	IIC Bus Output Sink Current	-	5	-	mA	Viicoutl = 0.4V
Vth	Input Threshold Voltage at HFLB & VFLB pin	1.8	2.0	2.2	V	-
VSTIH	Schmitt Trigger Input High Voltage		1.7	2	V	-
VSTIL	Schmitt Trigger Input Low Voltage	0.8	1.1	-	V	-
Iin	Input Current of Hsync, Vsync, SDA, SCL pins	-10	-	+10	uA	Schmitt Trigger Buffer

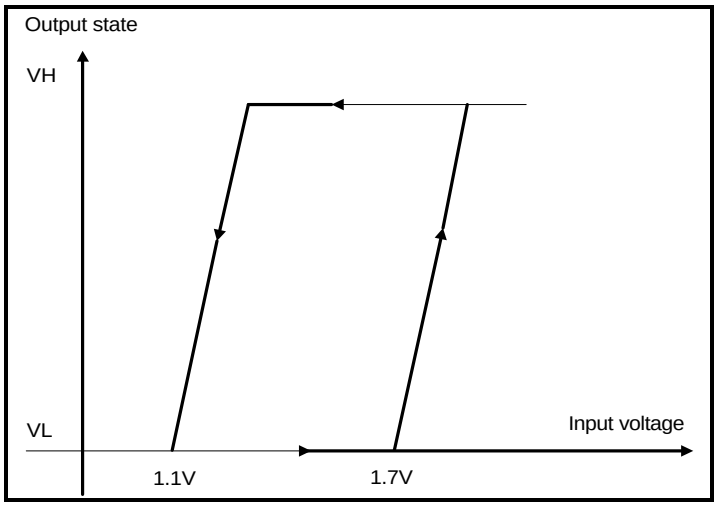


Figure 1. Schmitt Trigger Diagram

AC Characteristic

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Fhfy	Horizontal Fly-back Frequency	30	-	120	KHz	-
Vhfly	Horizontal Fly-back Input	-	-	5	V	-
		0	-	-	V	-
Thflymin	Minimum Pulse Width of Horizontal Fly-back	0.7	-	-	us	-
Thflymax	Maximum Pulse Width of Horizontal Fly-back	-	-	5.5	us	-
Fvfy	Vertical Fly-back Frequency	50	-	200	Hz	-
Vvfly	Vertical Fly-back Input	-	-	5	V	-
		0	-	-	V	-
Tvflymin	Minimum Pulse Width of Vertical Fly-back	20	-	-	us	-
Tvflymax	Maximum Pulse Width of Vertical Fly-back	-	-	1	ms	-

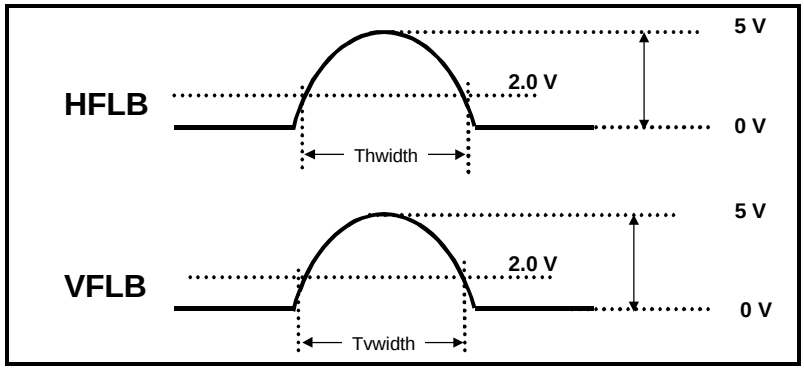


Figure 2. H/V Fly-Back Signal

I²C Bus– Slave Transmitter & Receiver (Slave address: $7A & $7B)

Table 1. I²C Bus

Symbol	Parameter	Min.	Typ.	Max.	Unit	Notes
Fmaxcl	Maximum SCL Clock Frequency			100	KHz	
VIL	Input Low Voltage	-0.5		1.5	V	
VIH	Input High Voltage	3.0		5.5	V	
Tlow	Low Period of the SCL Clock	4.7			us	SCL, SDA
Thigh	High Period of the SCL Clock	4.0			us	
Tsudat	Data Setup Time	250			ns	
Thddat	Data Hold Time	300			ns	
Tiicr	Rising Time of IIC Bus			1000	ns	
Tiicf	Falling Time of IIC Bus			300	ns	
Tsusta	Setup Time for Repeated START Condition	1.3			us	
Thdsta	Hold Time for START Condition	4.0			us	
Tsusta	Setup Time for START Condition	4.7			us	
Tsusto	Setup Time for STOP Condition	4.0			us	
Tiicbuf	Time the IIC bus must be free before the next new transmission can start	4.7			us	
Iiicl	IIC Bus Sink Current	4	5		mA	Viicoutl = 0.4 V
Tfilter	Input filter spike suppression			100	ns	SCL, SDA

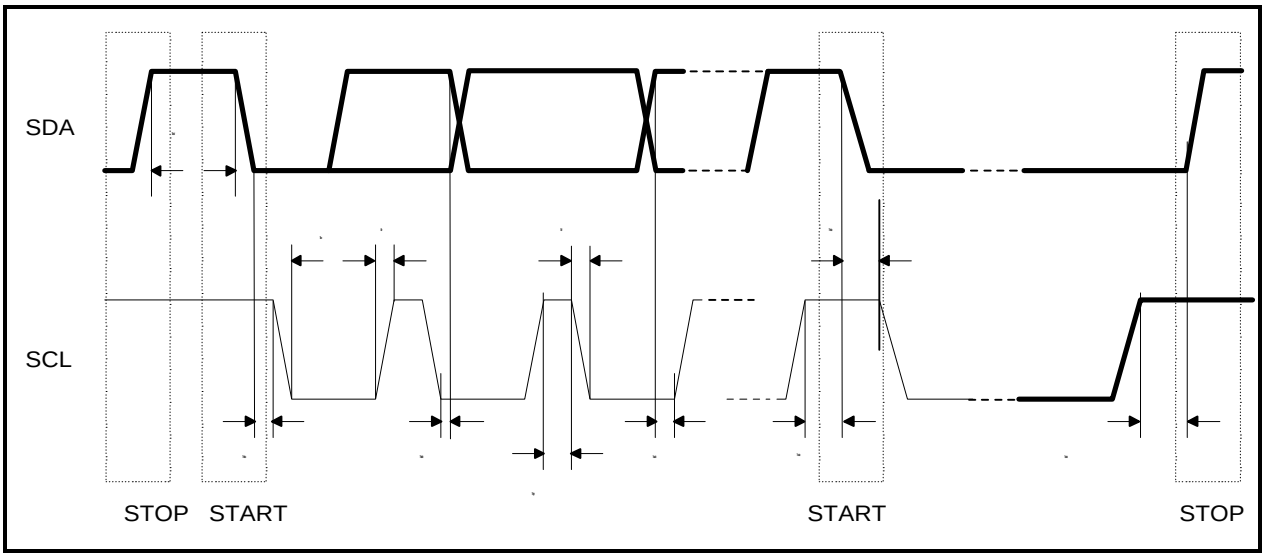


Figure 3. I²C Bus Timing

Memory Map

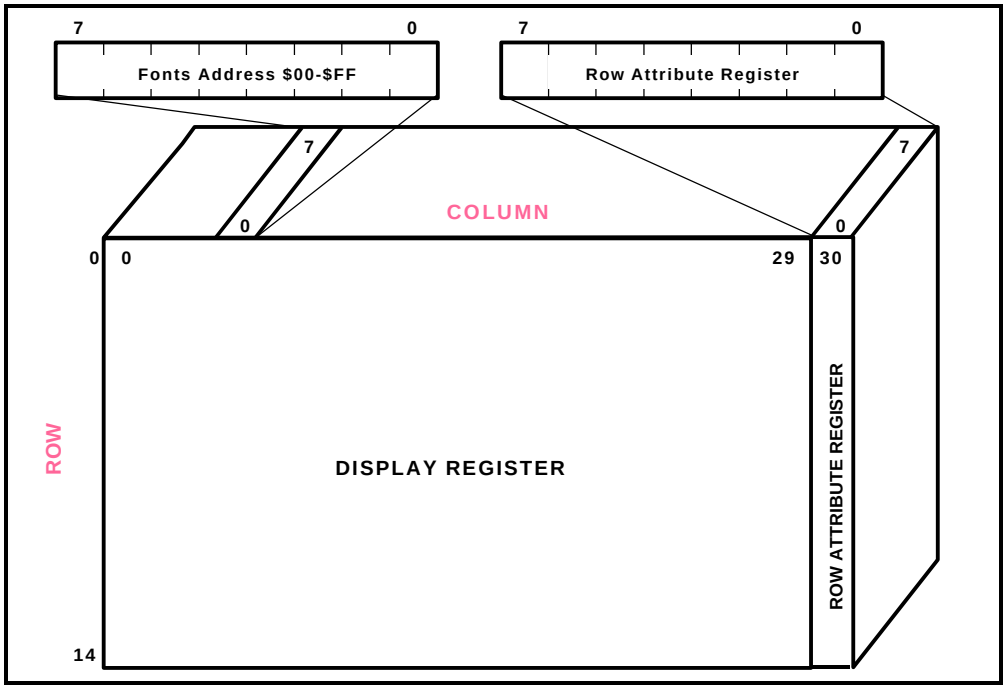


Figure 4. Memory Map of Display Register (Row 0 - 14)

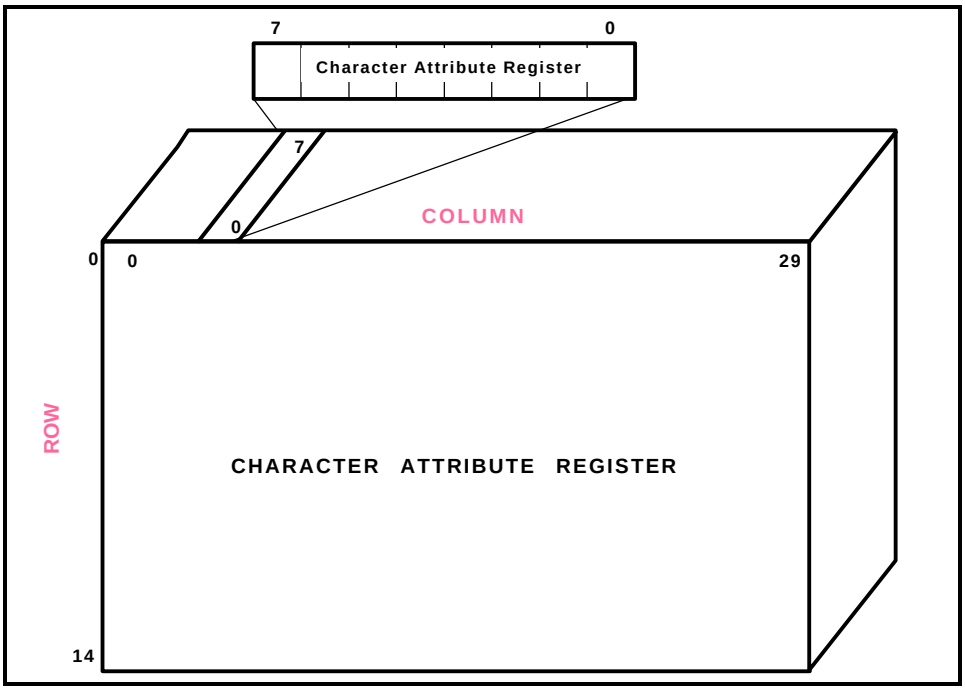


Figure 5. Memory Map of Attribute Register (Row 0 - 14)

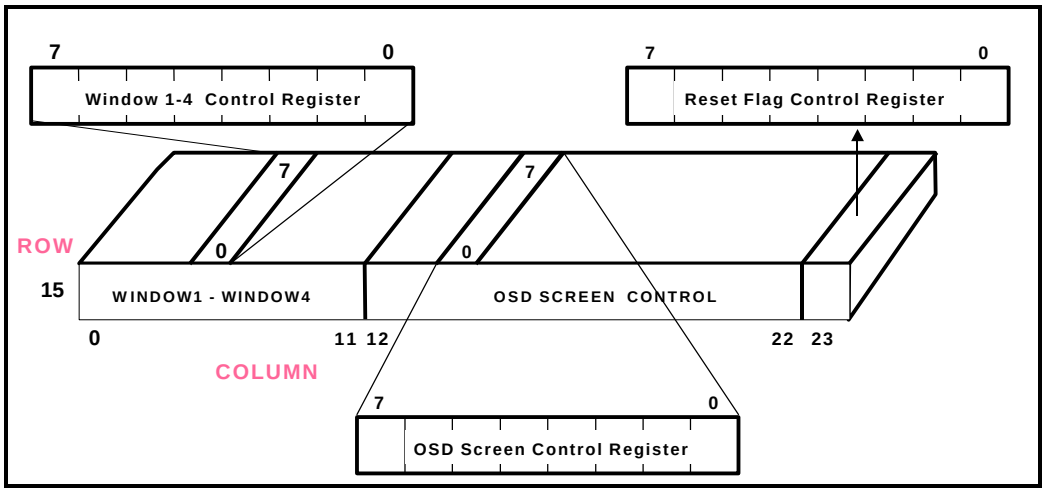


Figure 6. Memory Map of Control Register (Row 15)

List of Control Registers:

(1) Display Register: Row 0 - 14, Column 0 - 29

Row 0 - 14
Column 0 - 29

7	6	5	4	3	2	1	0
MSB							LSB

Font's Address $00 - $FF

Bit 7 - 0: These eight bits address one of the 256 characters/symbols residing in the character ROM fonts.

Note that if the user clear the MCFONT bit (row 15, column 20) to '0', the 0 ~ 255 will address the standard ROM fonts, and if sets this bit to "1", the 0 ~ 239 will address the standard ROM fonts & the 240 ~ 255 will address the multi-color ROM fonts.

(2) Character Attribute Register: Row 0 - 14, Column 0 - 29

Row 0 - 14
Column 0 - 29

7	6	5	4	3	2	1	0
	BKR	BKG	BKB	BLNK	R	G	B

Character's Attribute Control

Bit 6 - 4: BKR/G/B- These three bits define the color attributes of the background for the corresponding haracter/symbol. If all three bits are cleared, no background will be displayed. Refer to the Table 8 for the color selections.

Bit 3: BLNK - This bit enables the blinking effect of the corresponding character/symbol when set to '1'. The blinking frequency is approximately 1Hz with a fifty-fifty duty cycle at 80Hz vertical sync frequency.

Bit 2 - 0: R/G/B -These three bits define the color attributes of the corresponding character/symbol. Refer to the Table 7 for the color selections.

Table 7. Character/Windows Color Selection

COLOR	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

Table 8. Character/Windows' Background Color Selection

COLOR	R	G	B
No Background	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

(3) Row Attribute Register: Row 0 - 14, Column 30

Row 0 - 14, Column 30	7	6	5	4	3	2	1	0
							DBH	DBW

Row's Attribute Control

Bit 1: DBH- This bit controls the height of the displayed character/symbol. When this bit is set, the character/symbol is displayed in double height.

Bit 0: DBW- This bit controls the width of the displayed character/symbol. When this bit is set, the character/symbol is displayed in double width.

(4) Window 1 Registers: Row 15, Column 0

Row 15, Column 0	7	6	5	4	3	2	1	0
	Row Start Address				Row End Address			
	MSB			LSB	MSB			LSB

Window 1 Row Size Control

Bit 7 - 4: These bits determine the row start position of window 1on the 15*30 OSD screen.

Bit 3 - 0: These bits determine the row end position of window 1on the 15*30 OSD screen.

Row 15, Column 1	7	6	5	4	3	2	1	0
	Column Start Address					WINEN		SHAD
	MSB				LSB			

Window1 Column Size Control & Attribute Control

Bit 7-3: These bits determine the column start position of window 1on the 15*30 OSD screen.

Bit 2: WINEN - This bit enables window 1 when it is set. The default value of it is '0' after power on.

Bit 0: SHAD - This bit enables the shadowing on the window when it is set to '1'. The default value of it is '0' after power on.

Row 15, Column 2	7	6	5	4	3	2	1	0
	Column End Address					R	G	B
	MSB				LSB			

Window1 Column Size Control & Attribute Control

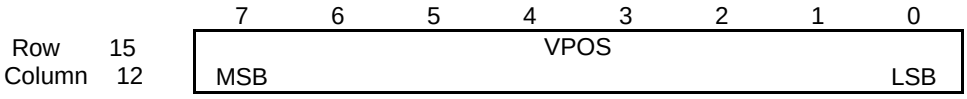
Bit 7 - 3: These bits determine the column end position of window 1on the 15*30 OSD screen.

Bit 2 - 0: R/G/B - These bits control the background color of window 1. Refer to Table 7 for color selection.

Note: Window 1 control registers occupy column 0 - 2 of row 15, Window 2 from column 3 - 5, Window 3 from 6 - 8 and Window 4 from 9 - 11. The function of Window 2 - 4 control registers is the same as Window 1. Window 1 has the highest priority, and Window 4 the least. The higher priority color will take over on the overlapped window area.

If the start address of the row/column is greater than the end address, this window will not be displayed. An out of range setting (over the 15 row or 30 column range) will cause abnormal operation.

(5) OSD Screen Position Control Registers: Row 15, Column 12 - 13

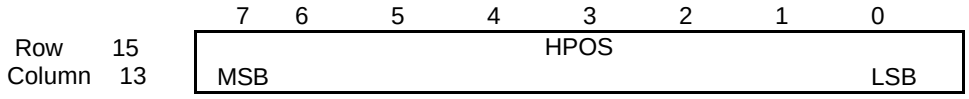


Vertical Position Adjustment

Bit 7 - 0: VPOS - These bits determine the vertical starting position for the character display. It is the vertical delay starting from the leading edge of VFLB. The unit of this setting is 4 horizontal lines and the equation is defined as below:

Vertical delay = (Vpos * 4 +1) * Horizontal line

The default value of it is 4 ($04) after power on.



Horizontal Position Adjustment

Bit 7 - 0: HPOS - These bits determine the horizontal starting position for the character display. It is the horizontal delay starting from the leading edge of HFLB. The unit of this setting is 6 dots movement shift to right on the monitor screen and the equation is defined as below:

Horizontal delay = (Hpos * 6 + 49) / P.R.

where the P.R. (pixel rate) is defined by the HDR & Horizontal Frequency.

P.R. (Pixel Rate) = HDR * 12 * $Freq_{HFLB}$

Refer to the HDR control register at row15 / column15 for the P.R. setting.
The default value of these bit is 15 ($ 0F) after power on.

(6) Character Height Control: Row 15, Column 14

Row 15
Column 14

7	6	5	4	3	2	1	0
	CRH6	CRH5	CRH4	CRH3	CRH2	CRH1	CRH0

Character's Height Control

Bit 6 - 0: CRH6 - CRH0 - These bits determine the displayed character height. The character, with an original 12 by 18 font matrix, can be expanded from 18 to 71 lines. Refer to the Table 9 below. All of these bits will be cleared to '0' after power on.

If the setting value of CH0 - CH6 is great than 17, then the algorithm will repeat at most 17 lines.

Table 9. Lines Expanded Control

CRH6 ~ CRH0	Lines Inserted
CRH6 = ' 1 ' , CRH5 = ' 1 '	All 18 lines repeat twice
CRH6 = ' 1 ' , CRH5 = ' 0 '	All 18 lines repeat once
CRH6 = ' 0 ' , CRH5 = ' X '	Repeat at most 17 lines
CRH4 = ' 1 '	Insert 16 lines
CRH3 = ' 1 '	Insert 8 lines
CRH2 = ' 1 '	Insert 4 lines
CRH1 = ' 1 '	Insert 2 lines
CRH0 = ' 1 '	Insert 1 line

Table 10. Lines Expanded Position

No. of Lines Inserted	Repeat Position																	
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Insert 1 line									!									
Insert 2 lines					!								!					
Insert 4 lines			!				!				!				!			
Insert 8 lines		!		!		!		!		!		!		!		!		
Insert 16 lines		!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	
Insert 17 lines	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	

(7) Flexible Display Control Register: Row 15, Column 15

	7	6	5	4	3	2	1	0
Row 15 Column 15		HDR						
		MSB						LSB

Horizontal Display Resolution Control

Bit 6 - 0: HDR - These bits determine the resolution of the horizontal display line. The unit of this setting is twelve dots (one character). With a total of 92 steps ($24 ~ $7F: 36 ~ 127 steps. Its value can't be smaller than 36 at anytime), the user can adjust the resolution from 36 to 127 characters on each horizontal line. Note that the resolution adjustment must be done in cooperation with the VCO setting at the row15/column18 control register. Refer to the Table 11 of the control register at row15/column18. The default value of it is 40 after power on.

(8) OSD Row to Row Space Control Register: Row 15, Column 16

	7	6	5	4	3	2	1	0
Row 15 Column 16				R2RSPACE				
				MSB				LSB

Row To Row Space Adjustment

Bit 4 - 0: R2RSPACE - These bits define the row to row spacing in the units of horizontal line. It means extra lines, defined by this 5-bit value, will be appended to each display row. The default value of it is '0' after power on and there are no extra lines inserted between the rows. All of these bits will be cleared to '0' after power on.

(9) Input/Output Control Register: Row 15, Column 17

	7	6	5	4	3	2	1	0
Row 15 Column 17	OSDEN	BSEN	SHADOW	FADE	BLANK	CLRWIN	CLRDSPR	FBKGC

OSD Screen Control 1

Bit 7: OSDEN - This bit will enable the OSD circuit when it is set to '1'. The default value is '0' after power on.

Bit 6: BSEN - This bit will enable the bordering and shadowing effect when it is set to '1'. The default value is '0' after power on.

Bit 5: SHADOW - When the BSEN is set to '1', it will enable the shadowing effect when this bit set to '1', too. Otherwise, it will enable the bordering effect when this bit is cleared to '0'. The default value is '0' after power on.

Bit 4: FADE - This bit enables the fade-in/out effect when the OSD screen is turned on by changing OSDEN from '0' to '1' or when turned off by changing OSDEN from '1' to '0'. The fade-in/out effect will be completed in about 0.5 seconds when the input Vsync is 60 Hz. The default value of this bit is '0' after power on.

Bit 3: BLANK - This bit will force the FBKG pin to output high when this bit & the FBKGOP bit is set to '1'. Otherwise, the FBKG pin will output low when this bit is set to '1' & the FBKGOP bit is set to '0'. The default value of this bit is '0' after power on.

Bit 2: CLRWIN - This bit will clear all windows' WINEN control bit when it is set to '1'. The default value of this bit is '0' after power on.

Bit 1: CLRDSPR - This bit will clear all of the contents in the display registers and the R, G, G, BLNK bits in the character attribute registers when it is set to '1'. The default value of this bit is '0' after power on.

Bit 0: FBKGC - It determines the configuration of the FBKG output pin. When it is cleared, the FBKG pin will output high when displaying characters or windows. Otherwise, it will output high only when displaying characters. The default value of this bit is '0' after power on.

		7	6	5	4	3	2	1	0
Row	15	RGBF	FBKGOP	PWMCTRL	DBOUNCE	HPOL	VPOL	VCO1	VCO0
Column	18								

OSD Screen Control 2

Bit 7: RGBF - This bit controls the driving state of the output pins, R, G, B and FBKG when the OSD is disabled. After power on, this bit is cleared to '0' and all of the R, G, B and FBKG pins output high impedance state while the OSD is being disabled. If this bit is set to '1', the R, G, B output pins will drive low and the FBKG pin will drive high or low depending on the FBKGOP (If FBKGOP=0, it will drive high. If FBKGOP=1, it will drive low) while the OSD is being disabled.

Bit 6: FBKGOP - This bit selects the polarity of the output signal of the FBKG pin. This signal is active low when the user clears this bit. Otherwise, active high, set this bits. Refer the Figure 7 below for the FBKG output timing. The default value is '1' after power on.

Bit 5: PWMCTRL - This bit selects the output option to the PWM/HFTON pin. This bit will enable the PWM output when it is set to '1'. Otherwise, it will select the HFTON option. Refer to the Figure 7 below for the HFTON output timing. The default value is '0' after power on.

Bit 4: DBOUNCE - This bit is to activate the debounce circuit of the horizontal and vertical scan. It is to prevent the OSD screen shaking when the user adjusts the horizontal phase or vertical position. This bit will be cleared after power on.

Bit 3: HPOL - This bit selects the polarity of the input signal of the horizontal sync (HFLB pin). If the input sync signal has negative polarity, the user must clear this bit. Otherwise, set this bit to '1' to accept the positive polarity signal. After power on, this bit is cleared to '0' and it will accept a negative polarity sync signal.

Bit 2: VPOL - This bit selects the polarity of the input signal of the vertical sync (VFLB pin). If the input sync signal has negative polarity, the user must clear this bit. Otherwise, set this bit to '1' to accept the positive polarity signal. After power on, this bit is cleared to '0' and it will accept a negative polarity sync signal.

Bit 1 - 0: VCO1/0 – These bits select the VCO frequency range when the user sets the horizontal display resolution flexibly. It is related to the horizontal display resolution and the user must set the control register at row15/column15 properly. The default value is VCO1 = 0 & VCO0 = 0 after power on state. The relationship between VCO1/0 and the display resolution is list below:

Table 11. P.R. (Pixel Rate) = HDR * 12 * $Freq_{HFLB}$

Section	VCO1	VCO0	VCO Freq. Min	VCO Freq. Max	Unit	P.R. Limit	HFLB Freq. Limit
Freq1	0	0	6	12	MHz	Min < P.R. < Max	(Min/HDR*12) < $Freq_{HFLB}$ < Max/(HDR*12)
Freq2	0	1	12	24			
Freq3	1	0	24	48			
Freq4	1	1	48	92.2			

If there is no signal at HFLB input, the PLL will generate an approximate 2.5 MHz clock to ensure the proper operation of I^2C bus and other control registers.

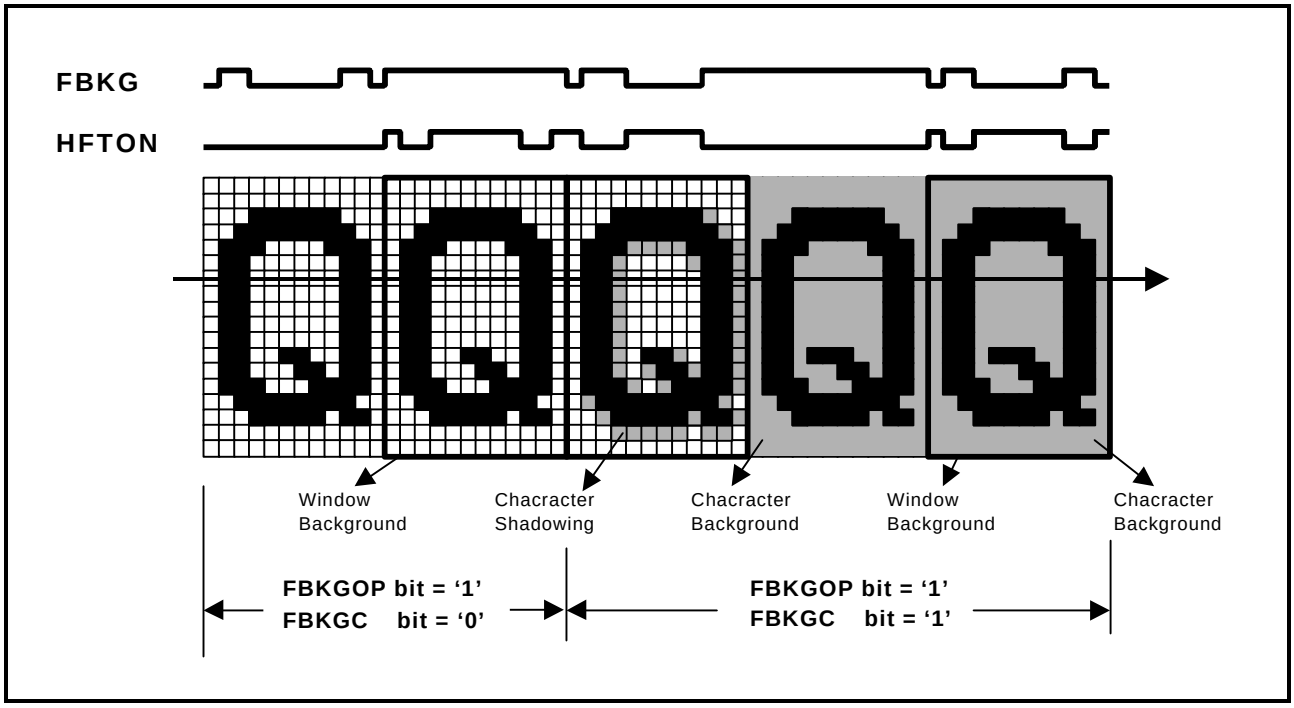


Figure 7. FGBK & HFTON Output Timing

(10) Color Selection for Shadowing/Bordering Effect: Row 15, Column 19

Row 15
Column 19

7	6	5	4	3	2	1	0
	WINR	WING	WINB		CHR	CHG	CHB

Shadowing/Bordering Color Control

Bit 6 - 4: WINR/G/B - These bits control the shadowing color of windows 1-4. Refer to the Table 12 for color selection. All of these bits will be cleared to '0' after power on.

Bit 2 - 0: CHR/G/B - These bits control the shadowing/bordering color of each character. Refer to the Table 12 for color selection. All of these bits will be cleared to '0' after power on.

Table 12. Character/Windows' Shadowing Color Selection

COLOR	R	G	B
Black	0	0	0
Blue	0	0	1
Green	0	1	0
Cyan	0	1	1
Red	1	0	0
Magenta	1	0	1
Yellow	1	1	0
White	1	1	1

(11) Multi-Color Fonts' Control: Row 15, Column 20

Row 15
Column 20

7	6	5	4	3	2	1	0
							MCFONT

Multi-Color Fonts Control

Bit 0: MCFONT - This bit will enable the multi-color fonts addressed from 240 to 255 when it is set to '1'. The default value is '0' after power on and enables the standard ROM fonts.

(12) Adjustments of Width & Height for Windows' Shadowing: Row 15, Column 21, 22

	7	6	5	4	3	2	1	0
Row 15 Column 21	W4WD1	W4WD0	W3WD1	W3WD0	W2WD1	W2WD0	W1WD1	W1WD0

Setting of Windows' Shadowing Width

WxWD1/0 - These bits will determine the size of the window's width when the SHAD bit of the windows control register (row 15 column 1, 4, 7, 10) is set to '1'. The default values are '0, 0 ' after power on. Refer to the Table 13 below for the size adjustments.

Table 13. Windows' Shadowing Width Control

WxWD1/0	(0 , 0)	(0 , 1)	(1 , 0)	(1 , 1)	Units
Windows' Shadowing Width	2	4	6	8	Pixels

	7	6	5	4	3	2	1	0
Row 15 Column 22	W4HT1	W4HT0	W3HT1	W3HT0	W2HT1	W2HT0	W1HT1	W1HT0

Setting of Windows' Shadowing Height

WxHT1/0 - These bits will determine the size of the window's height when the SHAD bit of the windows control register (row 15 column 1, 4, 7, 10) is set to '1'. The default values are '0' after power on. Refer to the Table 14 below for the size adjustments.

Table 14. Windows' Shadowing Height Control

WxHT1/0	(0 , 0)	(0 , 1)	(1 , 0)	(1 , 1)	Units
Windows' Shadowing Height	2	4	6	8	Pixels

(13) Reset Flag Control Registers

	7	6	5	4	3	2	1	0
Row 15 Column 23							RESETFLG	

Bit 1: RESTFLG - After system reset, the system will clear this bit. The user can set this bit at the beginning to check if this bit has been cleared by the system reset action.

This bit can be read back through the IIC bus by an external master device, for example, an MCU.

The other bits are reserved.

(14) Reserved Control Register:

	7	6	5	4	3	2	1	0
Row 15 Column 24	Reserved							

This control register is reserved and no data can be written into this register.

	7	6	5	4	3	2	1	0
Row 15 Column 31	Reserved							

This control register is reserved and no data can be written into this register.

IIC Bus Read Mode Operation ¡ G

Type	(1)	(2)	(3)	(16)
(a)	START Condition	OSD Slave Address '$7B'	Row15 Column 23 Data	STOP Condition
		8 bits	8 bits	

The user may read these bytes of data sequentially and check the reset flag on row 15 column 23. Every time the user sends the START condition and slave address $7B, the NT6827 will respond with an acknowledgement and then transmit the data. It is prohibited to read extra data more than 1 bytes of data.

I²C Bus Communication:

Figure 8 shows the I²C Bus transmission format. The master initiates a transmission routine by generating a START condition, followed by a slave address byte. Once the address is properly identified, the slave will respond with an ACKNOWLEDGEMENT (ACK) signal by pulling the SDA line LOW during the ninth SCL clock. Each data byte which then follows must be eight bits long, plus the ACK bit, to make up nine bits together. This ACK bit is sent by NT6827 during WRITE mode operation and by the master, during READ mode. In WRITE mode, appropriate row and column address information and display data can be downloaded sequentially from the master in one of the three transmission formats, described in Figure 8 Access Register Operation. In READ mode, the content in some control registers can be transferred to the master. In the cases of no ACK or completion of the data transfer, the master will generate a STOP condition to terminate the transmission routine. Note that the OSD_EN bit must be set after all the display information has been sent in order to activate the displaying circuitry of NT6827, so that the received information can then be displayed.

Write Operation of the Control Registers:

After the proper identification by the receiving device, a data train of arbitrary length is transmitted from the master. There are three transmission formats from (a) to (c) as stated below timing. The data train in each sequence consists of a row address, a column address and data. In format (a), data must be preceded by the corresponding row address and column address. This format is particularly suitable for updating small amounts of data between different rows. However, if the current information byte has the same row address as the one before, format (b) is recommended. For a full screen pattern change which requires a massive information update, or during a power up situation, most of the row and column addresses in either (a) or (b) format will appear to be redundant. A more efficient data transmission format (c) should be applied. This sends the starting row and column addresses once only, and then treats all subsequent data as display information. The row and column addresses will be automatically incremented internally for each display information data from the starting location.

To differentiate the row and column addresses when transferring data from the master, the MSB (Most Significant Bit) is set as Table 15 Transmission: ‘1’ represents the row, with ‘0’ representing the column address. Furthermore, to distinguish the column address in formats (a), (b) and (c), the sixth bit of the column address is set to ‘1’, which represents format (c), and to ‘0’ for format (a) or (b). There is some limitation on using mixed formats during a single transmission. It is permissible to change the format from (a) to (b), or from (a) to (c), or from (b) to (a), but not from (c) back to (a) or (b).

I²C Bus Write Operation Timing:

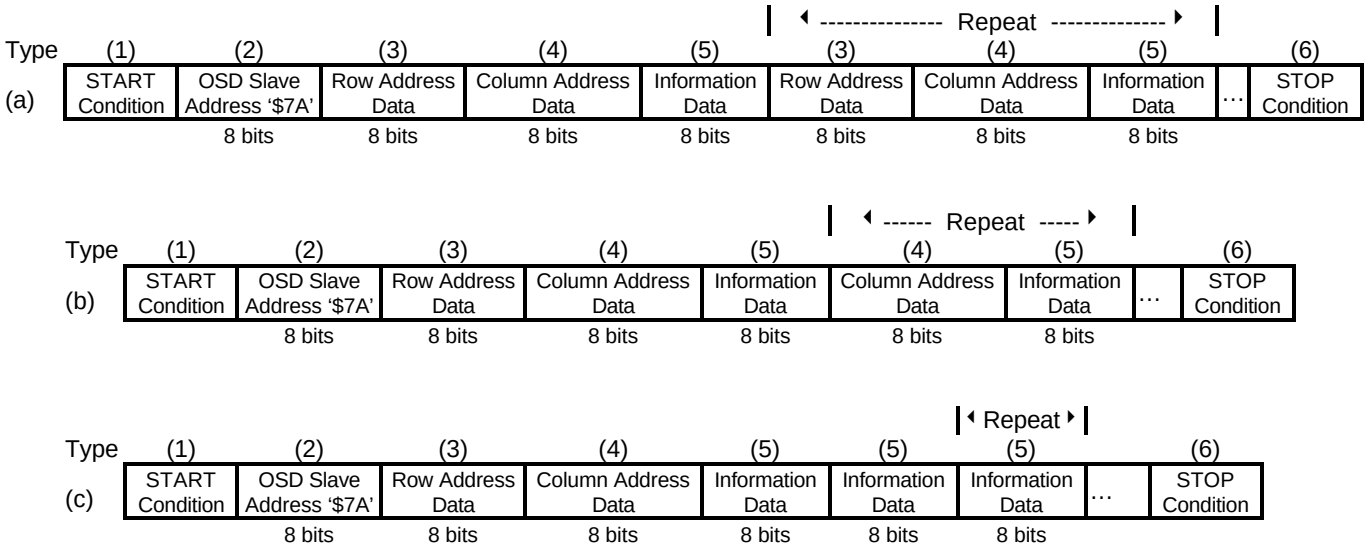


Figure 8. Access Register Read Operation

Table 15. Address Data Transmission for Registers

ITEM	No	ADDRESS	B7	B6	B5	B4	B3	B2	B1	B0	Type
Display Register	1	Row	1	0	0	X	D	D	D	D	(a),(b),(c)
	2	Column	0	0	X	D	D	D	D	D	(a),(b)
	3	Column	0	1	X	D	D	D	D	D	(c)
Attribute / Control Register	4	Row	1	0	1	X	D	D	D	D	(a),(b),(c)
	5	Column	0	0	X	D	D	D	D	D	(a),(b)
	6	Column	0	1	X	D	D	D	D	D	(c)

Read Operation of the Control Registers:

Not all of the control registers can be read by the master via IIC bus of the READ mode. Below is listed the proper identification of the slave address ($7B) by the NT6827, One byte of data is transmitted to the master. The user only checks bit1 of this byte transmission data. (the reset flag on row 15 column 23),

Item	Register	Bytes
1	Row 15 Column 23 Control Register	1

I²C Bus Read Operation Timing:

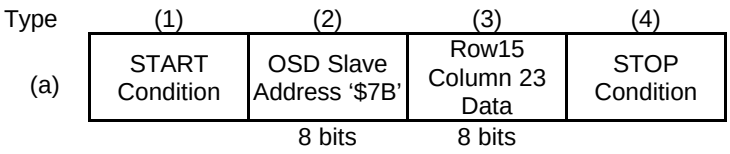


Figure 9: Access Register Write Operation

The user may read these bytes of data and check the reset flag on row 15 column 23. Every time the user sends the START condition and the slave address $7B, the NT6827 will respond with an acknowledgement and then transmit data. It is prohibited to read extra data more than 1 bytes of data.

Font Access

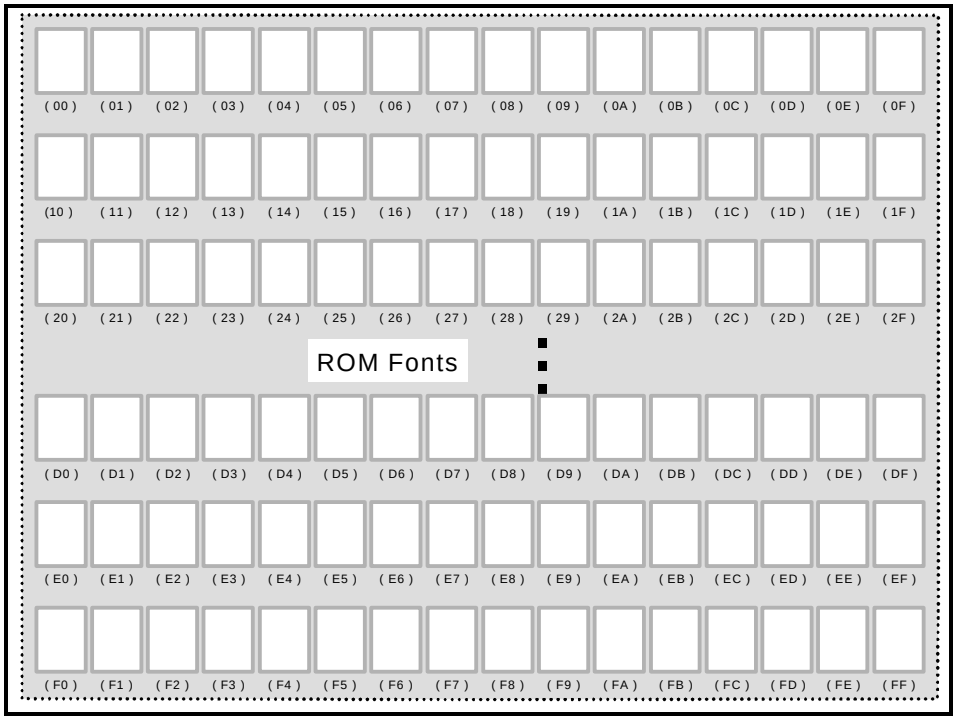


Figure 10. 256 Standard ROM FONT Configuration

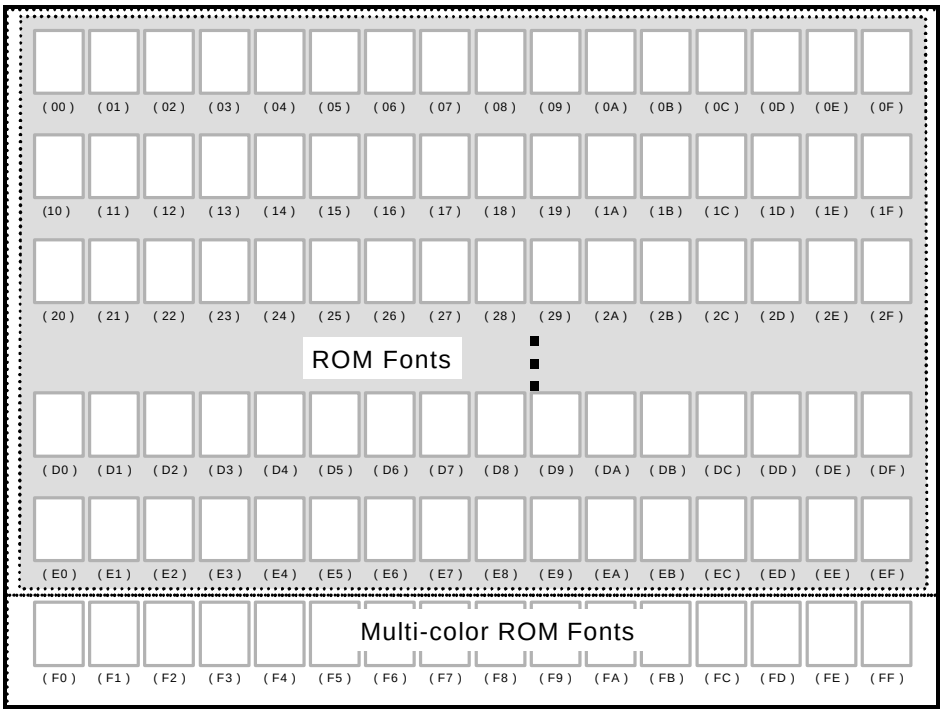


Figure 11. 240 Standard ROM FONT Configuration & 16 Multi-color ROM FONT

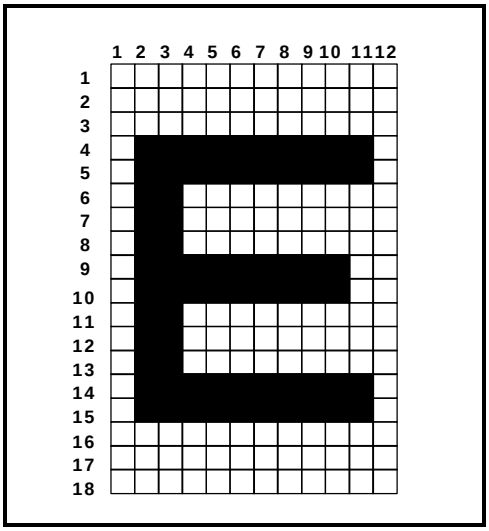


Figure 12. 12 X 18 Dots Font

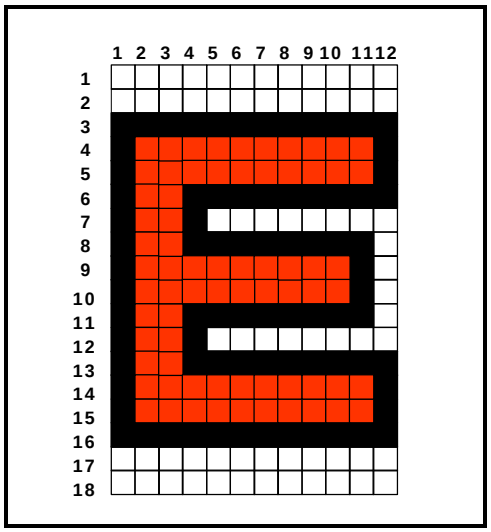


Figure 13. Bordering Effect

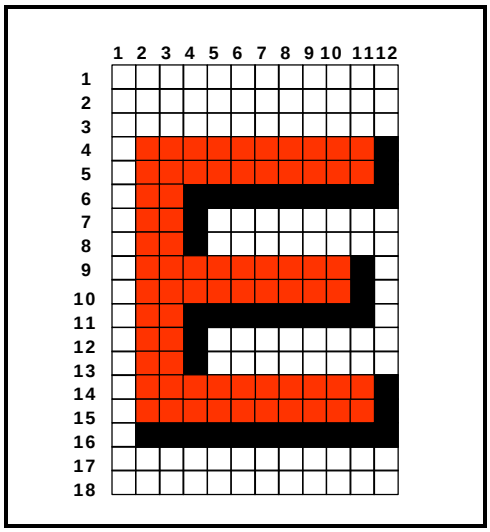


Figure 14. Shadowing Effect

OSD Screen Position:

Figure, below, illustrates the positions of all display characters on the screen relative to the leading edge of the horizontal and vertical fly-back signals.

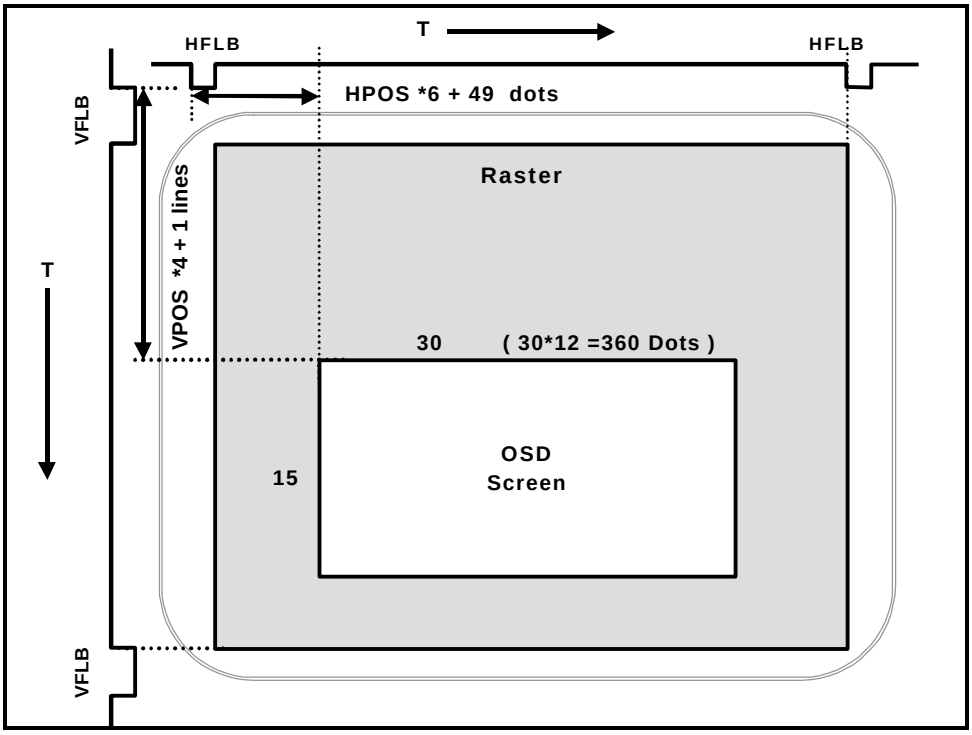


Figure 15. OSD Screen Position

OSD Display Format:

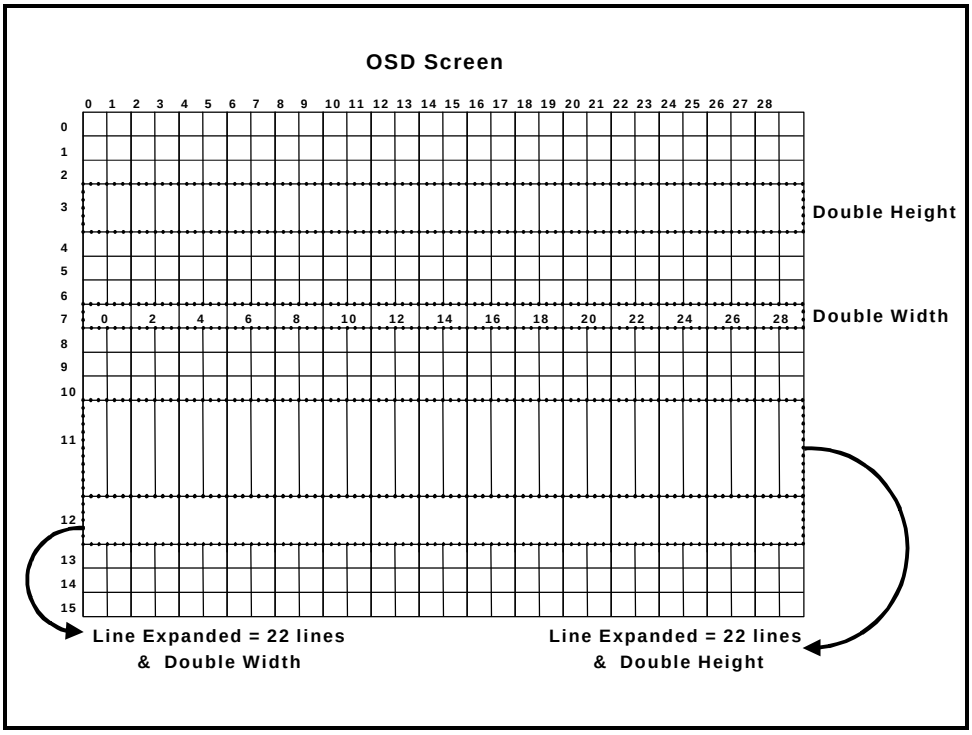


Figure 16. OSD Display Format

OSD Window Setting:

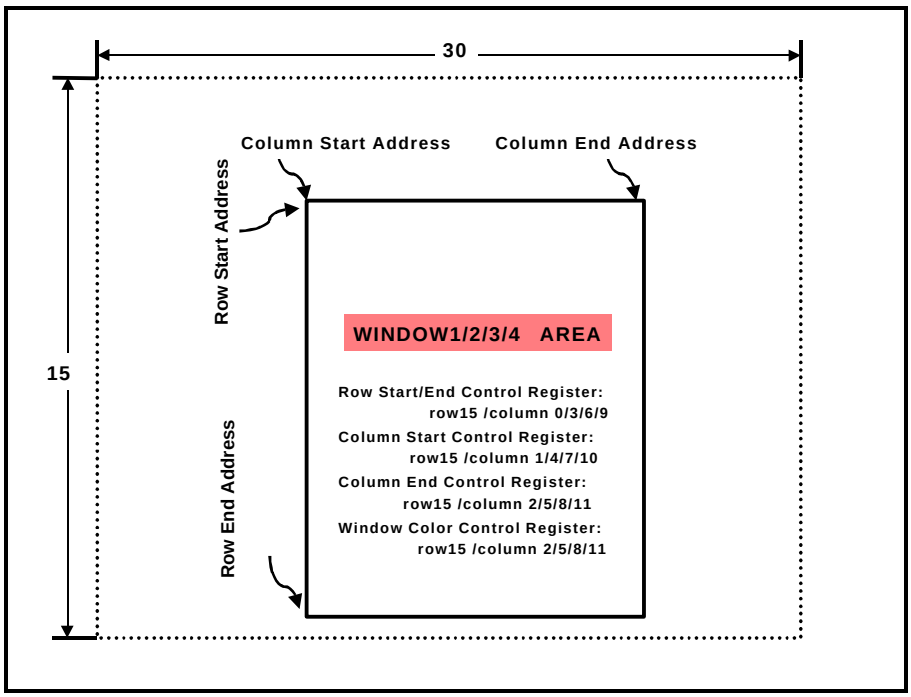


Figure 17. Windows' Size Setting

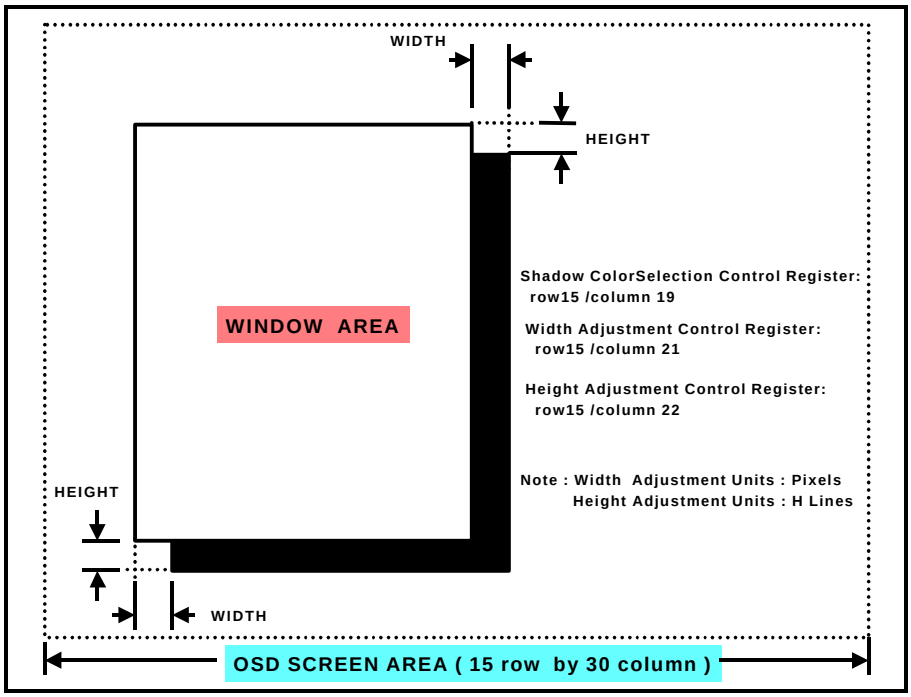


Figure 18. Windows' Shadowing Setting

Characters' Programmable Height:

Table 16. Line Expanded

Example 1: If user sets CRH0 = 1, CRH2 = 1, CRH3 = 1

Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Original Font	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!
CRH0									!									
CRH2			!				!				!				!			
CRH3		!		!		!		!		!		!		!		!		
CH4 – CH 0 <= 18		!	!	!		!	!	!	!	!	!	!		!	!	!		
Result : 31 lines 18+ 8*CRH3+4*CRH2 +CRH0	!	!!	!!	!!	!	!!	!!	!!	!!	!!	!!	!!	!	!!	!!	!!	!	!

Example 2: If user sets CRH0 = 1, CRH 3 = 1, CRH4 = 1

Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Original Font	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!
CRH0									!									
CRH3		!		!		!		!		!		!		!		!		
CRH4		!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	
CH4 – CH 0 >= 18	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	
Result : 35 lines 18+17	!!	!!	!!	!!	!!	!!	!!	!!	!!	!!	!!	!!	!!	!!	!!	!!	!!	!

Example 3: If user sets CRH1 = 1, CRH3 = 1, CH5 = 0, CH6 = 1

Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
Original Font	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!
CRH1					!								!					
CRH3		!		!		!		!		!		!		!		!		
CH4 – CH0 < 18		!		!	!	!		!		!		!	!	!		!		
CRH6,5=(1,0)	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!	!
Result : 46 lines 18+(8 * CRH3) + (2*CRH1)+ 18 * 1	!!	!!!	!!	!!!	!!!	!!!	!!	!!!	!!	!!!	!!	!!!	!!!	!!!	!!	!!!	!!	!!

Multi-color Font Operation:

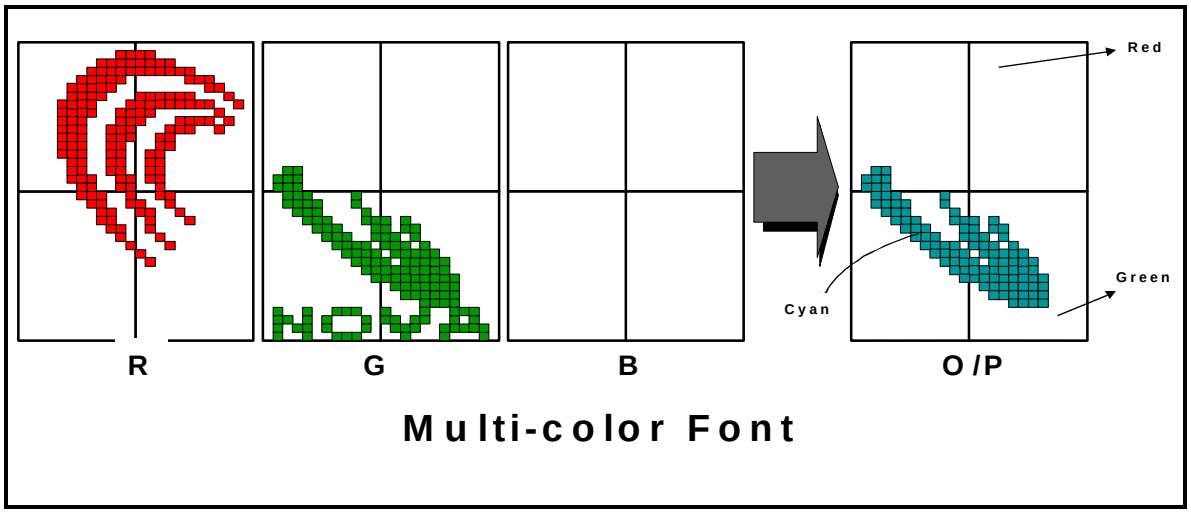


Figure 19. Multi-Color Font Operation

In the example above, the NOVATEK logo consists of four fonts. The R, G, B output channels will send out their corresponding font data and it can then display multiple colors in the same font.

Reminder: when using the multi-color font, it can not be set to black color and the bordering and shadowing options are not available.

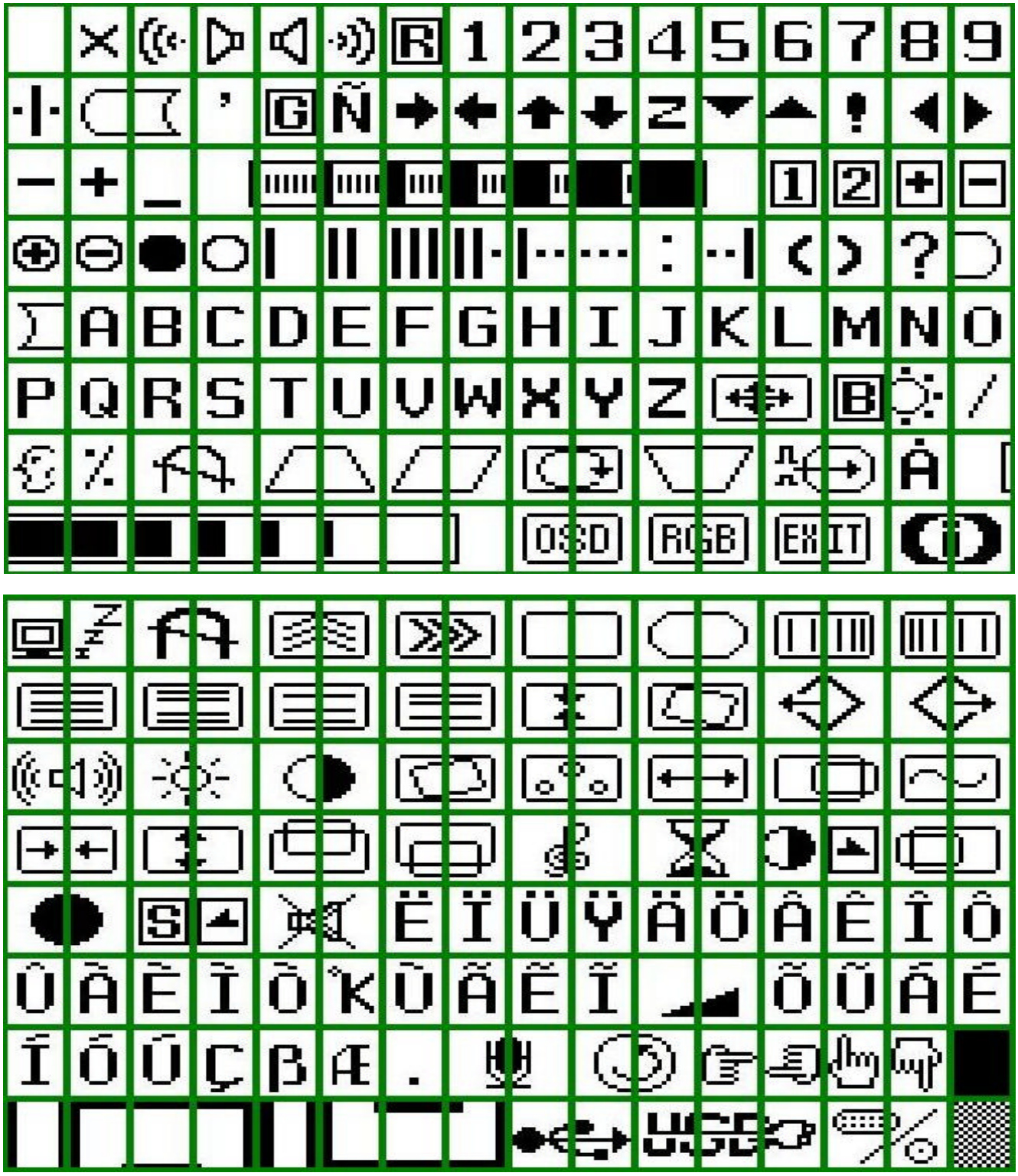


Figure 20. Font Code Example NT6827 - 00012

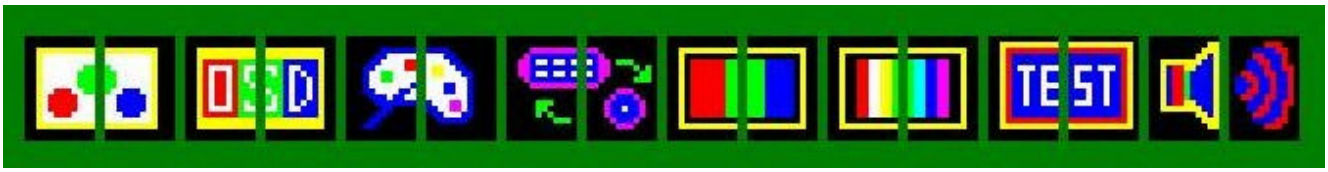
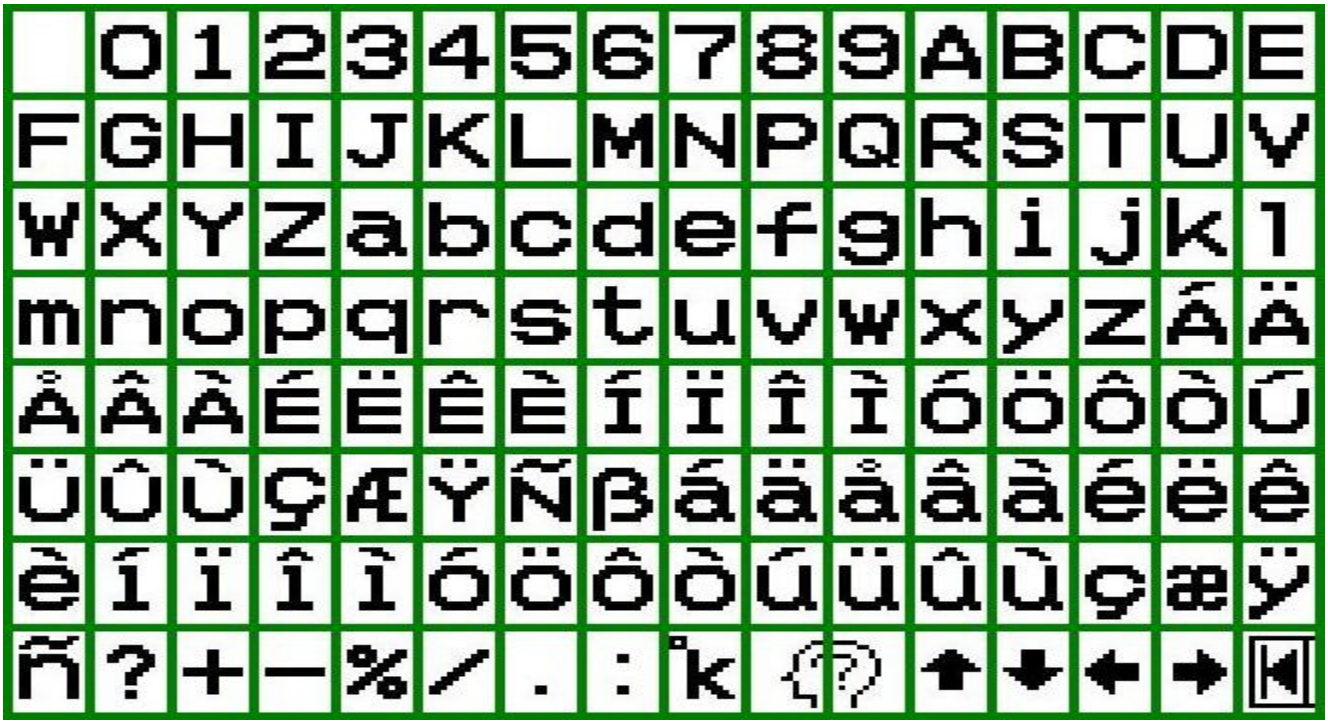


Figure 21. Font Code Example NT6827-00012 (Multi Color Fonts)



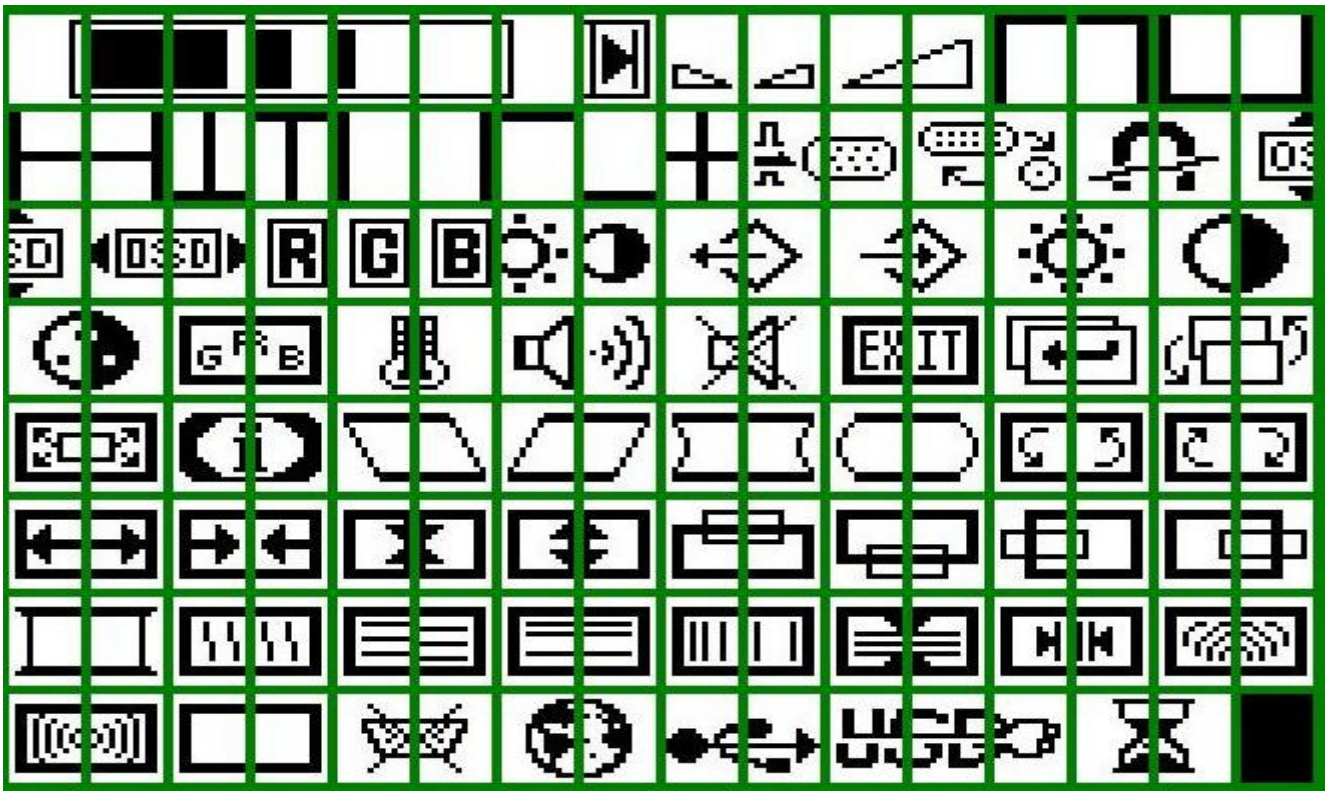


Figure 22. Font Code Example NT6827-00013

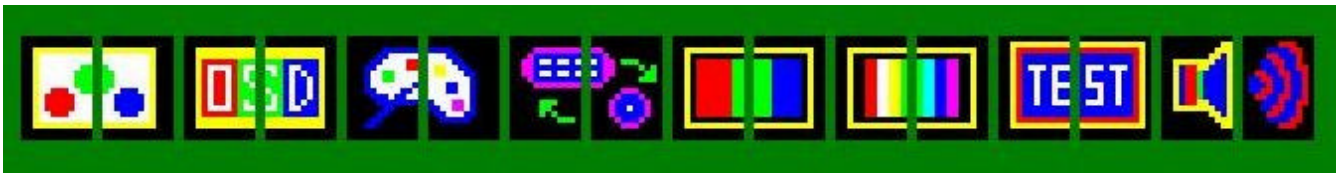
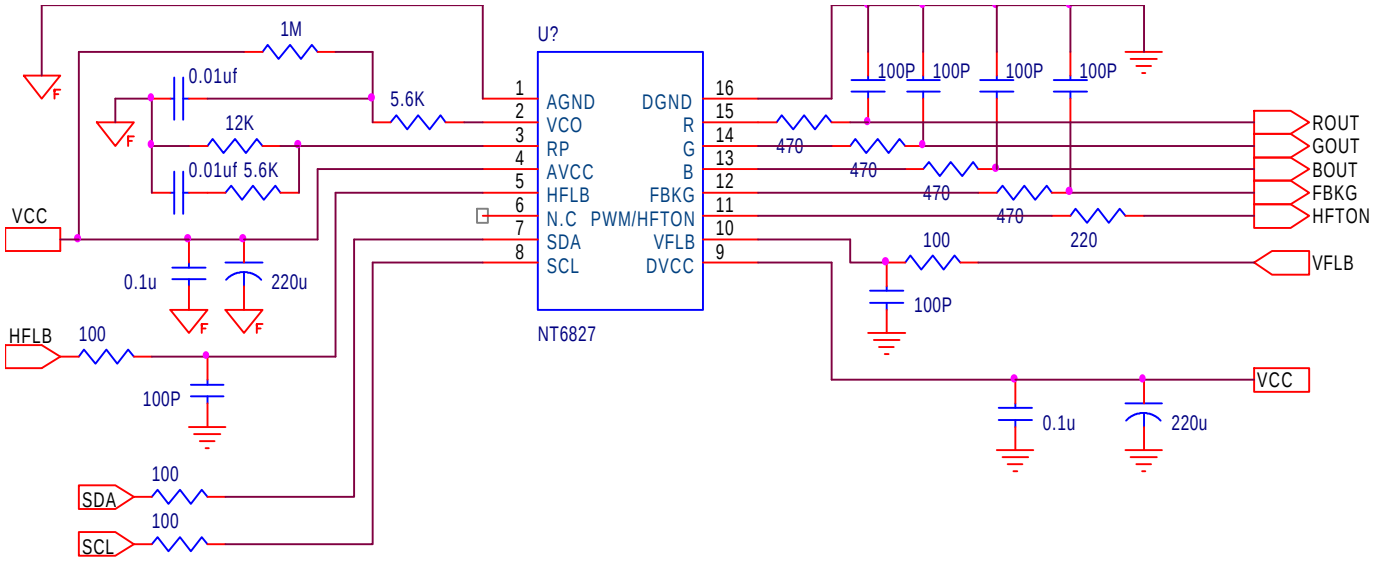


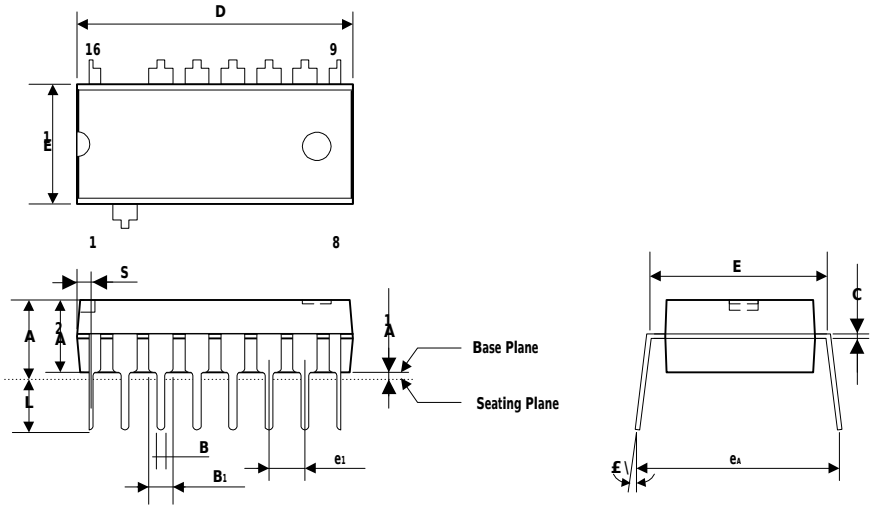
Figure 23. Font Code Example NT6827-00013 (Multi Color Fonts)

Application Circuit



Package Information

P-DIP 16L Outline Dimensions **unit: inches/mm**



Symbol	Dimension in inch	Dimension in mm
A	0.175 Max.	4.45 Max.
A_1	0.010 Min.	0.25 Min.
A_2	0.130±0.010	3.30±0.25
B	0.018 +0.004 -0.002	0.46 +0.10 -0.05
B_1	0.060 +0.004 -0.002	1.52 +0.10 -0.05
C	0.010 +0.004 -0.002	0.25 +0.10 -0.05
D	0.750 Typ. (0.770 Max.)	19.05 Typ. (19.56 Max.)
E	0.300±0.010	7.62±0.25
E_1	0.250 Typ. (0.262 Max.)	6.35 Typ. (6.65 Max.)
e_1	0.100±0.010	2.54±0.25
L	0.130±0.010	3.30±0.25
£ \	0°~ 15°	0°~ 15°
e_A	0.345±0.035	8.76±0.89
S	0.040 Max.	1.02 Max.

Note:
1. The maximum value of dimension D includes end flash.
2. Dimension E1 does not include resin fins.
3. Dimension S includes end flash.