KL5KUSB102

"One Chip"- USB to Ethernet Controller

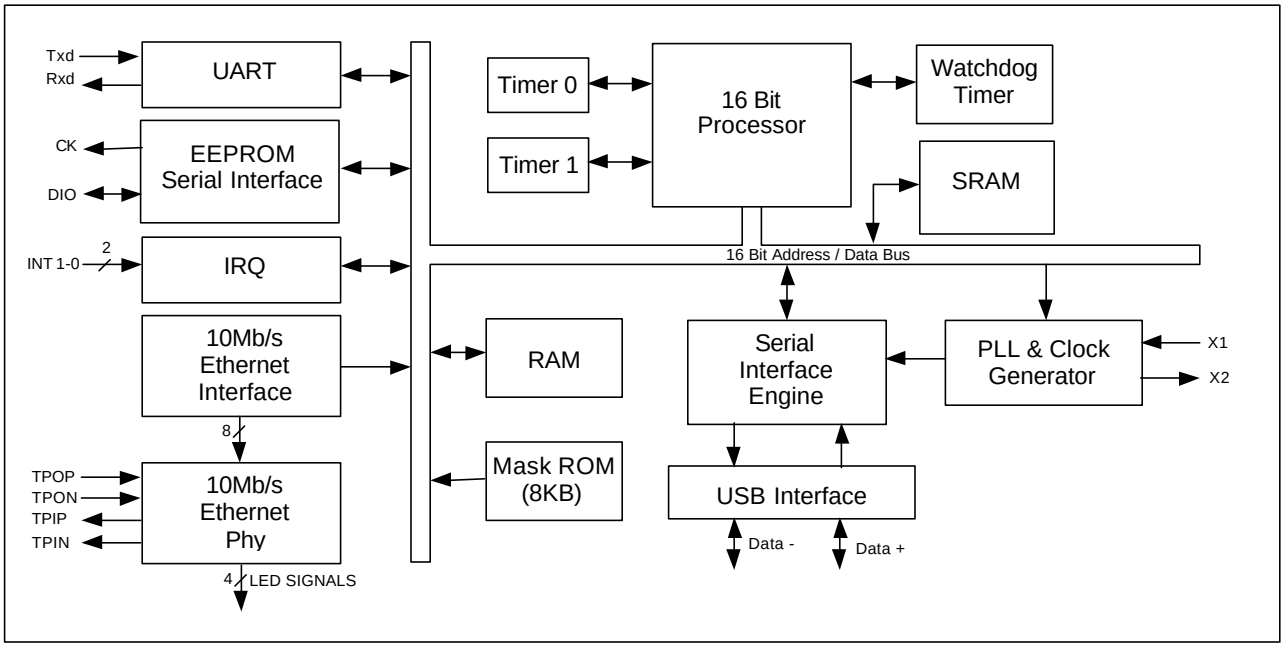
General Description

The KL5KUSB102 design provides the smallest available solution for connectivity between USB and Ethernet with PHY. This has been accomplished by its highly integrated functionality. The USB controller consists of a central 16-bit processor, mask ROM, RAM buffer, clock generator, Ethernet interface, UART, IRQ, Watchdog Timer, Serial interface, SRAM and PHY. The SIE (Serial Interface Engine) is fully compatible with the USB specification. This USB to Ethernet controller is ideal for LAN (Local Area Network), HAN (Home Area Network), Cable Modem, Set Top Boxes, or Mobile Networking applications.

Features

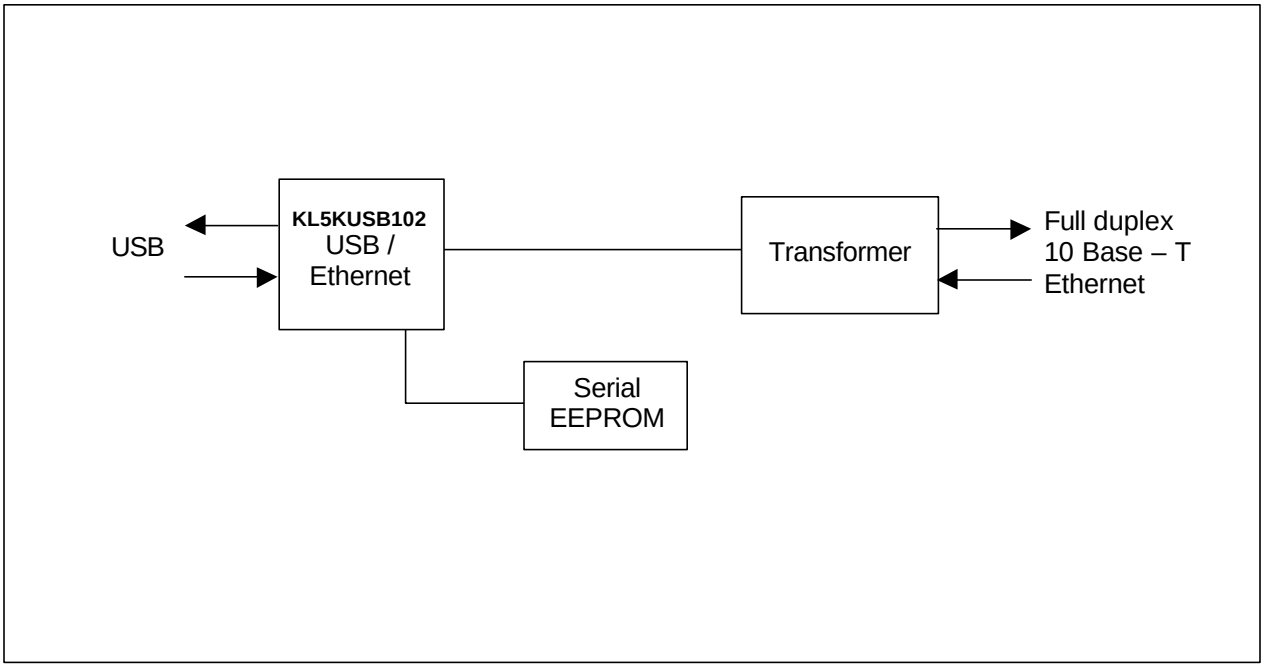
- Advanced 16 Bit processor for USB transaction processing and control data processing
- USB interface ver. 1.0/1.1 compliant
- Transceivers and SIE (Serial Interface Engine)
- Internal Clock Generation
- Utilizes low cost external crystal circuitry
- Internal RAM buffer
- Serial Interface for external EEPROM
- One Chip solution includes Ethernet MAC, SRAM, and PHY.
- PHY for 10Base-T.
- Watchdog timer
- Fully IEEE 802.3 compliant 10 Mbit/sec Ethernet MAC Layer.
- UART
- 100 pin LQFP package

Block Diagram

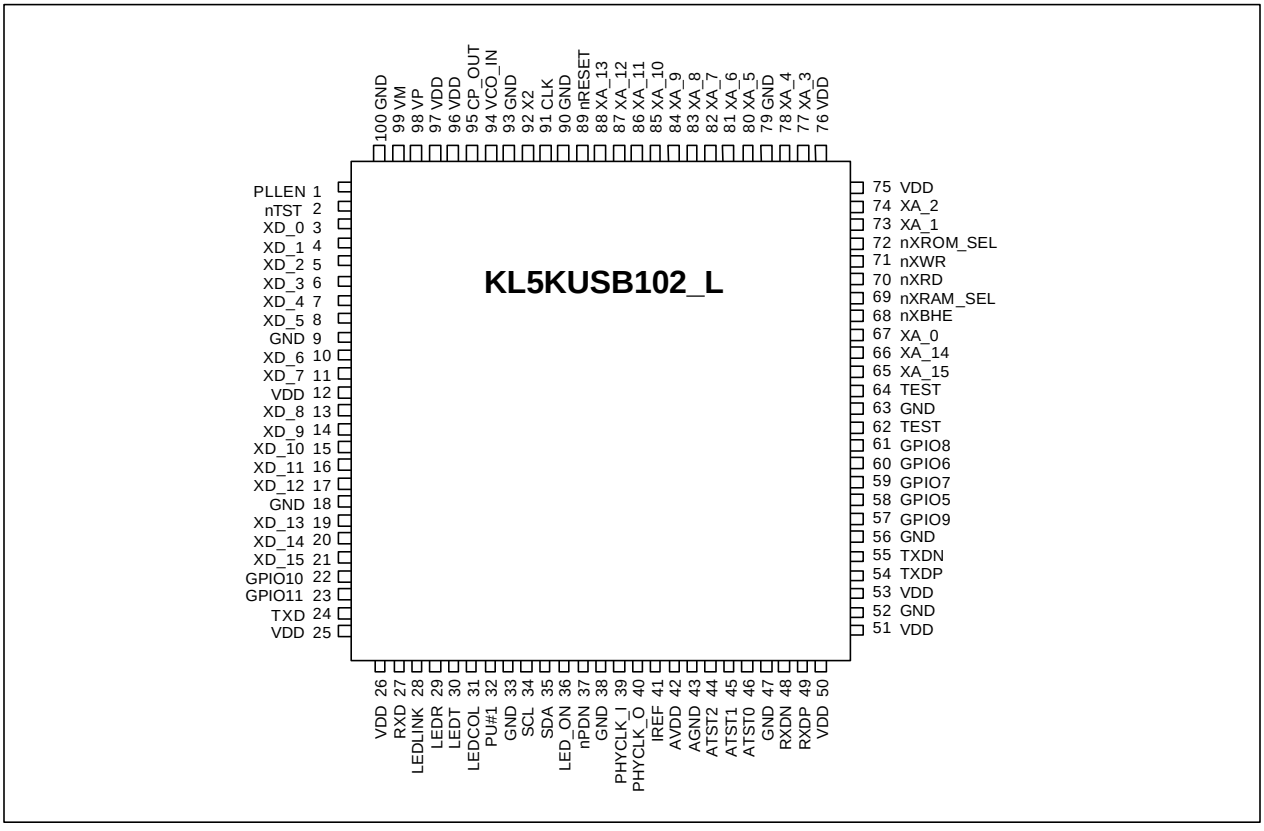


Kawasaki LSI • 2570 North First Street • Suite 301 • San Jose, CA 95131 • Tel: (408) 570-0555 • Fax: (408) 570-0567 • www.klsi.com

KL5KUSB102 Application Block Diagram



Pin Diagram 100QFP



Pin Description

Pin # QFP	I/O	Pin Name	Description
1	IN	PLLEN	PLL enable
2	IN	nTST	TEST pin (Active Low)
3	IN/OUT	XD_0	External Data Pin
4	IN/OUT	XD_1	External Data Pin
5	IN/OUT	XD_2	External Data Pin
6	IN/OUT	XD_3	External Data Pin
7	IN/OUT	XD_4	External Data Pin
8	IN/OUT	XD_5	External Data Pin
9		GND	Ground
10	IN/OUT	XD_6	External Data Pin
11	IN/OUT	XD_7	External Data Pin
12	-	VDD	Supply Voltage
13	IN/OUT	XD_8	External Data Pin
14	IN/OUT	XD_9	External Data Pin
15	IN/OUT	XD_10	External Data Pin
16	IN/OUT	XD_11	External Data Pin
17	IN/OUT	XD_12	External Data Pin
18	-	GND	Ground
19	IN/OUT	XD_13	External Data Pin
20	IN/OUT	XD_14	External Data Pin
21	IN/OUT	XD_15	External Data Pin
22	IN/OUT	GPIO10	IRQ0 or GPIO
23	IN/OUT	GPIO11	IRQ1or GPIO
24	OUT	TXD	UART TXD
25	-	VDD	Supply Voltage
26	-	VDD	Supply Voltage
27	IN	RXD	UART RXD
28	OUT	LEDLINK	LED for Link
29	OUT	LEDR	LED for Receive
30	OUT	LEDT	LED for Transmit
31	OUT	LEDCOL	LED for Collision
32	IN/OUT	PU#1	USB pull-up control
33	-	GND	Ground
34	IN/OUT	SCL	Serial ROM Clock
35	IN/OUT	SDA	Serial ROM Data
36	IN/OUT	LED_ON	LED on
37	IN/OUT	nPDN	PHY Power Down
38	-	GND	Ground
39	IN	PHYCLK_I	PHY Clock - 25MHz oscillator input
40	OUT	PHYCLK_0	PHY Clock - 25MHz oscillator output
41	-	IREF	Analog PHY - Current reference. Must be connected to ground by a ____ Ohm resistor
42	-	AVDD	Analog PHY - VDD
43	-	AGND	Analog PHY - Ground
44	-	ATST2	Analog PHY - No Connect

Pin # QFP	I/O	Pin Name	Description
45	-	ATST1	Analog PHY - No Connect
46	-	ATST0	Analog PHY - No Connect
47	-	GND	Analog PHY - Ground
48	-	RXDN	Analog PHY - Twisted pair data input.
49	-	RXDP	Analog PHY - Twisted pair data input.
50	-	VDD	Analog PHY - Supply Voltage
51	-	VDD	Analog PHY - Supply Voltage
52	-	GND	Analog PHY - Ground
53	-	VDD	Analog PHY - Supply Voltage
54	-	TXDP	Analog PHY - Twisted pair data output.
55	-	TXDN	Analog PHY - Twisted pair data output.
56	-	GND	Analog PHY - Ground
57	IN/OUT	GPIO9	Transmit data to external PHY to GPIO
58	IN/OUT	GPIO5	Collision input from external PHY or GPIO
59	IN/OUT	GPIO7	Transmit enable to external PHY or GPIO
60	IN/OUT	GPIO6	External PHY carrier sense or GPIO
61	IN/OUT	GPIO8	External PHY receive data or GPIO
62	IN	TEST	External PHY transmit clock input or fixed to ground
63	-	GND	Ground
64	IN	TEST	External PHY receive clock input or fixed to ground
65	OUT	XA_15	External Address Pin
66	OUT	XA_14	External Address Pin
67	OUT	XA_0	External Address Pin
68	OUT	nXBHE	External SRAM byte high enable (Active Low)
69	OUT	nXRAM_SEL	External SRAM byte low enable (Active Low)
70	OUT	nXRD	External Memory Read (Active Low)
71	OUT	nXWR	External Memory Write (Active Low)
72	OUT	nXROM_SEL	External ROM CS (Active Low)
73	OUT	XA_1	External Address Pin
74	OUT	XA_2	External Address Pin
75	-	VDD	Supply Voltage
76	-	VDD	Supply Voltage
77	OUT	XA_3	External Address Pin
78	OUT	XA_4	External Address Pin
79	-	GND	Ground
80	OUT	XA_5	External Address Pin
81	OUT	XA_6	External Address Pin
82	OUT	XA_7	External Address Pin
83	OUT	XA_8	External Address Pin
84	OUT	XA_9	External Address Pin
85	OUT	XA_10	External Address Pin
86	OUT	XA_11	External Address Pin
87	OUT	XA_12	External Address Pin
88	OUT	XA_13	External Address Pin
89	IN	nRESET	Reset pin (Active Low)
90	-	GND	Ground
91	IN	CLK	12MHz oscillator input
92	OUT	X2	12Mhz oscillator output
93	-	GND	Ground

Pin # QFP	I/O	Pin Name	Description
94	IN	VCO_IN	PLL VCO In
95	OUT	CP_OUT	PLL CP Out
96	-	VDD	Supply Voltage
97	-	VDD	Supply Voltage
98	IN/OUT	VP	USB D+ Pin
99	IN/OUT	VM	USB D- Pin
100	-	GND	Ground

Function Description

16 Bit Processor

The integrated 16 bit processor serves as a micro controller for USB peripherals. The processor can execute approximately five million instructions per second. With this processing power it allows the design of intelligent peripherals that can process data prior to passing it on to the host PC, thus improving overall performance of the system. The masked ROM (8K X 16) in the KL5KUSB102 or external memory contains a specialized instruction set that has been designed for highly efficient coding of processing algorithms and USB transaction processing.

The 16-bit processor is designed for efficient data execution by having direct access to the RAM Buffer, external memory, I/O interfaces, and all the control and status registers. The divide/multiply feature expands the capability of USB peripherals.

The processor supports prioritized vectored hardware interrupts. In addition, as many as 240 software interrupt vectors are available.

The processor provides six addressing modes, supporting memory-to-memory, memory-to-register, register-to-register, immediate-to-register or immediate-to-memory operations. Register, direct, immediate, indirect, and indirect indexed addressing modes are supported. In addition, there is an auto-increment mode in which a register, used as an address pointer is automatically incremented after each use, making repetitive operations more efficient both from a programming and a performance standpoint.

The processor features a full set of program control, logical, and integer arithmetic instructions. All instructions are sixteen bits wide, although some instructions require operands, which may occupy another one or two words. Several special " short immediate" instructions are available, so that certain frequently used operations with small constant operand will fit into a 16-bit instruction.

RAM Buffer

The USB controller contains a 28K byte internal buffer memory. The memory is used to buffer data and USB packets and accessed by the 16 Bit processor and the SIE. USB transactions are automatically routed to the memory buffer. The 16-bit processor has the ability to set up pointers and block sizes in buffer memory for USB transactions. Data is read from the interface and is processed and packetized by the 16-bit I/O processor.

PLL Clock Generator

The PLL circuitry is provided to generate the internal 48MHz clock requirements. This circuitry is designed to allow use of a low cost 12 MHz external crystal which is connected to the CLK and X2 pins.

USB Interface

The USB controller meets the Universal Serial Bus (USB) specification ver 1.0/1.1. The transceiver is capable of transmitting and receiving serial data at the USB's full speed, 12 Mbits/sec data rate. The driver portion of the transceiver is differential, while the receive section is comprised of a differential receiver and two single ended receivers. Internally, the transceiver interfaces to the SIE logic. Externally, the transceiver connects to the physical layer of the USB.

10Mb/sec Ethernet Interface

The KL5KUSB102 Controller has a built in 10 Mbit/sec 10-base T Ethernet MAC (Media Access Controller) which is fully compliant with the IEEE 802.3 Ethernet standard. The KL5KUSB102 Controller 16-bit processor has direct access to the registers of the MAC.

UART Interface

Supports a transfer rate of 900 to 115.2K baud.

Serial EEPROM Support

The USB Controller serial interface is used to provide access to external EEPROM's. The interface can support a variety of serial EEPROM formats.

10 base-T PHY Interface

Provides the physical layer for 10BASE-T. Drives the 10BASE-T twisted pair cable with an isolation transformer.