

# ESD5102

## Product Preview

# ESD Protection Diodes

## Micro-packaged Diodes for ESD Protection

The ESD5102 is designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, and fast response time provide best in class protection on designs that are exposed to ESD. Because of its small size, it is suited for use in smartphone, smart-watch, or many other portable / wearable applications where board space comes at a premium.

### Features

- Bi-directional Dual Line ESD Protection
- Low Capacitance (5 pF Max, I/O to GND)
- Small Body Outline Dimensions: 0.705 x 0.23 mm
- Protection for the Following IEC Standards:  
IEC 61000-4-2 (Level 4)
- Low ESD Clamping Voltage
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T <sub>J</sub>	-55 to +125	°C
Storage Temperature Range	T <sub>stg</sub>	-55 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	T <sub>L</sub>	260	°C
IEC 61000-4-2 Contact (ESD)	ESD	±15	kV
IEC 61000-4-2 Air (ESD)	ESD	±15	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.



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### MARKING DIAGRAM

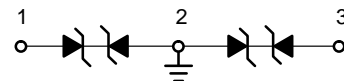


DSN3  
CASE 152AW



T = Specific Device Code  
M = Month Code

### PIN CONFIGURATION AND SCHEMATIC



### ORDERING INFORMATION

Device	Package	Shipping†
ESD5102FCT5G	DSN3 (Pb-Free)	10,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V <sub>RWM</sub>	I/O Pin to GND			3.3	V
Breakdown Voltage	V <sub>BR</sub>	I <sub>T</sub> = 1 mA, I/O Pin to GND	4	5	6.5	V
Reverse Leakage Current	I <sub>R</sub>	V <sub>RWM</sub> = 3.3 V, I/O Pin to GND			1	μA
Clamping Voltage TLP (Note 1)	V <sub>C</sub>	I <sub>PP</sub> = 8 A } IEC 61000-4-2 Level 2 equivalent (±4 kV Contact, ±4 kV Air)		5.4		V
		I <sub>PP</sub> = 16 A } IEC 61000-4-2 Level 2 equivalent (±8 kV Contact, ±15 kV Air)		6.5		
Junction Capacitance	C <sub>J</sub>	V <sub>R</sub> = 0 V, f = 1 MHz			5	pF

1. ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.  
TLP conditions: Z<sub>0</sub> = 50 Ω, t<sub>p</sub> = 100 ns, t<sub>r</sub> = 4 ns, averaging window; t<sub>1</sub> = 30 ns to t<sub>2</sub> = 60 ns.

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## TYPICAL CHARACTERISTICS

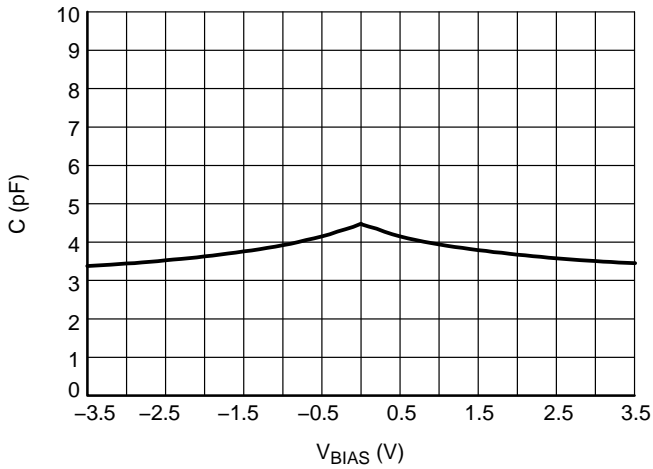


Figure 1. CV Characteristics

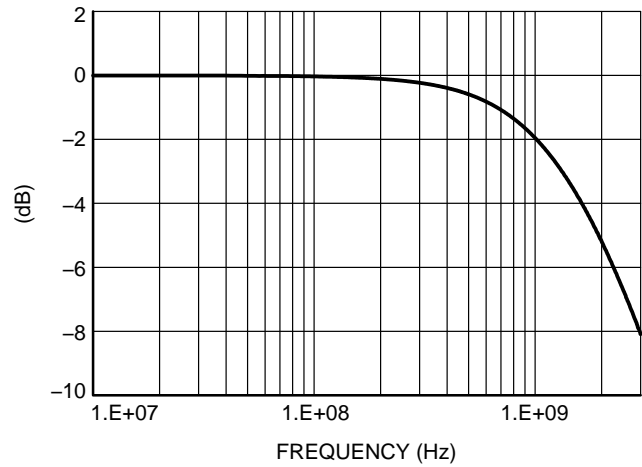


Figure 2. S21 Insertion Loss

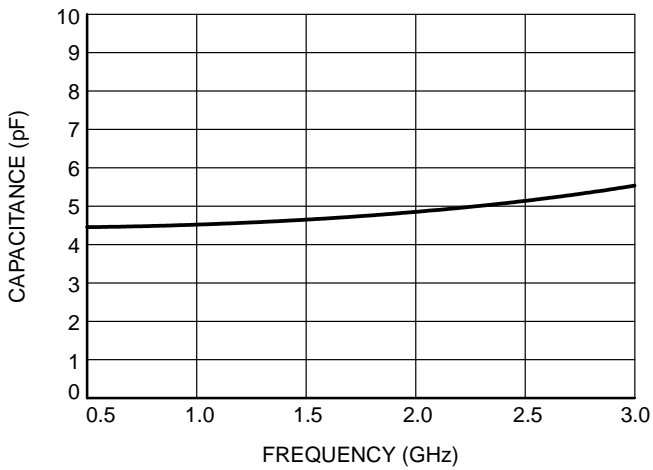


Figure 3. Capacitance over Frequency

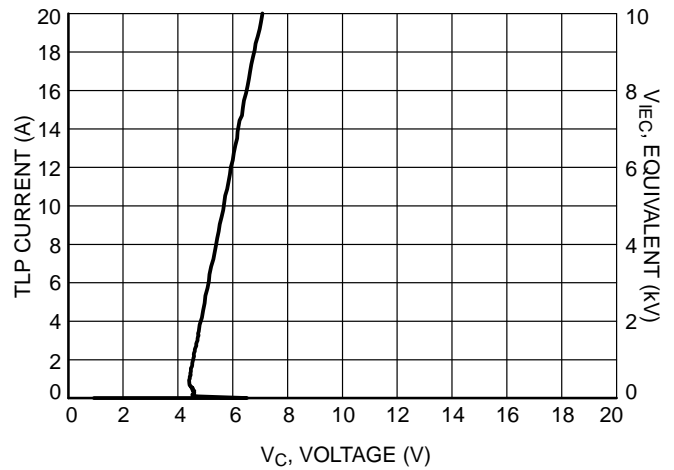


Figure 4. Positive TLP I-V Curve

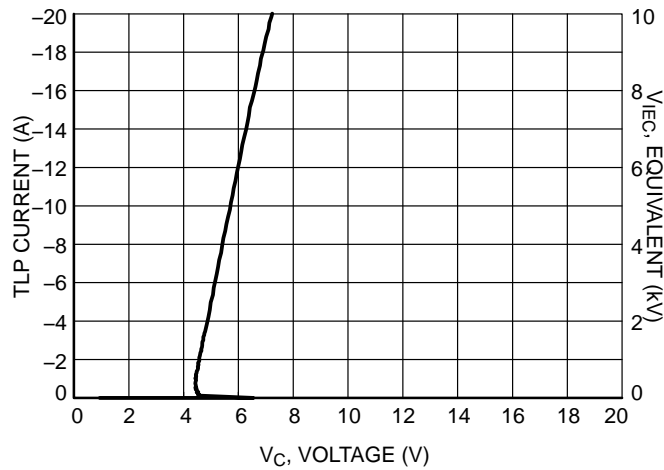


Figure 5. Negative TLP I-V Curve

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



Figure 6. IEC61000-4-2 Spec

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 7. TLP I-V curves of ESD protection devices accurately demonstrate the product’s ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 8 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

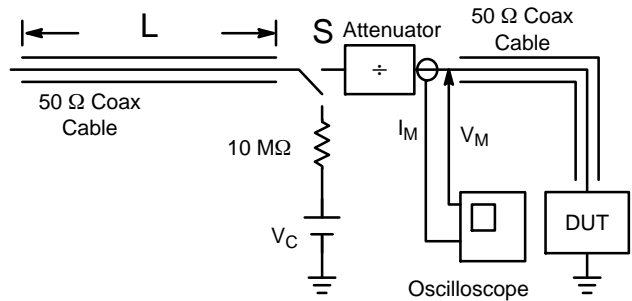


Figure 7. Simplified Schematic of a Typical TLP System

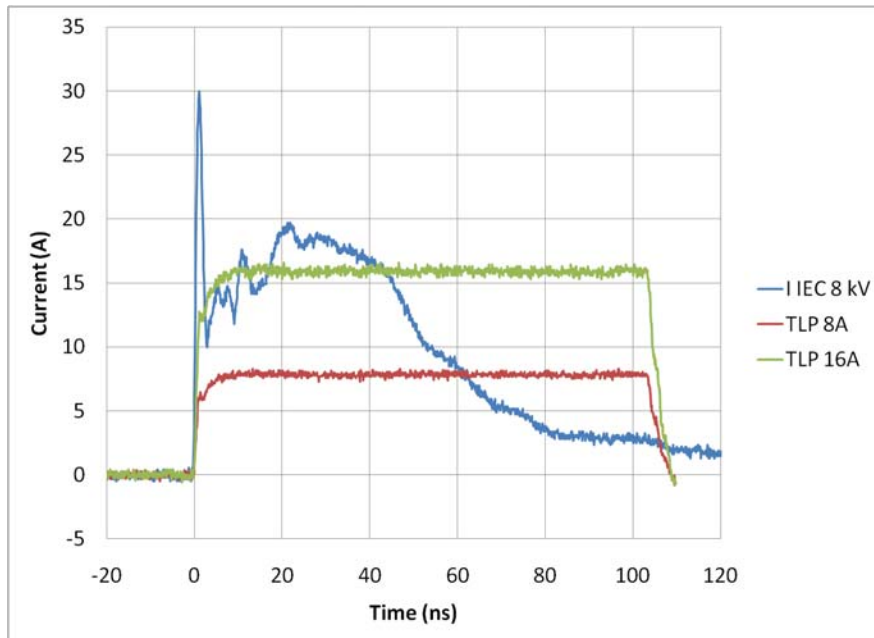
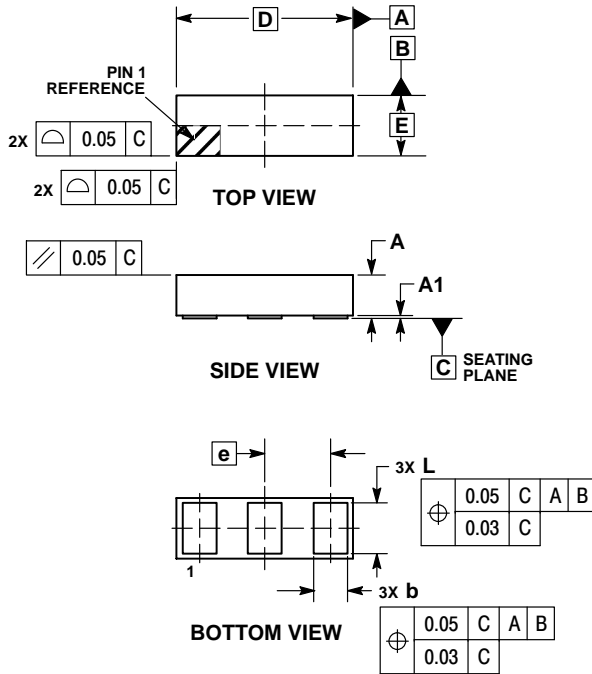


Figure 8. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

# ESD5102

## PACKAGE DIMENSIONS

DSN3, 0.73x0.25, 0.27P  
CASE 152AW  
ISSUE O

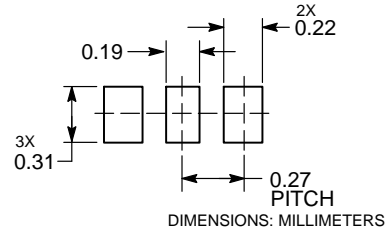


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.

MILLIMETERS		
DIM	MIN	MAX
A	0.13	0.23
A1	---	0.03
b	0.11	0.17
D	0.73 BSC	
E	0.25 BSC	
e	0.27 BSC	
L	0.18	0.24

**RECOMMENDED SOLDER FOOTPRINT\***



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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