

ESD5101, ESD5111

ESD Protection Diodes

Micro-packaged Diodes for ESD Protection

The ESD51x1 Series is designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, and fast response time provide best in class protection on designs that are exposed to ESD. Because of its small size, it is suited for use in smartphone, smart-watch, or many other portable / wearable applications where board space comes at a premium.

Features

- Low Capacitance (5 pF Max, I/O to GND)
- Small Body Outline Dimensions
 - ◆ 01005 Size: 0.435 x 0.23 mm
 - ◆ 0201 Size: 0.6 x 0.3 mm
- Protection for the Following IEC Standards:
IEC 61000-4-2 (Level 4)
- Low ESD Clamping Voltage
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T _J	-55 to +125	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Lead Solder Temperature – Maximum (10 Seconds)	T _L	260	°C
IEC 61000-4-2 Contact (ESD)	ESD	±15	kV
IEC 61000-4-2 Air (ESD)	ESD	±15	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

See Application Note AND8308/D for further description of survivability specs.









This document contains information on some products that are still under development. ON Semiconductor reserves the right to change or discontinue these products without notice.



ON Semiconductor®

www.onsemi.com

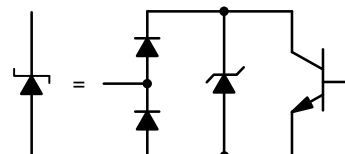
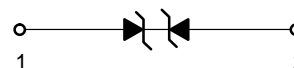
MARKING DIAGRAMS

	ESD5101 (01005) DSN2 CASE 152AK	
	ESD5101P (01005) DSN2 CASE TBD*	
	ESD5111 (0201) WLCSP2 CASE 567AV	
	ESD5111P (0201) WLCSP2 CASE TBD*	

L, E, X = Device Code
M = Date Code

* In Development

PIN CONFIGURATION AND SCHEMATIC



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ESD5101, ESD5111

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Working Voltage	V _{RWM}	I/O Pin to GND			3.3	V
Breakdown Voltage	V _{BR}	I _T = 1 mA, I/O Pin to GND	3.68	5.0	6.5	V
Reverse Leakage Current	I _R	V _{RWM} = 3.3 V, I/O Pin to GND			0.1	μA
ESD5101, ESD5111 Clamping Voltage TLP (Note 1)	V _C	I _{PP} = 8 A } IEC 61000-4-2 Level 2 equivalent (±4 kV Contact, ±4 kV Air)		5.5		V
		I _{PP} = 16 A } IEC 61000-4-2 Level 2 equivalent (±8 kV Contact, ±15 kV Air)		6.5		
Junction Capacitance	C _J	V _R = 0 V, f = 1 MHz			5.5	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.

TLP conditions: Z₀ = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t₁ = 30 ns to t₂ = 60 ns.

ORDERING INFORMATION

Device	Package	Shipping†
ESD5101FCT5G	DSN2 (Pb-Free)	10,000 / Tape & Reel
ESD5111FCT5G	WLCSP2 (Pb-Free)	10,000 / Tape & Reel
ESD5101PFCT5G**	Side wall Isolated 01005	10,000 / Tape & Reel
ESD5111PFCT5G**	Side wall Isolated 0201	10,000 / Tape & Reel

** In Development. Contact local sales rep for availability.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ESD5101, ESD5111

TYPICAL CHARACTERISTICS

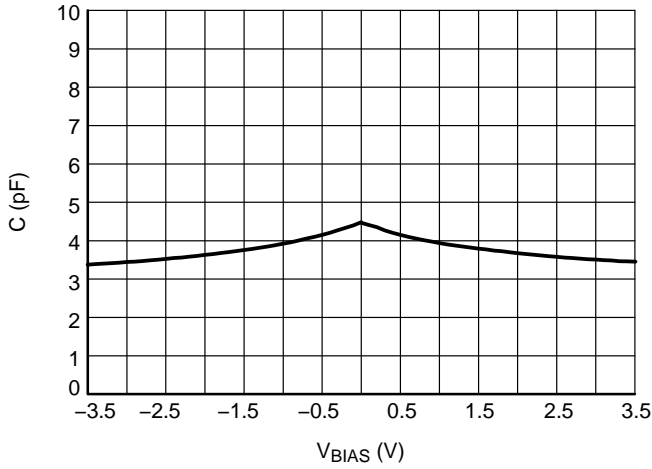


Figure 1. ESD5101 CV Characteristics

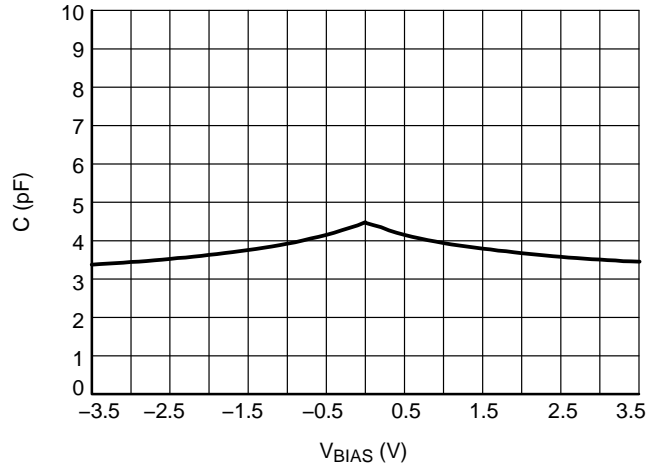


Figure 2. ESD5111 CV Characteristics

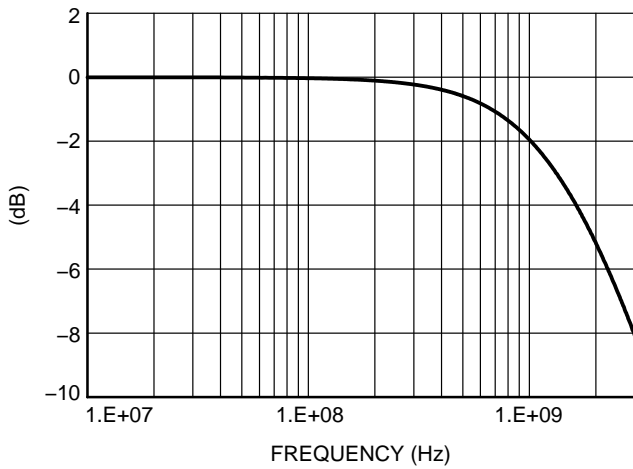


Figure 3. ESD5101 S21 Insertion Loss

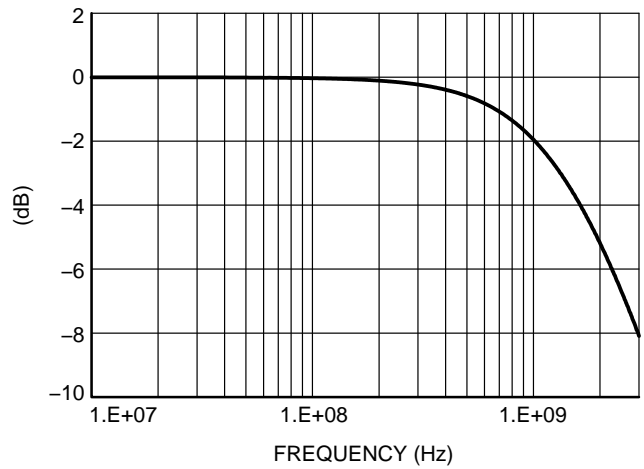


Figure 4. ESD5111 S21 Insertion Loss

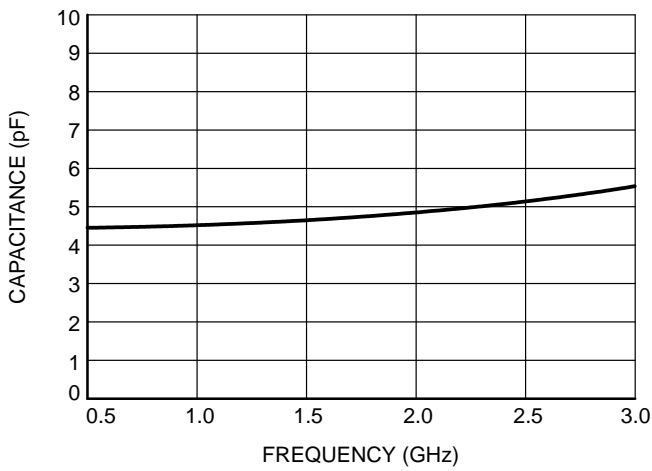


Figure 5. ESD5101 Capacitance over Frequency

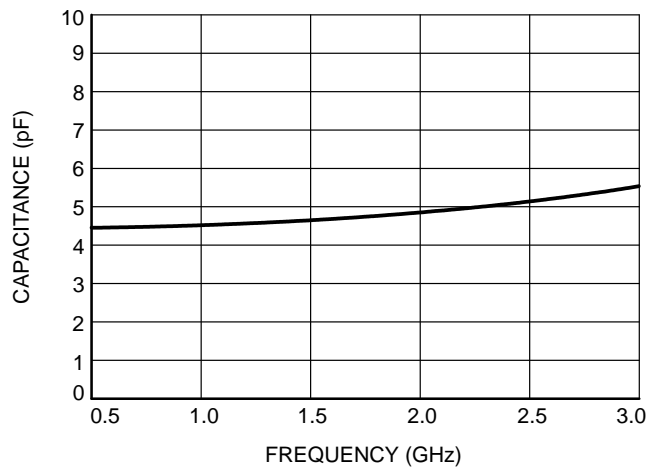


Figure 6. ESD5111 Capacitance over Frequency

ESD5101, ESD5111

TYPICAL CHARACTERISTICS

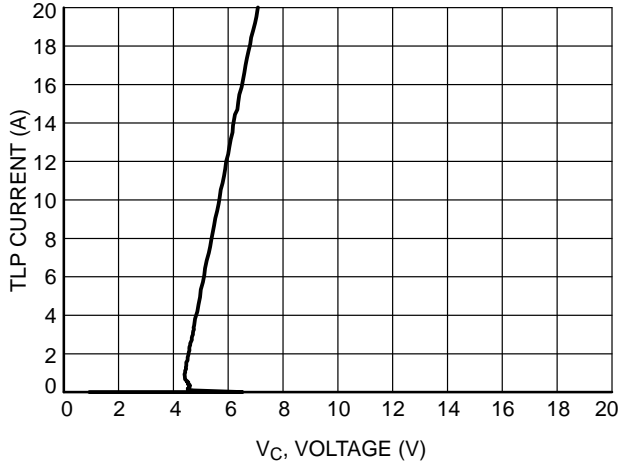


Figure 7. ESD5101 Positive TLP I-V Curve

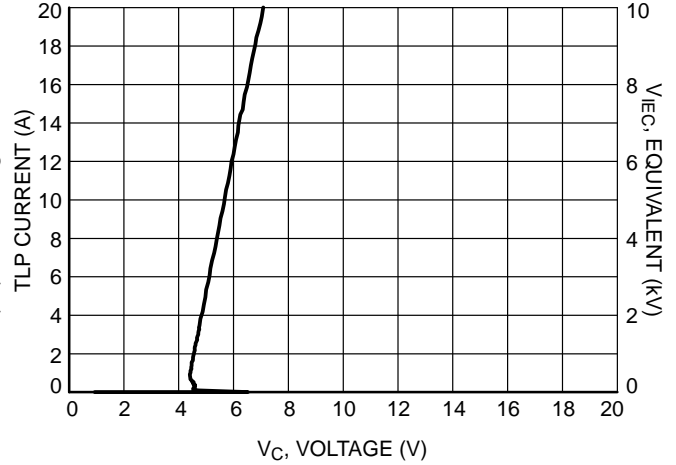


Figure 8. ESD5111 Positive TLP I-V Curve

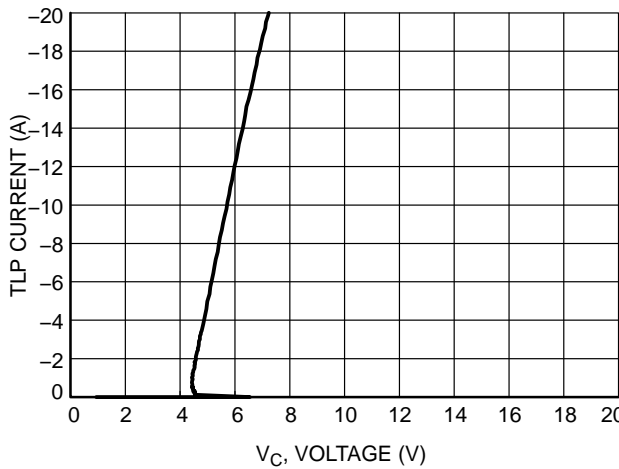


Figure 9. ESD5101 Negative TLP I-V Curve

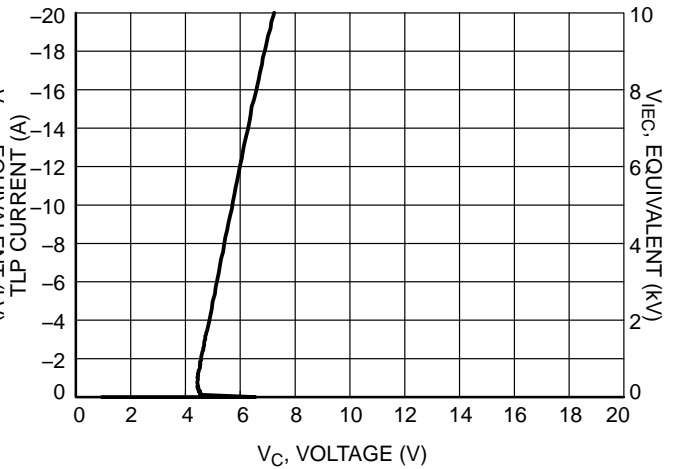


Figure 10. ESD5111 Negative TLP I-V Curve

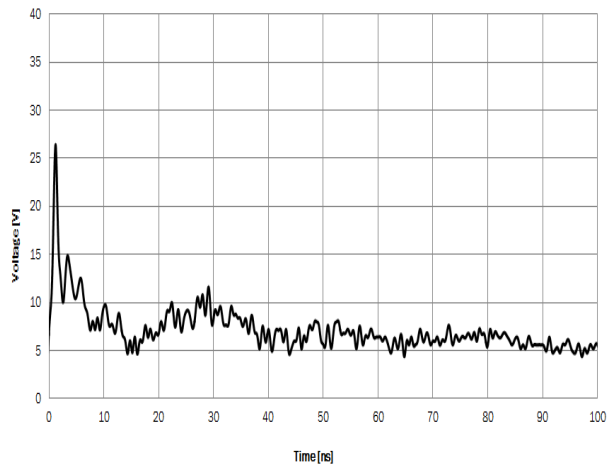


Figure 11. ESD5111 Positive 8 kV ESD Contact Discharge

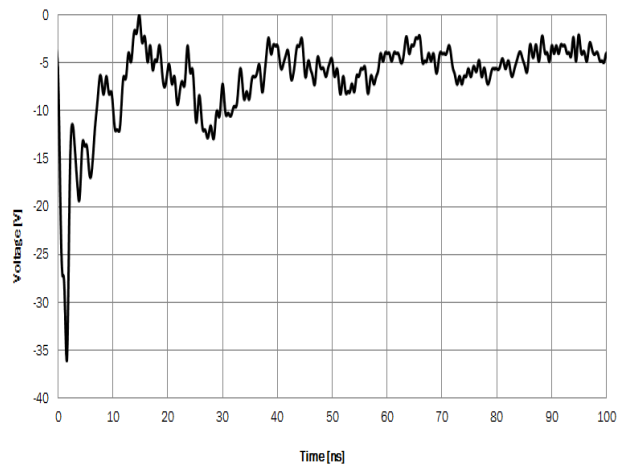


Figure 12. ESD5111 Negative 8 kV ESD Contact Discharge

ESD5101, ESD5111

IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8



Figure 13. IEC61000-4-2 Spec

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 14. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 15 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

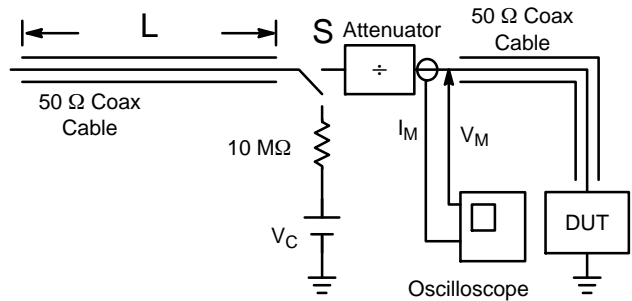


Figure 14. Simplified Schematic of a Typical TLP System

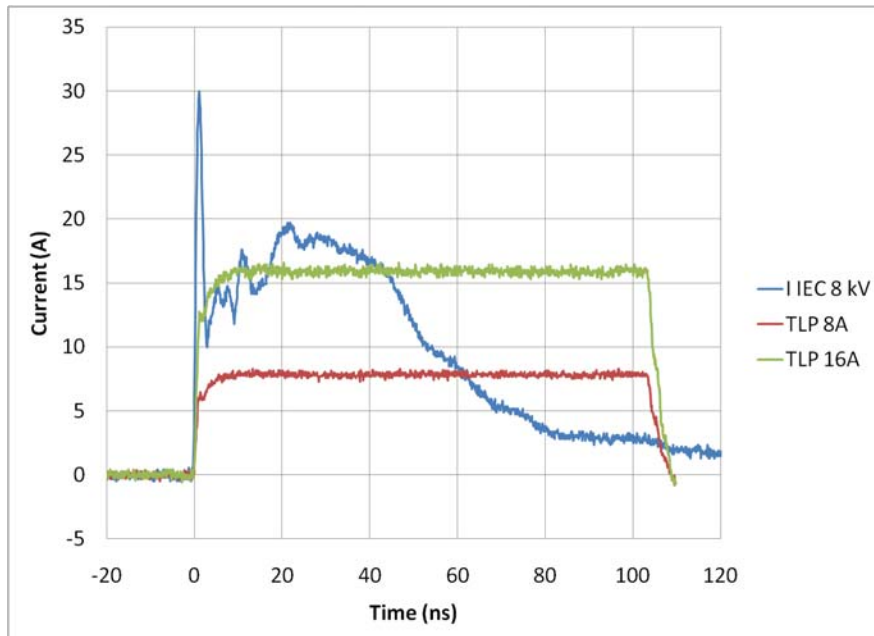
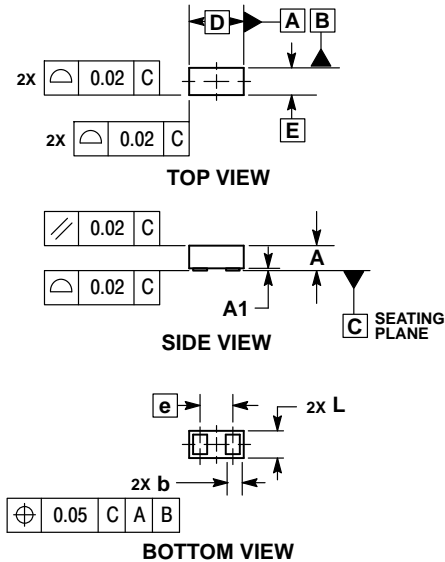


Figure 15. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

ESD5101, ESD5111

PACKAGE DIMENSIONS – ESD5111 (0201)

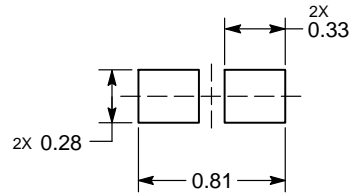
WLCSP2, 0.6x0.3
CASE 567AV
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.

MILLIMETERS		
DIM	MIN	MAX
A	0.25	0.30
A1	0.00	0.05
b	0.14	0.17
D	0.60	BSC
E	0.30	BSC
e	0.36	BSC
L	0.19	0.24

RECOMMENDED SOLDER FOOTPRINT*

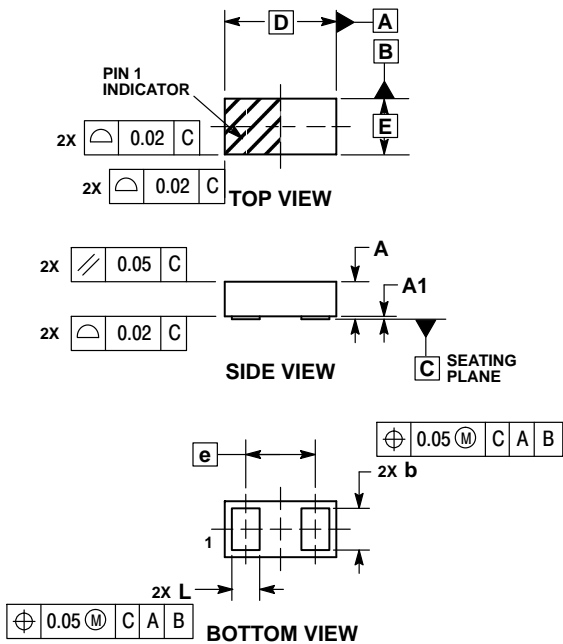


DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS – ESD5101 (01005)

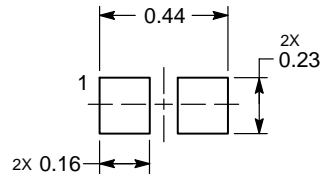
DSN2, 0.435x0.23, 0.27P, (01005)
CASE 152AK
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.

MILLIMETERS		
DIM	MIN	MAX
A	0.165	0.195
A1	—	0.030
b	0.177	0.193
D	0.435	BSC
E	0.230	BSC
e	0.270	BSC
L	0.112	0.128

RECOMMENDED SOLDER FOOTPRINT*



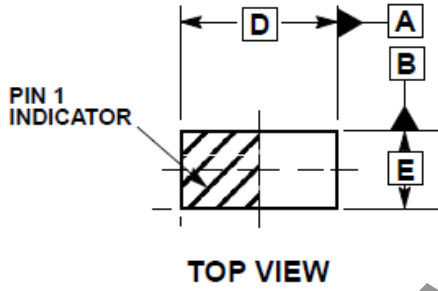
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ESD5101, ESD5111

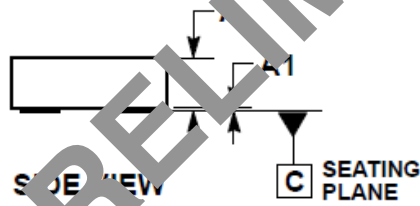
PACKAGE DIMENSIONS – ESD5101P (01005)

Side Wall Isolated 0.435x0.23 [01005]
 CASE TBD
 PRELIMINARY

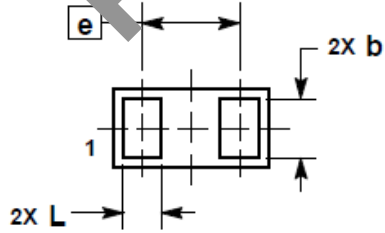


TOP VIEW

MILLIMETERS		
SYM	MIN	MAX
A	TBD	
A1	---	0.030
b	0.177	0.193
D	0.435 BSC	
E	0.230 BSC	
e	0.270 BSC	
L	0.112	0.128



SIDE VIEW

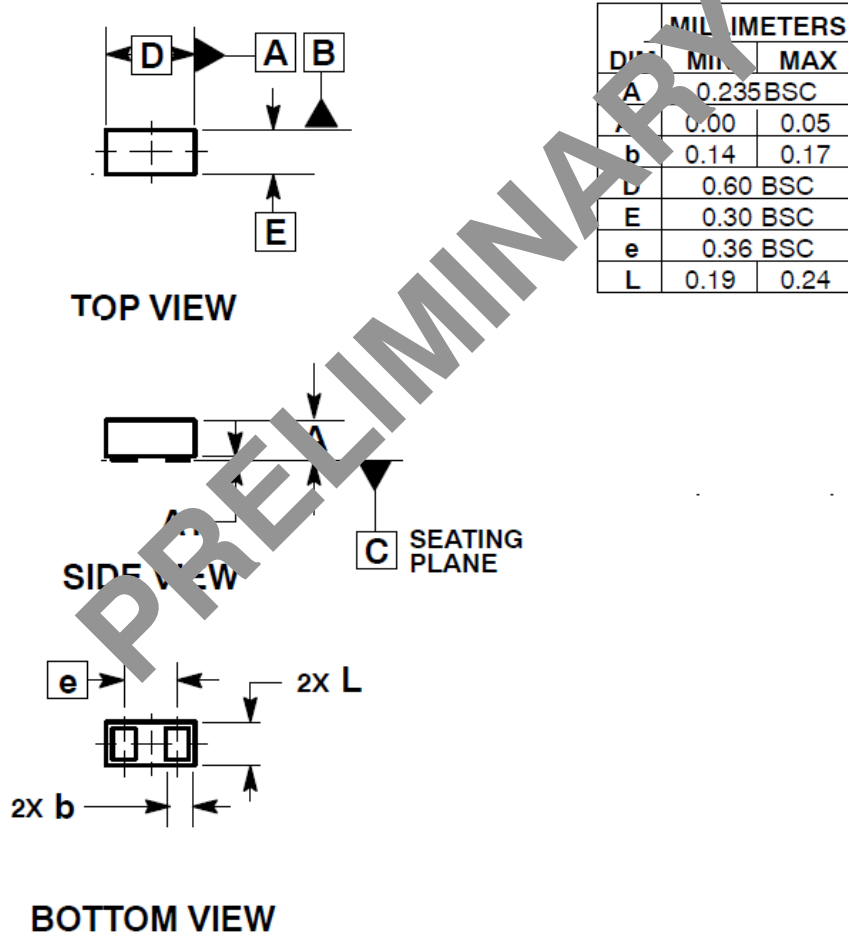


BOTTOM VIEW

ESD5101, ESD5111

PACKAGE DIMENSIONS – ESD5111P (0201)

Side Wall Isolated 0.6x0.3 [0201]
 CASE TBD
 PRELIMINARY



ON Semiconductor and the are registered trademarks of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and/or other countries. SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
 Literature Distribution Center for ON Semiconductor
 19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
 USA/Canada
Europe, Middle East and Africa Technical Support:
 Phone: 421 33 790 2910
Japan Customer Focus Center
 Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
 For additional information, please contact your local
 Sales Representative