AK4357

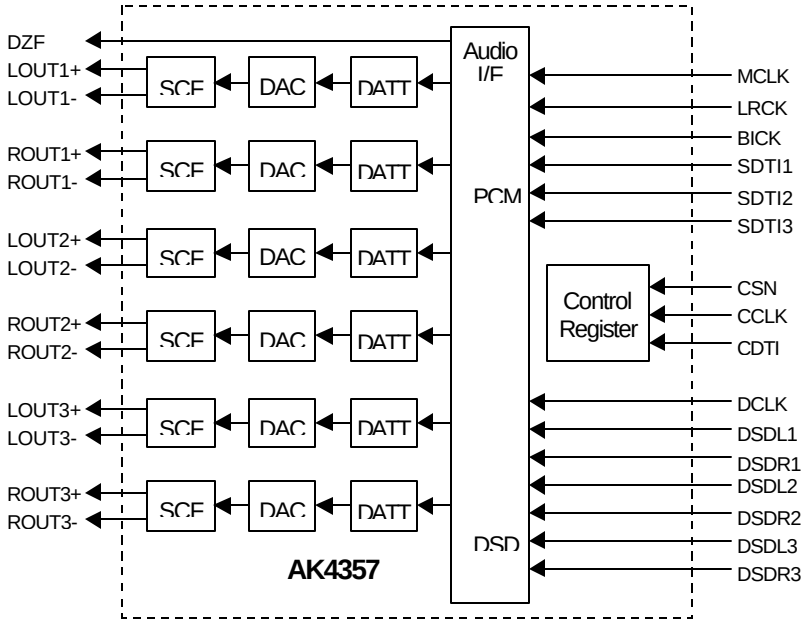
192kHz 24-Bit 6ch DAC with DSD Input

GENERAL DESCRIPTION

The AK4357 is six channels 24bit DAC corresponding to digital audio system. Using AKM's advanced multi bit architecture for its modulator the AK4357 delivers a wide dynamic range while preserving linearity for improved THD+N performance. The AK4357 has full differential SCF outputs, removing the need for AC coupling capacitors and increasing performance for systems with excessive clock jitter. The AK4357 accepts 192kHz PCM data and 1-Bit DSD data, ideal for a wide range of applications including DVD-Audio and SACD.

FEATURES

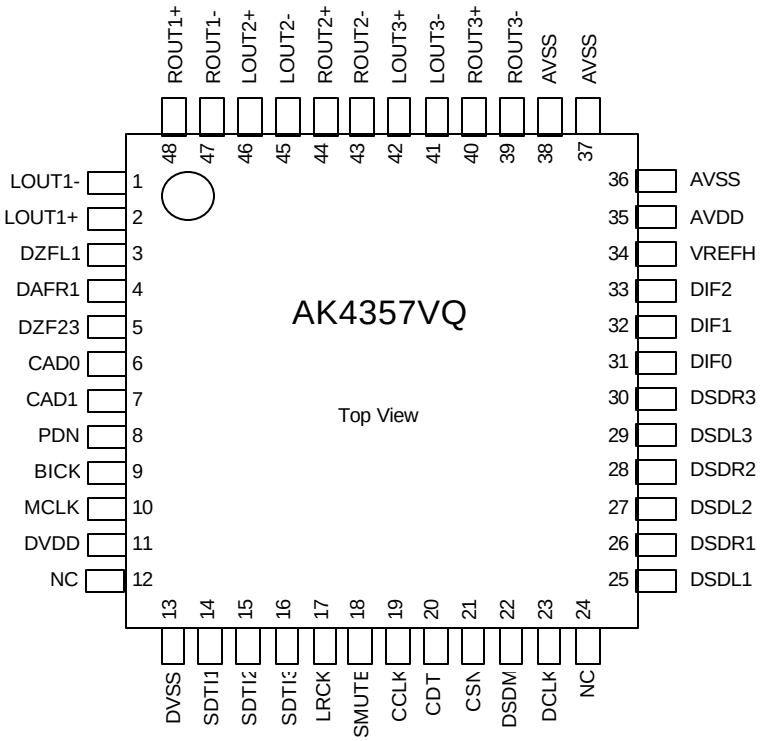
- **Sampling Rate Ranging from 8kHz to 192kHz**
- **24Bit 8 times Digital Filter with Slow roll-off option**
- **THD+N: -90dB**
- **DR, S/N: 106dB**
- **High Tolerance to Clock Jitter**
- **Low Distortion Differential Output**
- **DSD Data input available**
- **Channel Independent Digital De-emphasis for 32, 44.1 & 48kHz sampling**
- **Zero Detect function**
- **Channel Independent Digital Attenuator with soft-transition (3 Speed mode)**
- **Soft Mute**
- **3-wire Serial Interface for Volume Control**
- **Master clock: 256fs, 384fs, 512fs or 768fs (PCM Normal Speed Mode)**
  128fs, 192fs, 256fs or 384fs (PCM Double Speed Mode)
  128fs or 192fs (PCM Quad Speed Mode)
  512fs or 768fs (DSD Mode)
- **Power Supply: 4.75 to 5.25V**
- **48pin LQFP Package**



■ Ordering Guide

AK4357VQ	-40 ~ +85°C	48LQFP
AKD4357	Evaluation Board for AK4357	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	LOUT1-	O	DAC1 Lch Negative Analog Output Pin
2	LOUT1+	O	DAC1 Lch Positive Analog Output Pin
3	DZFL1	O	DAC1 Lch Zero Input Detect Pin
4	DZFR1	O	DAC1 Rch Zero Input Detect Pin
5	DZF23	O	DAC2,3 Zero Input Detect Pin
6	CAD0	I	Chip Address 0 Pin
7	CAD1	I	Chip Address 1 Pin
8	PDN	I	Power-Down Mode Pin When at "L", the AK4357 is in the power-down mode and is held in reset. The AK4357 should always be reset upon power-up.
9	BICK	I	Audio Serial Data Clock Pin
10	MCLK	I	Master Clock Input Pin An external TTL clock should be input on this pin.

No.	Pin Name	I/O	Function
11	DVDD	-	Digital Power Supply Pin, +4.75~+5.25V
12	NC	-	NC pin No internal bonding
13	DVSS	-	Digital Ground Pin
14	SDTI1	I	DAC1 Audio Serial Data Input Pin
15	SDTI2	I	DAC2 Audio Serial Data Input Pin
16	SDTI3	I	DAC3 Audio Serial Data Input Pin
17	LRCK	I	L/R Clock Pin
18	SMUTE	I	Soft Mute Pin When this pin goes to "H", soft mute cycle is initialized. When returning to "L", the output mute releases.
19	CCLK	I	Control Data Clock Pin
20	CDTI	I	Control Data Input Pin
21	CSN	I	Chip Select Pin
22	DSDM	I	DSD Mode Enable Pin (Pull-down Pin) "0": PCM mode "1": DSD mode
23	DCLK	I	DSD Clock Pin
24	NC	-	NC pin No internal bonding
25	DSDL1	I	DAC1 DSD Lch Data Input Pin
26	DSDR1	I	DAC1 DSD Rch Data Input Pin
27	DSDL2	I	DAC2 DSD Lch Data Input Pin
28	DSDR2	I	DAC2 DSD Rch Data Input Pin
29	DSDL3	I	DAC3 DSD Lch Data Input Pin
30	DSDR3	I	DAC3 DSD Rch Data Input Pin
31	DIF0	I	Audio Data Interface Format 0 Pin
32	DIF1	I	Audio Data Interface Format 1 Pin
33	DIF2	I	Audio Data Interface Format 2 Pin
34	VREFH	I	Positive Voltage Reference Input Pin
35	AVDD	-	Analog Power Supply Pin, +4.75~+5.25V
36	AVSS	-	Analog Ground Pin
37	AVSS	-	Analog Ground Pin
38	AVSS	-	Analog Ground Pin
39	ROUT3-	O	DAC3 Rch Negative Analog Output Pin
40	ROUT3+	O	DAC3 Rch Positive Analog Output Pin
41	LOUT3-	O	DAC3 Lch Negative Analog Output Pin
42	LOUT3+	O	DAC3 Lch Positive Analog Output Pin
43	ROUT2-	O	DAC2 Rch Negative Analog Output Pin
44	ROUT2+	O	DAC2 Rch Positive Analog Output Pin
45	LOUT2-	O	DAC2 Lch Negative Analog Output Pin
46	LOUT2+	O	DAC2 Lch Positive Analog Output Pin
47	ROUT1-	O	DAC1 Rch Negative Analog Output Pin
48	ROUT1+	O	DAC1 Rch Positive Analog Output Pin

Note: All input pins except pull-down pin should not be left floating.

ABSOLUTE MAXIMUM RATINGS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	max	Units
Power Supplies	Analog	AVDD	-0.3	6.0	V
	Digital	DVDD	-0.3	6.0	V
	|AVSS-DVSS| (Note 2)	ΔGND	-	0.3	V
Input Current (any pins except for supplies)		IIN	-	±10	mA
Analog Input Voltage		VINA	-0.3	AVDD+0.3	V
Digital Input Voltage		VIND	-0.3	DVDD+0.3	V
Ambient Operating Temperature		Ta	-40	85	°C
Storage Temperature		Tstg	-65	150	°C

Note: 1. All voltages with respect to ground.
2. AVSS and DVSS must be connected to the same analog ground plane.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS, DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies (Note 3)	Analog	AVDD	4.75	5.0	5.25	V
	Digital	DVDD	4.75	5.0	5.25	V
Voltage Reference		VREF	AVDD-0.5	-	AVDD	V

Note: 1. All voltages with respect to ground.
3. The power up sequence between AVDD and DVDD is not critical.

*AKM assumes no responsibility for the usage beyond the conditions in this datasheet.

ANALOG CHARACTERISTICS

(Ta=25°C; AVDD, DVDD=5V; VREF=AVDD; fs=44.1kHz; BICK=64fs; Signal Frequency=1kHz; 24bit Input Data; Measurement frequency=20Hz ~ 20kHz; $R_L \geq 4k\Omega$; unless otherwise specified)

Parameter			min	typ	max	Units
Resolution					24	Bits
Dynamic Characteristics	(Note 4)					
THD+N	fs=44.1kHz BW=20kHz	0dBFS		-90	-86	dB
	fs=96kHz BW=40kHz	0dBFS		-88	-84 -	dB dB
	fs=192kHz BW=40kHz	0dBFS		-86	- -	dB dB
Dynamic Range (-60dBFS with A-weighted)		(Note 5)	100	106		dB
S/N (A-weighted)		(Note 6)	100	106		dB
Interchannel Isolation (1kHz)			90	100		dB
Interchannel Gain Mismatch				0.2	0.5	dB
DC Accuracy						
Gain Drift				100	-	ppm/°C
Output Voltage		(Note 7)	±2.35	±2.5	±2.65	Vpp
Load Resistance		(Note 8)	4			kΩ
Power Supplies						
Power Supply Current (AVDD+DVDD)						
Normal Operation (PDN = "H", fs≤96kHz)				50	75	mA
Normal Operation (PDN = "H", fs=192kHz)				60	85	mA
Power-Down Mode (PDN = "L")		(Note 9)		10	100	μA

Note: 4. Measured by Audio Precision System Two. Refer to the evaluation board manual.
5. 100dB at 16bit data.
6. S/N is independent of input bit length.
7. Full scale voltage (0dB). Output voltage scales with the voltage of VREFH pin.
AOUT(typ.@0dB)=(AOUT+)-(AOUT-)=±2.5Vpp*VREFH/5.0
8. For AC-load. 8kΩ for DC-load
9. All digital inputs including clock pins (MCLK, BICK and LRCK) are held DVDD or DVSS.

SHARP ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; AVDD, DVDD = 4.75 ~ 5.25V; fs = 44.1kHz; DEM = OFF; SLOW="0"; PCM Mode)

Parameter			Symbol	min	typ	max	Units
Digital filter							
Passband ±0.05dB (Note 9)			PB	0		20.0	kHz
-6.0dB				-	22.05	-	kHz
Stopband (Note 10)			SB	24.1			kHz
Passband Ripple			PR			± 0.02	dB
Stopband Attenuation			SA	54			dB
Group Delay (Note 11)			GD	-	19.1	-	1/fs
Digital Filter + SCF							
Frequency Response	20.0kHz	Fs=44.1kHz	FR	-	± 0.2	-	dB
	40.0kHz	Fs=96kHz	FR	-	± 0.3	-	dB
	80.0kHz	Fs=192kHz	FR	-	+0/-0.6	-	dB

Notes: 10. The passband and stopband frequencies scale with fs(system sampling rate).
For example, PB=0.4535×fs (@±0.05dB), SB=0.546×fs.

11. The calculating delay time which occurred by digital filtering. This time is from setting the 16/24bit data of both channels to input register to the output of analog signal.

SLOW ROLL-OFF FILTER CHARACTERISTICS

(Ta = 25°C; AVDD, DVDD = 4.75~5.25V; fs = 44.1kHz; DEM = OFF; SLOW = "1"; PCM Mode)

Parameter			Symbol	min	Typ	max	Units
Digital Filter							
Passband ±0.04dB (Note 12)			PB	0		8.1	kHz
-3.0dB				-	18.2	-	kHz
Stopband (Note 12)			SB	39.2			kHz
Passband Ripple			PR			± 0.005	dB
Stopband Attenuation			SA	72			dB
Group Delay (Note 11)			GD	-	19.1	-	1/fs
Digital Filter + SCF							
Frequency Response	20.0kHz	fs=44.kHz	FR	-	+0/-5	-	dB
	40.0kHz	fs=96kHz	FR	-	+0/-4	-	dB
	80.0kHz	fs=192kHz	FR	-	+0/-5	-	dB

Note: 12. The passband and stopband frequencies scale with fs.
For example, PB = 0.185×fs (@±0.04dB), SB = 0.888×fs.

DC CHARACTERISTICS

(Ta = 25°C; AVDD, DVDD = 4.75 ~ 5.25V)

Parameter	Symbol	min	Typ	max	Units
High-Level Input Voltage	VIH	2.2	-	-	V
Low-Level Input Voltage	VIL	-	-	0.8	V
High-Level Output Voltage (Iout = -80μA)	VOH	DVDD-0.4	-	-	V
Low-Level Output Voltage (Iout = 80μA)	VOL	-		0.4	V
Input Leakage Current (Note 13)	Iin	-	-	± 10	μA

Note: 13. DSDM pin has internal pull-down devices, nominally 100kΩ.

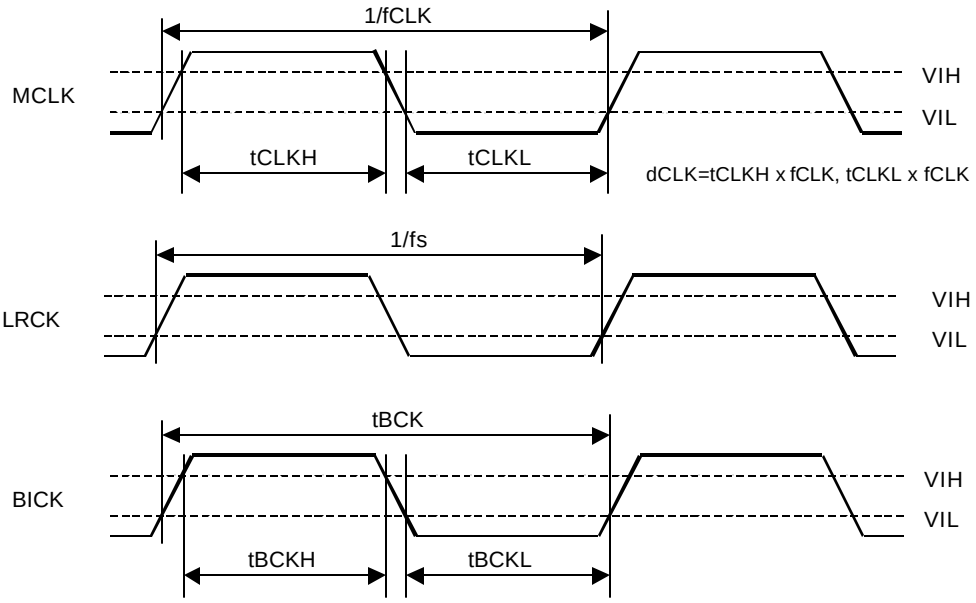
SWITCHING CHARACTERISTICS

(Ta = 25°C; AVDD, DVDD = 4.75 ~ 5.25V; C_L = 20pF)

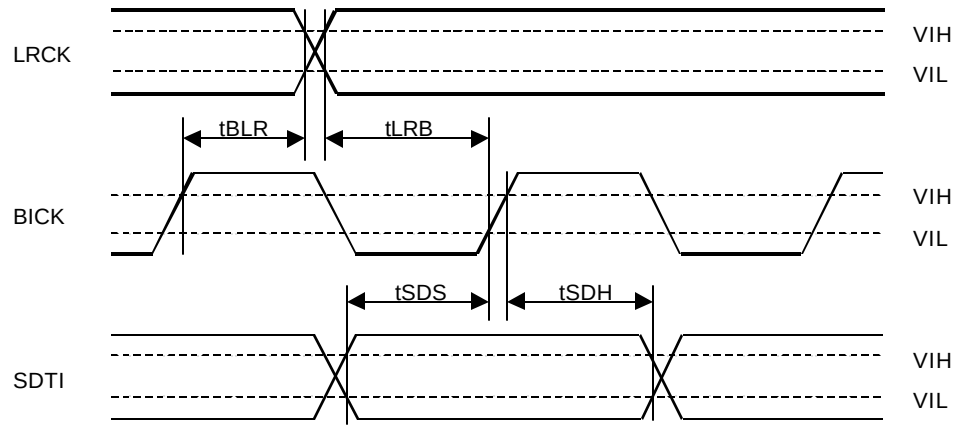
Parameter		Symbol	min	Typ	max	Units
Master Clock Frequency		fCLK	2.048	11.2896	36.864	MHz
Duty Cycle		dCLK	40		60	%
LRCK Frequency						
Normal Speed Mode		fsn	8		48	kHz
Double Speed Mode		fsd	60		96	kHz
Quad Speed Mode		fsq	120		192	kHz
Duty Cycle		Duty	45		55	%
PCM Audio Interface Timing						
BICK Period						
Normal Speed Mode		tBCK	1/128fs			ns
Double/Quad Speed Mode		tBCK	1/64fs			ns
BICK Pulse Width Low		tBCKL	30			ns
Pulse Width High		tBCKH	30			ns
BICK "↑" to LRCK Edge	(Note 13)	tBLR	20			ns
LRCK Edge to BICK "↑"	(Note 13)	tLRB	20			ns
SDTI Hold Time		tSDH	20			ns
SDTI Setup Time		tSDS	20			ns
DSD Audio Interface Timing						
DCLK Period		tDCK	1/64fs			ns
DCLK Pulse Width Low		tDCKL	160			ns
Pulse Width High		tDCKH	160			ns
DCLK Edge to DSDL/R	(Note 14)	tDDD	-20		20	ns
Control Interface Timing						
CCLK Period		tCCK	200			ns
CCLK Pulse Width Low		tCCKL	80			ns
Pulse Width High		tCCKH	80			ns
CDTI Setup Time		tCDS	40			ns
CDTI Hold Time		tCDH	40			ns
CSN High Time		tCSW	150			ns
CSN "↓" to CCLK "↑"		tCSS	50			ns
CCLK "↑" to CSN "↑"		tCSH	50			ns
Reset Timing						
PDN Pulse Width	(Note 15)	tPD	150			ns

Notes: 13. BICK rising edge must not occur at the same time as LRCK edge.
14. DSD data transmitting device must meet this time.
15. The AK4357 can be reset by bringing PDN= "L".

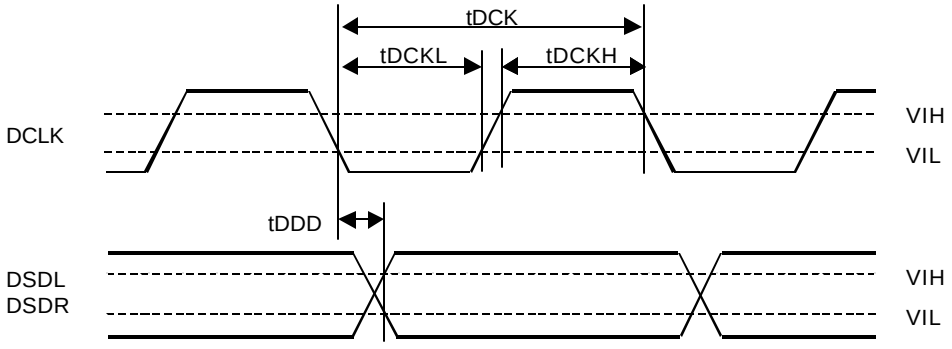
■ Timing Diagram



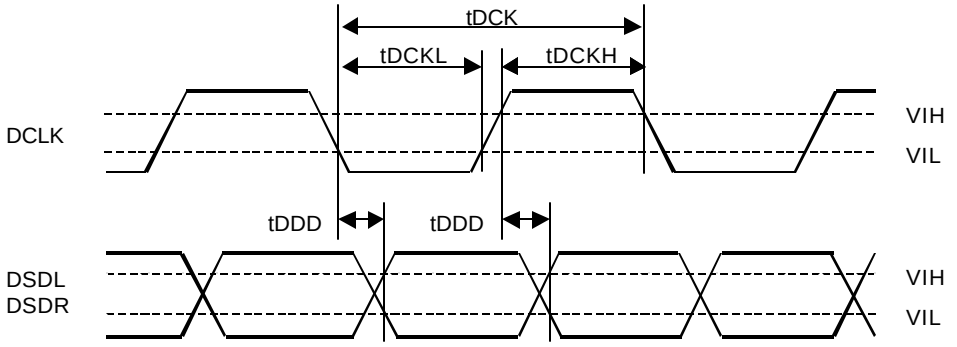
Clock Timing



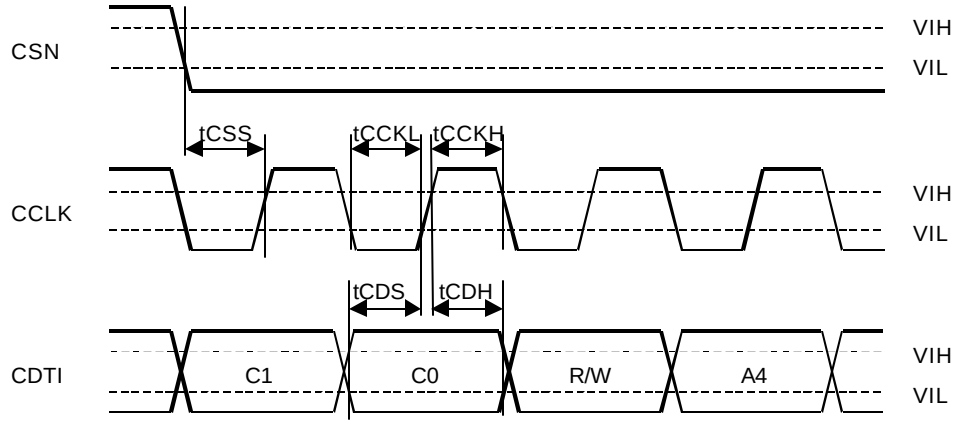
Audio Serial Interface Timing (PCM Mode)



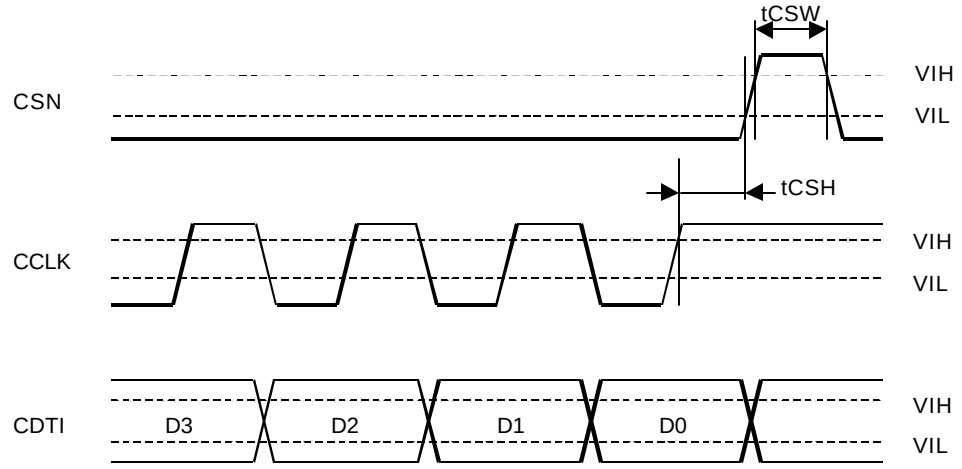
Audio Serial Interface Timing (DSD Normal Mode, DCKB = "0")



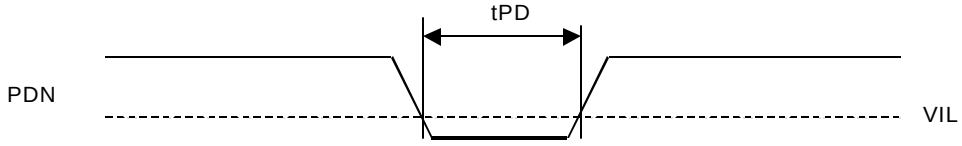
Audio Serial Interface Timing (DSD Phase Modulation Mode, DCKB = "0")



WRITE Command Input Timing



WRITE Data Input Timing



Power-down Timing

OPERATION OVERVIEW

■ D/A Conversion Mode

The AK4357 can perform D/A conversion for both PCM data and DSD data. When DSD mode, DSD data can be input from DCLK, DSDL1-3 and DSDR1-3 pins. When PCM mode, PCM data can be input from BICK, SDTI1-3 and LRCK pins. PCM/DSD mode changes by DSDM pin or D/P bit, DSDM pin setting and D/P bit setting are ORed internal. When PCM/DSD mode changes by DSDM pin or D/P bit, the AK4357 should be reset by RSTN bit, PW bit (PW1=PW2=PD3="0") or PDN pin. It takes about 2/fs to 3/fs to change the mode.

DSDM pin	D/P bit	DAC Output
L	0	PCM
	1	DSD
H	0	DSD
	1	DSD

Table 1. DSD/PCM Mode Control

■ System Clock

1) PCM Mode

The external clocks, which are required to operate the AK4357, are MCLK, LRCK and BICK. The master clock (MCLK) should be synchronized with LRCK but the phase is not critical. The MCLK is used to operate the digital interpolation filter and the delta-sigma modulator. There are two methods to set MCLK frequency. In Manual Setting Mode (ACKS = "0": Register 00H), the sampling speed is set by DFS0/1(Table 2). The frequency of MCLK at each sampling speed is set automatically. (Table 3~5). In Auto Setting Mode (ACKS = "1": Default), as MCLK frequency is detected automatically (Table 6), and the internal master clock becomes the appropriate frequency (Table 7), it is not necessary to set DFS0/1.

All external clocks (MCLK, BICK and LRCK) should always be present whenever the AK4357 is in the normal operation mode (PDN= "H"). If these clocks are not provided, the AK4357 may draw excess current and may fall into unpredictable operation. This is because the device utilizes dynamic refreshed logic internally. The AK4357 should be reset by PDN= "L" after these clocks are provided. If the external clocks are not present, the AK4357 should be in the power-down mode (PDN= "L"). After exiting reset(PDN = "↑") at power-up etc., the AK4357 is in the power-down mode until MCLK is input. DSD interface signals (DCLK, DSDL1-3, DSDR1-3) are fixed to "H" or "L".

DFS1	DFS0	Sampling Rate (fs)		
0	0	Normal Speed Mode	8kHz~48kHz	Default
0	1	Double Speed Mode	60kHz~96kHz	
1	0	Quad Speed Mode	120kHz~192kHz	

Table 2. Sampling Speed (Manual Setting Mode)

LRCK	MCLK				BICK
fs	256fs	384fs	512fs	768fs	64fs
32.0kHz	8.1920MHz	12.2880MHz	16.3840MHz	24.5760MHz	2.0480MHz
44.1kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	2.8224MHz
48.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	3.0720MHz

Table 3. System Clock Example (Normal Speed Mode @Manual Setting Mode)

LRCK	MCLK				BICK
fs	128fs	192fs	256fs	384fs	64fs
88.2kHz	11.2896MHz	16.9344MHz	22.5792MHz	33.8688MHz	5.6448MHz
96.0kHz	12.2880MHz	18.4320MHz	24.5760MHz	36.8640MHz	6.1440MHz

Table 4. System Clock Example (Double Speed Mode @Manual Setting Mode)

LRCK	MCLK		BICK
fs	128fs	192fs	64fs
176.4kHz	22.5792MHz	33.8688MHz	11.2896MHz
192.0kHz	24.5760MHz	36.8640MHz	12.2880MHz

Table 5. System Clock Example (Quad Speed Mode @Manual Setting Mode)

MCLK		Sampling Speed
512fs	768fs	Normal
256fs	384fs	Double
128fs	192fs	Quad

Table 6. Sampling Speed (Auto Setting Mode)

LRCK	MCLK (MHz)						Sampling Speed
fs	128fs	192fs	256fs	384fs	512fs	768fs	
32.0kHz	-	-	-	-	16.3840	24.5760	Normal
44.1kHz	-	-	-	-	22.5792	33.8688	
48.0kHz	-	-	-	-	24.5760	36.8640	
88.2kHz	-	-	22.5792	33.8688	-	-	Double
96.0kHz	-	-	24.5760	36.8640	-	-	
176.4kHz	22.5792	33.8688	-	-	-	-	Quad
192.0kHz	24.5760	36.8640	-	-	-	-	

Table 7. System Clock Example (Auto Setting Mode)

2) DSD Mode

The external clocks, which are required to operate the AK4357, are MCLK and DCLK. The master clock (MCLK) should be synchronized with DSD clock (DCLK) but the phase is not critical. The frequency of MCLK is set by DCKS bit.

All external clocks (MCLK, DCLK) should always be present whenever the AK4357 is in the normal operation mode (PDN= "H"). If these clocks are not provided, the AK4357 may draw excess current because the device utilizes dynamic refreshed logic internally. The AK4357 should be reset by PDN= "L" after threse clocks are provided. If the external clocks are not present, the AK4357 should be in the power-down mode (PDN= "L"). After exiting reset(PDN = "↑") at power-up etc., the AK4357 is in the power-down mode until MCLK is input. PCM interface signals (BICK, LRCK, SDTI1-3) are fixed to "H" or "L".

DCKS	0	1
MCLK	512fs	768fs
DCLK	64fs	64fs

Table 8. System Clock (fs=44.1kHz)

■ Audio Serial Interface Format

1) PCM Mode

When PCM mode, data is shifted in via the SDTI1-3 pins using BICK and LRCK inputs. The DIF0-2 as shown in Table 7 can select five serial data modes . Initial value of DIF0-2 bits is"000", each DIF0-2 bits is ORed with DIF0-2 pins. In all modes the serial data is MSB-first, 2 's compliment format and is latched on the rising edge of BICK. Mode 2 can be used for 16/20 MSB justified formats by zeroing the unused LSBs.

Mode	DIF2	DIF1	DIF0	SDTI Format	BICK	Figure
0	0	0	0	16bit LSB Justified	≥32fs	Figure 1
1	0	0	1	20bit LSB Justified	≥40fs	Figure 2
2	0	1	0	24bit MSB Justified	≥48fs	Figure 3
3	0	1	1	24bit I^2S Compatible	≥48fs	Figure 4
4	1	0	0	24bit LSB Justified	≥48fs	Figure 2

Table 9. Audio Data Formats

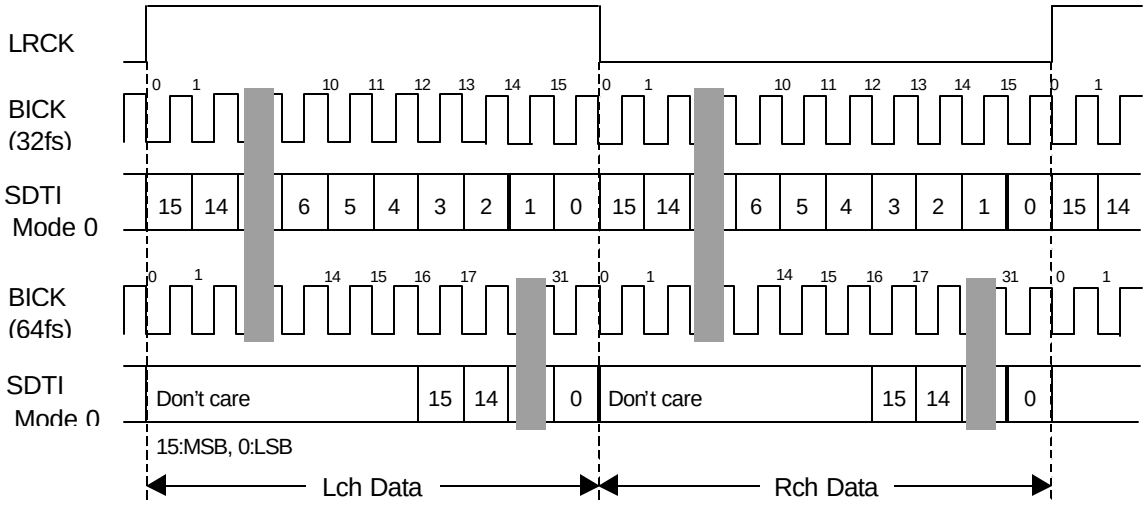


Figure 1. Mode 0 Timing

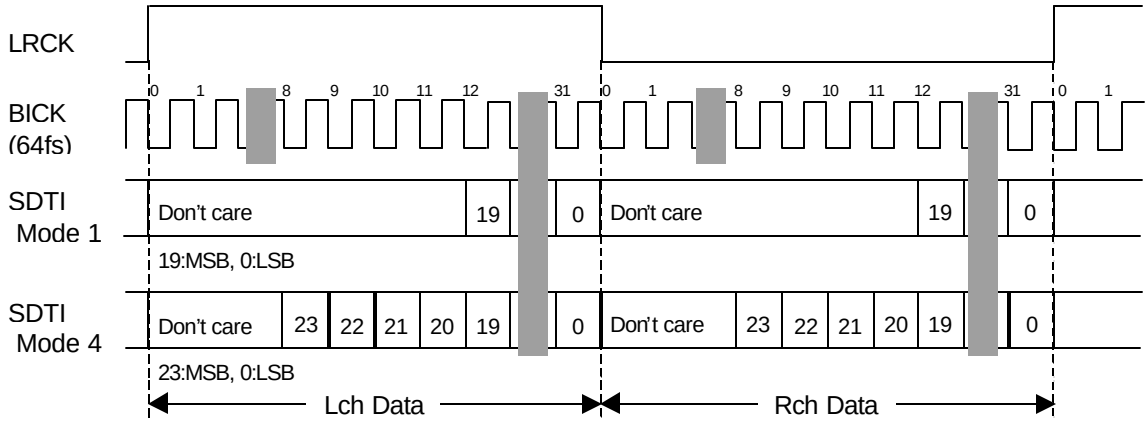


Figure 2. Mode 1,4 Timing

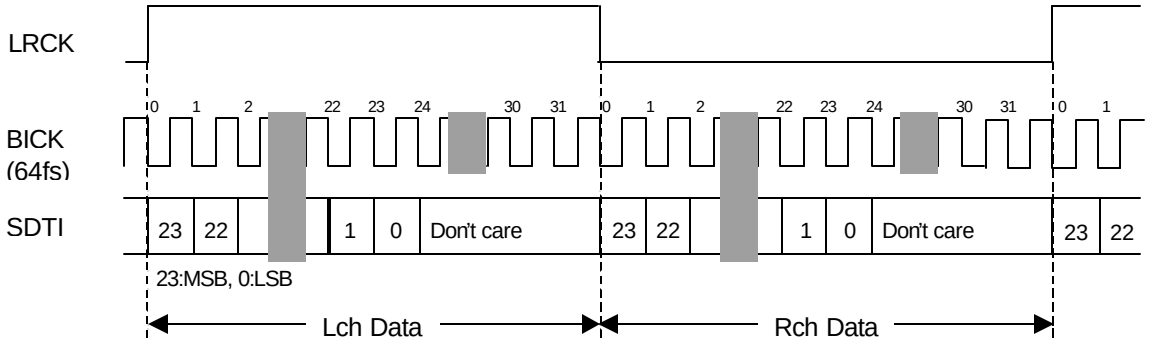


Figure 3. Mode 2 Timing

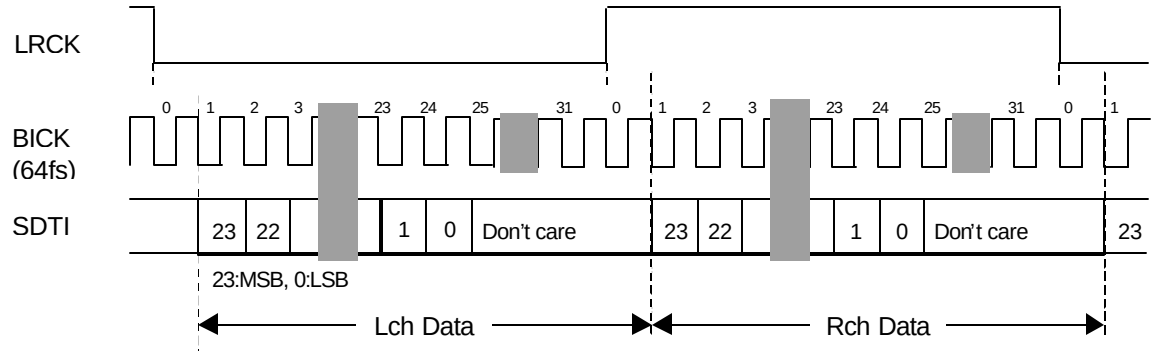


Figure 4. Mode 3 Timing

2) DSD Mode

In case of DSD mode, DIF0-2 are ignored. The frequency of DCLK is fixed to 64fs. DCKB bit can invert the polarity of DCLK.

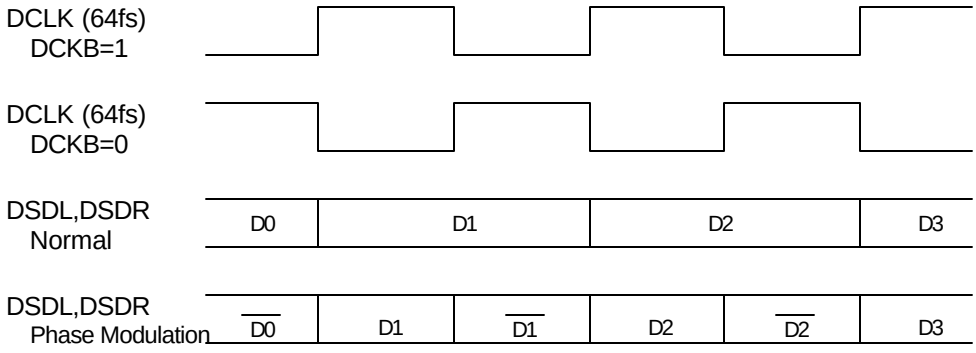


Figure 5. DSD Mode Timing

■ De-emphasis Filter

A digital de-emphasis filter is available for 32, 44.1 or 48kHz sampling rates (tc = 50/15µs) and is enabled or disabled with DEM0 and DEM1. In case of double speed and quad speed mode, the digital de-emphasis filter is always off. When DSD mode, DEM0-1 is invalid.

DEM1	DEM0	Mode	
0	0	44.1kHz	
0	1	OFF	Default
1	0	48kHz	
1	1	32kHz	

Table 8. De-emphasis Filter Control (Normal Speed Mode)

■ Output Volume

The AK4357 includes channel independent digital output volumes (ATT) with 128 levels at 0.5dB steps including MUTE. These volumes are in front of the DAC and can attenuate the input data from 0dB to−63dB and mute. Transition time is set by AST1-0 bits(Table12) When changing levels, transitions are executed via soft changes; thus no switching noise occurs during these transitions.

ATT7-0	Attenuation Level	
FFH	0dB	Default
FEH	-0.5dB	
FDH	-1.0dB	
:	:	
82H	-62.5dB	
81H	-63.0dB	
80H	MUTE (-∞)	
:	:	
02H	MUTE (-∞)	
01H	MUTE (-∞)	
00H	MUTE (-∞)	

Table 11. Attenuation Level of Output Volume

Mode	ATS1	ATS0	ATT speed	
0	0	0	1792/fs	Default
1	0	1	896/fs	
2	1	0	256/fs	
3	1	1	256/fs	

Table 12. Transition time of output volume

In case Mode0, it takes 1792/ fs to transit from FFH(0dB) to 80H(MUTE). In case Mode1, it takes 896/fs to transit from FFH(0dB) to 80H(MUTE). In case Mode2 and 3,it takes 256/fs to transit from FFH(0dB) to 80H (MUTE). If PDN pin goes to "L", ATT7-0 registers are initialized to FFH.ATTN7-0 registers go to FFH when RSTN bit is set to "0". When RSTN bit returns to "1", ATT7-0 registers go to the set value. Digital output volume function is independent of soft mute function.

The setting value of the register is held when switching between PCM mode and DSD mode.

■ Zero Detection

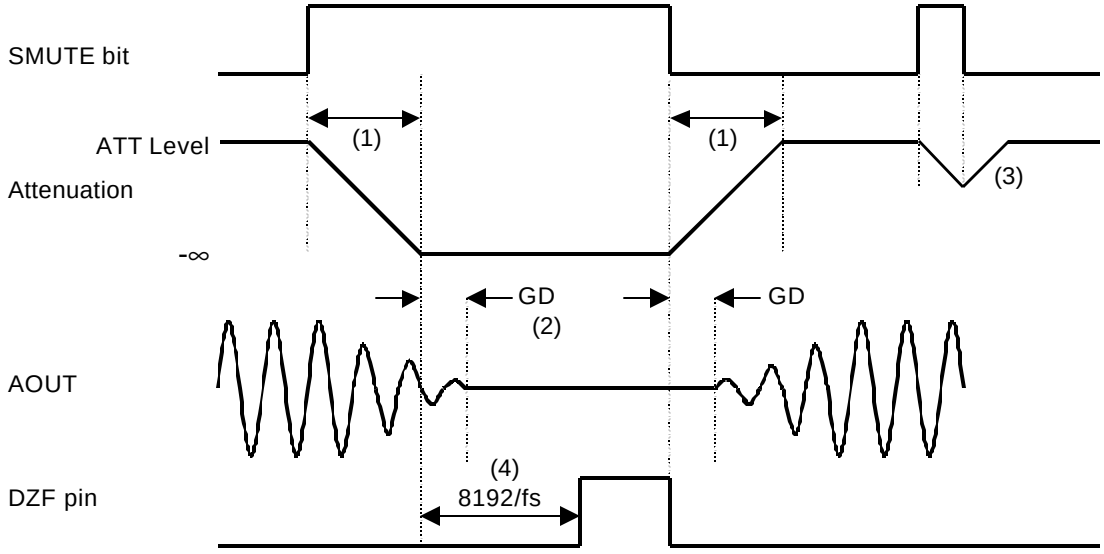
When the input data at all channels are continuously zeros for 8192 LRCK cycles, The AK4357 has Zero Detection like Table 13. DZF pin immediately goes to "L" if input data of each channel is not zero after going DZF "H". If RSTN bit is "0", DZF pin goes to "H". DZF pin goes to "L" at 4~5LRCK if input data of each channel is not zero after RSTN bit returns to "1". Zero detect function can be disabled by DZFE bit. In this case, DZF pins of both channels are always "L". DZFB bit can invert the polarity of DZF pin. When one of PW1-3 bit is set to "0", the input data of DAC which the PW bit is set to "0" should be zero in order to enable zero detection of the other channels. When all PW1-3 bits are set to "0", DZF pin fixes "L". When DZFM bit set to "1", only the input data at all channels are continuously zeros for 8192 LRCK cycles, all DZF pins go to "H".

DZF Pin	Operations
DZFL1	When Lch Data of DAC1 is "0", DZFL1 pin goes "H".
DZFR1	When Rch Data of DAC1 is "0", DZFR1 pin goes "H".
DZF23	When all Lch and Rch Data of DAC2,3 are "0", DZF23 goes "H".

Table 13. DZF pin Operations

■ Soft Mute Operation

Soft mute operation is performed at digital domain. When the SMUTE bit goes to "1", the output signal is attenuated by -∞ during ATT_DATA×ATT transition time (Table 12) from the current ATT level. When the SMUTE bit is returned to "0", the mute is cancelled and the output attenuation gradually changes to the ATT level during ATT_DATA×ATT transition time. If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

(1) ATT_DATA×ATT transition time (Table 12). For example, in Normal Speed Mode, this time is 1792LRCK cycles (1792/fs) at ATT_DATA=128.

(2) The analog output corresponding to the digital input has a group delay, GD.

(3) If the soft mute is cancelled before attenuating to -∞ after starting the operation, the attenuation is discontinued and returned to ATT level by the same cycle.

(4) When the input data at each channel is continuously zeros for 8192 LRCK cycles, DZF pin of each channel goes to "H". DZF pin immediately goes to "L" if input data are not zero after going DZF "H".

Figure 6. Soft Mute and Zero Detection

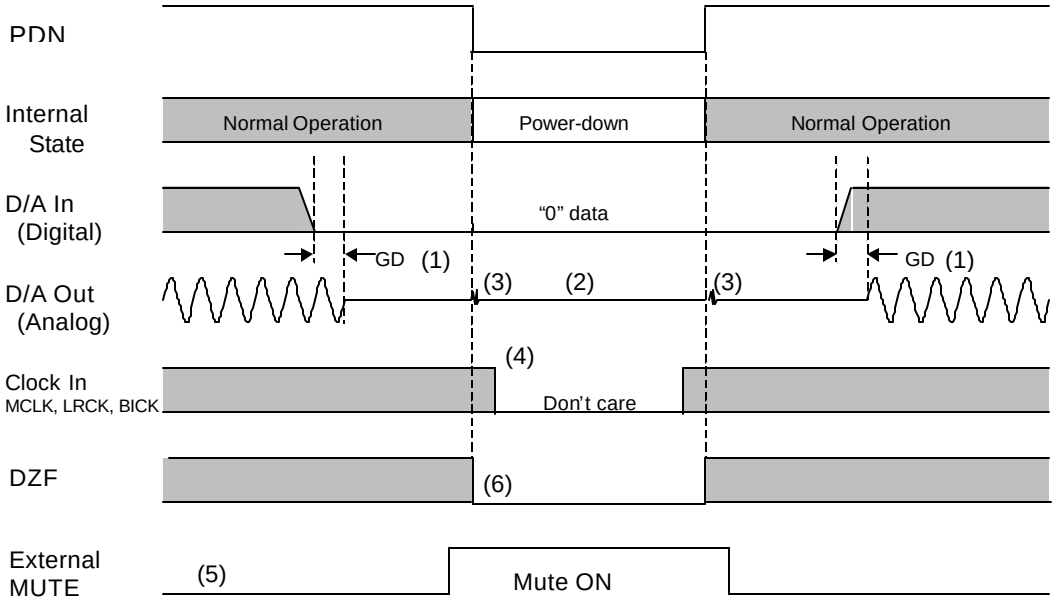
■ System Reset

The AK4357 should be reset once by bringing PDN= "L" upon power-up. The analog section exits power-down mode by MCLK input and then the digital section exits power-down mode after the internal counter counts MCLK during 4/fs.

■ Power-down

The AK4357 is placed in the power-down mode by bringing PDN pin "L" and the anlog outputs are floating (Hi-Z). Figure 6 shows an example of the system timing at the power-down and power-up.

Each DAC can be powered down by each power-down bit (PW1-3) "0". In this case, the internal register values are not initialized and the analog output is Hi-Z. Because some click noise occurs, the analog output should be muted externally if the click noise influences system application.



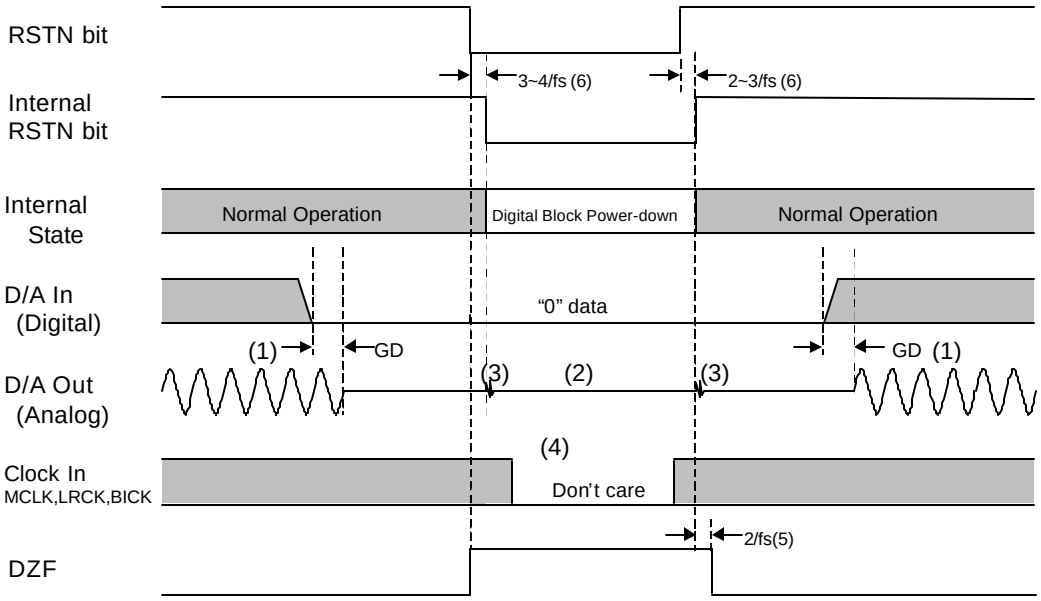
Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs are floating (Hi-Z) at the power-down mode.
(3) Click noise occurs at the edge of PDN signal. This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the power-down mode (PDN = "L").
(5) Please mute the analog output externally if the click noise (3) influence system application.
The timing example is shown in this figure.
(6) DZF pins are "L" in the power-down mode (PDN = "L").

Figure 7. Power-down/up Sequence Example

■ Reset Function

When RSTN=0, DAC is powered down but the internal register values are not initialized. The analog outputs go to VCOM voltage and DZFL/DZFR pins go to "H". Figure 8 shows the example of reset by RSTN bit.



Notes:

(1) The analog output corresponding to digital input has the group delay (GD).
(2) Analog outputs go to VCOM voltage.
(3) Click noise occurs at the edges("↑ ↓") of the internal timing of RSTN bit. This noise is output even if "0" data is input.
(4) The external clocks (MCLK, BICK and LRCK) can be stopped in the reset mode (RSTN = "L").
(5) DZF pins go to "H" when the RSTN bit becomes "0", and go to "L" at 2/fs after RSTN bit becomes "1".
(6) There is a delay, 3~4/fs from RSTN bit "0" to the internal RSTN bit "0", and 2~3/fs from RSTN bit "1" to the internal RSTN "1".

Figure 8. Reset Sequence Example

■ D/A conversion mode switching timing

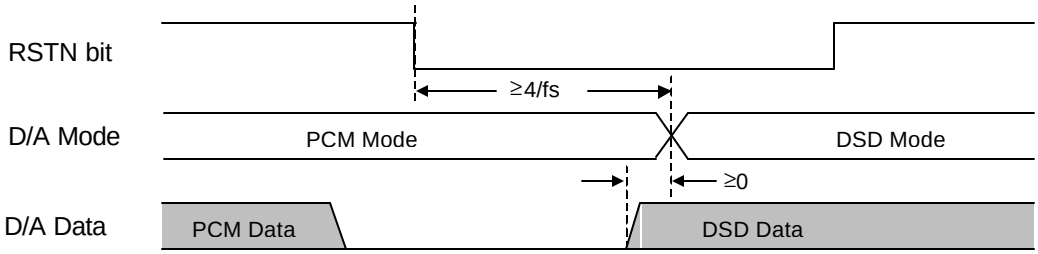


Figure 9. D/A Mode Switching Timing (PCM to DSD)

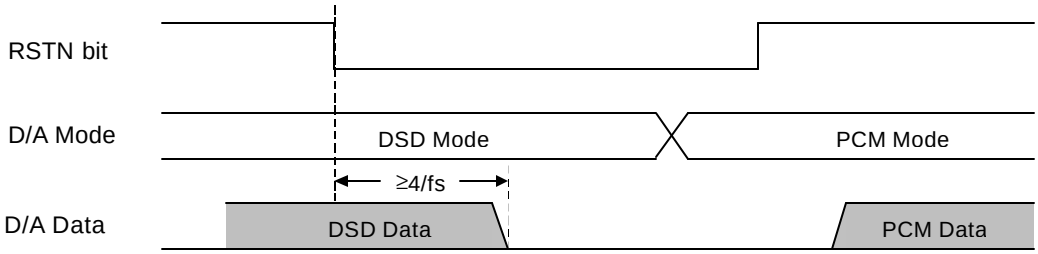


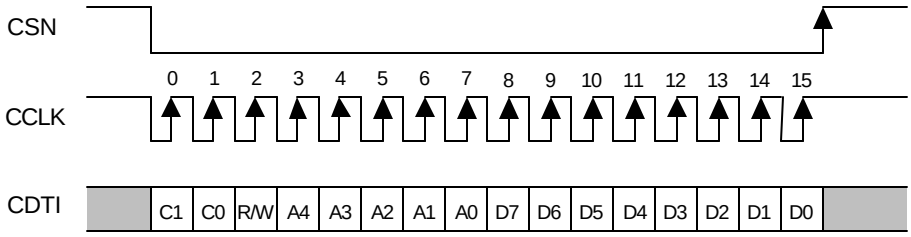
Figure 10. D/A Mode Switching Mode Timing (DSD to PCM)

Caution: In DSD mode, the signal level is ranging from 25% to 75%. Peak levels of DSD signal above this duty are not recommended by SACD format book (Scarlet Book).

■ Mode Control Interface

Internal registers may be written by 3-wire µP interface pins, CSN, CCLK and CDTI. The data on this interface consists of Chip Address (2bits, C1/0; fixed to "01"), Read/Write (1bit; fixed to "1", Write only), Register Address (MSB first, 5bits) and Control Data (MSB first, 8bits). The AK4357 latches the data on the rising edge of CCLK, so data should clocked in on the falling edge. The writing of data becomes valid by CSN "↑". The clock speed of CCLK is 5MHz (max).

PDN = "L" resets the registers to their default values. The internal timing circuit is reset by RSTN bit, but the registers are not initialized.



C1-C0: Chip Address (C1=CAD1, C0=CAD0)
R/W: READ/WRITE (Fixed to "1", Write only)
A4-A0: Register Address
D7-D0: Control Data

Figure 11. Control I/F Timing

*The AK4357 does not support the read command and chip address.
*When the AK4357 is in the power down mode (PDN = "L") or the MCLK is not provided, writing into the control register is inhibited.

■ Register Map

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	SLOW	DZFM	DZFE	DIF2	DIF1	DIF0	RSTN
01H	Control 2	0	0	0	0	0	0	SMUTE	RSTN
02H	Speed & Power Down Control	0	0	DFS1	DFS0	PW3	PW2	PW1	RSTN
03H	De-emphasis Control	0	0	0	0	0	0	DEM1	DEM0
04H	LOUT1 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	ROUT1 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
06H	LOUT2 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
07H	ROUT2 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
08H	LOUT3 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
09H	ROUT3 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
0AH	Control 3	0	0	DCKS	D/P	DCKB	DZFB	ATS1	ATS0

Note: For addresses from 0BH to 1FH, data must not be written.
When PDN goes to "L", the registers are initialized to their default values.
When RSTN bit goes to "0", the only internal timing is reset, and the registers are not initialized to their default values.
All data can be written to the registers even if PW1-3 or RSTN bit is "0".

■ Register Definitions

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
00H	Control 1	ACKS	SLOW	DZFM	DZFE	DIF2	DIF1	DIF0	RSTN
Default		1	0	0	1	0	0	0	1

RSTN: Internal timing reset
0: Reset. All DZF pins go to "H" and any registers are not initialized.
1: Normal operation
When MCLK frequency or DFS changes, the AK4357 should be reset by PDN pin or RSTN bit.

DIF2-0: Audio data interface modes (See Table 9, PCM Only)
Initial: "000", Mode 0
Register bits of DIF2-0 are ORed with the DIF2-0 pins.

DZFE: Data Zero Detect Enable
0: Disable
1: Enable
Zero detect function can be disabled by DZFE bit "0". In this case, the DZF pins are always "L".

DZFM: Data Zero Detect Mode
0: Channel Separated Mode (See table 13.)
1: Channel ANDed Mode
If the DZFM bit is set to "1", all DZF pins go to "H" only when the input data at all channels are continuously zeros for 8192 LRCK cycles.

SLOW: Slow Roll-off Filter Enable (PCM Only)
0: Sharp Roll-off Filter
1: Slow Roll-off Filter

ACKS: Master Clock Frequency Auto Setting Mode Enable
0: Disable, Manual Setting Mode
1: Enable, Auto Setting Mode
Master clock frequency is detected automatically at ACKS bit "1". In this case, the setting of DFS1-0 are ignored. When this bit is "0", DFS1-0 set the sampling speed mode.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
01H	Control 2	0	0	0	0	0	0	SMUTE	RSTN
Default		0	0	0	0	0	0	0	1

RSTN: Internal timing reset
0: Reset. All DZF pins of go to "H" and any registers are not initialized.
1: Normal operation
When MCLK frequency or DFS changes, the AK4357 should be reset by PDN pin or RSTN bit.

SMUTE: Soft Mute Enable
0: Normal operation
1: All DAC outputs soft-muted

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
02H	Speed & Power Down Control	0	0	DFS1	DFS0	PW3	PW2	PW1	RSTN
Default		0	0	0	0	1	1	1	1

RSTN: Internal timing reset
0: Reset. All DZF pins go to "H" and any registers are not initialized.
1: Normal operation
When MCLK frequency or DFS changes, the AK4357 should be reset by PDN pin or RSTN bit.

PW3-1: Power-down control (0: Power-down, 1: Power-up)
PW1: Power down control of DAC1
PW2: Power down control of DAC2
PW3: Power down control of DAC3
All sections are powered-down by PW1=PW2=PW3=0.

DFS1-0: Sampling speed control (See Table 2, PCM Only)
00: Normal speed
01: Double speed
10: Quad speed
When changing between Normal/Double Speed Mode and Quad Speed Mode, some click noise occurs.

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
03H	De-emphasis Control	0	0	0	0	0	0	DEM1	DEM0
Default		0	0	0	0	0	0	0	1

DEM1-0: De-emphasis response control for DAC1/2/3 data on SDTI1/2/3/ (See Table 10, PCM only)
Initial: "01", OFF

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
04H	LOUT1 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
05H	ROUT1 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
06H	LOUT2 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
07H	ROUT2 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
08H	LOUT3 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
09H	ROUT3 ATT Control	ATT7	ATT6	ATT5	ATT4	ATT3	ATT2	ATT1	ATT0
Default		1	1	1	1	1	1	1	1

ATT7-0: Attenuation Level
128 levels, 0.5dB step (See Table 11)

Addr	Register Name	D7	D6	D5	D4	D3	D2	D1	D0
0AH	Control 3	0	0	DCKS	D/P	DCKB	DZFB	ATS1	ATS0
Default		0	0	0	0	0	0	0	0

ATS1-0: DATT Speed Setting (See Table 12)
Initial: "00", mode 0

DZFB: Inverting Enable of DZF
0: DZF goes "H" at Zero Detection
1: DZF goes "L" at Zero Detection

DCKB: Polarity of DCLK (DSD Only)
0: DSD data is output from DCLK falling edge
1: DSD data is output from DCLK rising edge

D/P: DSD/PCM Mode Select
0: PCM Mode. SCLK, SDTI1-3, LRCK
1: DSD Mode. DCLK, DSDL1-3, DSDR1-3
D/P bit is ORed with the DSDM pin. When D/P changes, the AK4357 should be reset by PDN pin, PW bit or RSTN bit.

DCKS: Master Clock Frequency Select at DSD mode (DSD only)
0: 512fs
1: 768fs

SYSTEM DESIGN

Figure 12 shows the system connection diagram. An evaluation board (AKD4357) is available in order to allow an easy study on the layout of a surrounding circuit.

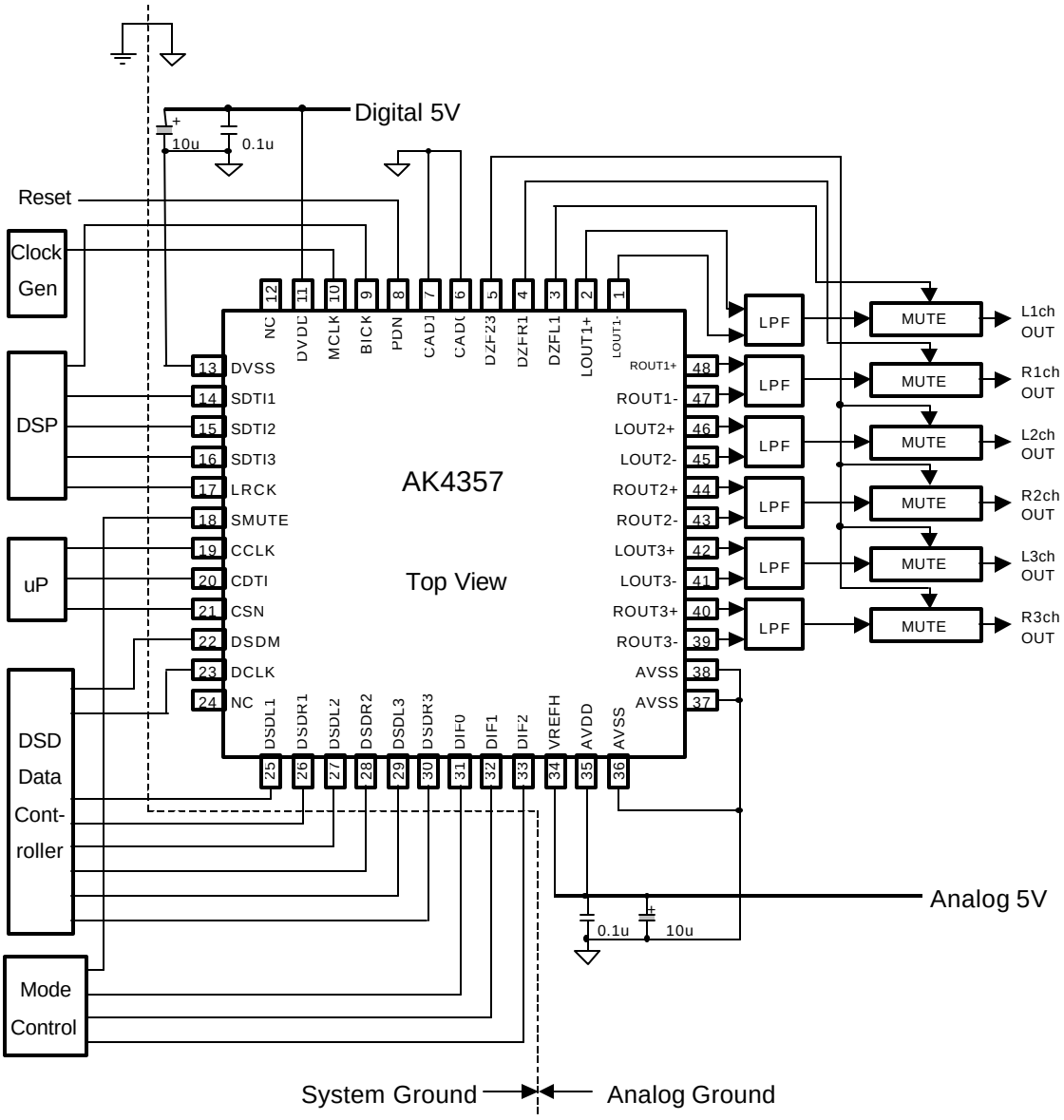


Figure 12. Typical Connection Diagram

Notes:

- LRCK = fs, BICK = 64fs.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.
- All input pins except pull-down pins should not be left floating.

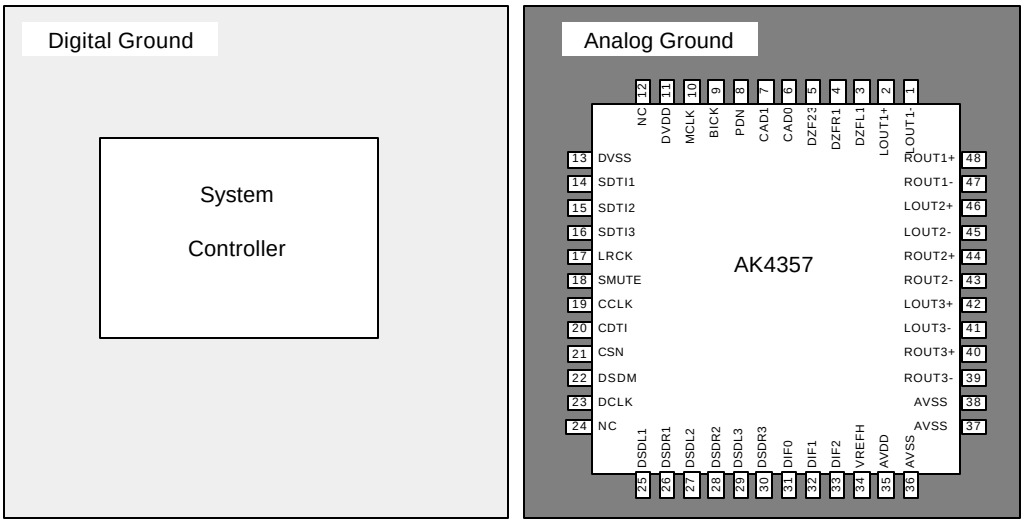


Figure 13. Ground Layout

1. Grounding and Power Supply Decoupling

AVDD and DVDD are usually supplied from analog supply in system and should be separated from system digital supply. Alternatively if AVDD and DVDD are supplied separately, the power up sequence is not critical. **AVSS and DVSS of the AK4357 must be connected to analog ground plane**. System analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitor, especially 0.1µF ceramic capacitor for high frequency should be placed as near to AVDD and DVDD as possible.

2. Voltage Reference

VREFH sets the analog output range. VREFH pin is normally connected to AVDD with a 0.1µF ceramic capacitor. All signals, especially clocks, should be kept away from the VREFH pin in order to avoid unwanted coupling into the AK4357.

3. Analog Outputs

The analog outputs are full-differential outputs and 0.5 x VREFH Vpp (typ) centered around the internal common voltage (about AVDD/2). The differential outputs are summed externally, V_{AOUT}=(AOUT+)-(AOUT-) between AOUT+ and AOUT-. If the summing gain is 1, the output range is 5.0Vpp (typ @VREFH=5V). The bias voltage of the external summing circuit is supplied externally. The input data format is 2's complement. The output voltage(V_{AOUT}) is a positive full scale for 7FFFFF (@24bit) and a negative full scale for 800000H (@24bit). The ideal V_{AOUT} is 0V for 000000H (@24bit).

The internal switched-capacitor filter and external low pass filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. DC offset on AOUT+/- is eliminated without AC coupling since the analog outputs are differential.

4. External Analog Filter

It is recommended by SACD format book (Scarlet Book) that the filter response at SACD playback is an analog low pass filter with a cut-off frequency of maximum 50kHz and a slop of minimum 30dB/Oct. The AK4357 can achieve this filter response by combination of the internal filter (Table 14) and an external filter (Figure 14).

Frequency	Gain
20kHz	-0.4dB
50kHz	-2.8dB
100kHz	-15.5dB

Table 14. Internal Filter Response at DSD mode

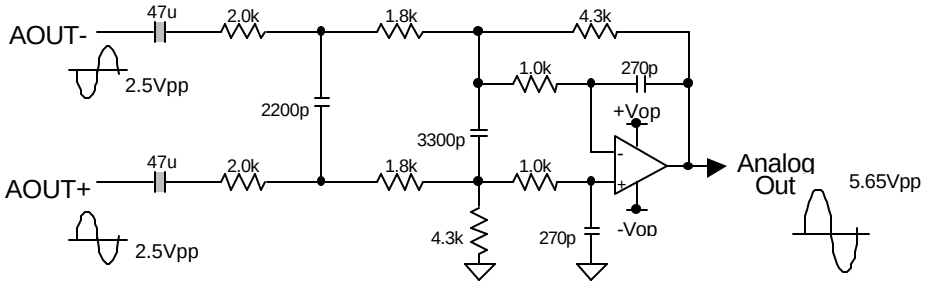


Figure 14. External 3rd order LPF Circuit Example

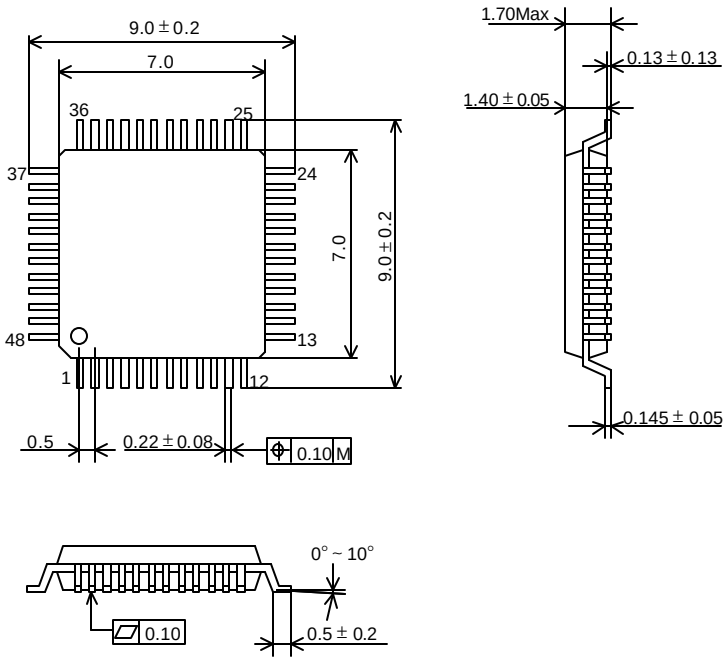
Frequency	Gain
20kHz	-0.05dBr
50kHz	-0.51dBr
100kHz	-16.8dBr

DC gain = 1.07dB

Table 15. 3rd order LPF (Figure 14) Response

PACKAGE

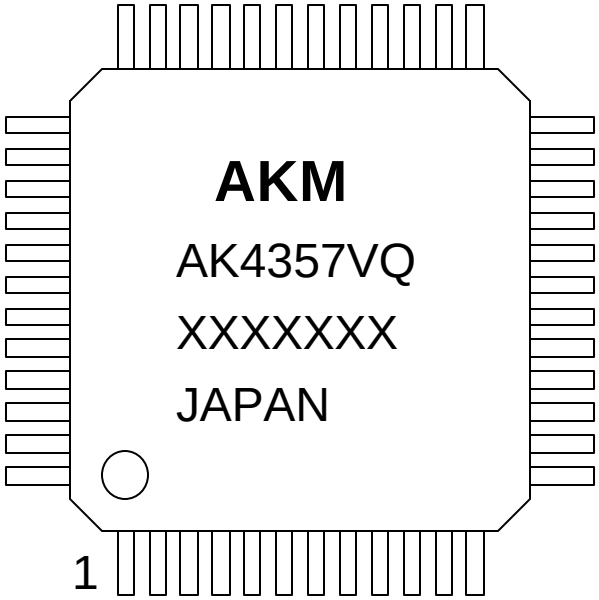
48pin LQFP(Unit:mm)



■ **Package & Lead frame material**

Package molding compound:	Epoxy
Lead frame material:	Cu
Lead frame surface treatment:	Solder (Pb free) plate

MARKING



1) Asahi Kasei Logo
2) Marking Code: AK4357VQ
3) Date Code: XXXXXXX(7 digits)
4) Country of Origin
5) Pin #1 indication