NEC

MOS INTEGRATED CIRCUIT
μPD70F3461

V850E/CAG4-M
32-Bit Single-Chip Microcontroller

DESCRIPTION

This device is a new, powerful NEC 32-bit RISC microcontroller with embedded FlexRay communication interface. With its high performance, large memory size and fully-fledged communication interfaces it is especially well suited for high end gateway and other body applications in the automotive area. This microcontroller extends the widely used NEC V850 family into the high performance range and supports with its FlexRay interface and the MediaLB™ interface the upcoming new standards for communication inside automotive.It is optimized for gateway applications featuring control of up to 6 CAN as standard interfaces in the automotive area. With the embedded MediaLB™ interface this device opens a new possibility to connect to the MOST® world, offering a very high data throughput espc. for asynchronous data transfer. The Timer structure is suitable for most body applications by offering high number of input capture and PWM outputs. The new Multi LIN Master macro can connect all 6 LIN channel in a very efficient way, with a minimum CPU interaction. With these features the device fits also to many body applications.

FEATURE

- 32-bit RISC CPU with Harvard Architecture
  - Floating Point Unit
- Internal Flash: 512 KB
- Internal RAM: 60 KB
- Data Flash: 32 KB
- Advanced Safety features
  - CRC modul
- FlexRay:
  - Bosch Eray V.2.1
  - 2 channel
- Full-CAN Interface: 6 channel
- 3-wire MediaLB interface
- Multi LIN Master
- Serial Interfaces: 11 channels
  - 3-wire mode: 4 channels
  - UART mode: 6 channels (LIN compatible)
  - I²C mode: 1 channel
- Timers: 9 channels
  - 16-bit capture/compare timer: 7 channel
  - Watch timer: 1 channel
  - Window Watchdog timer: 1 channel
  - Motor Control: 1 channel
- Non multiplexed 16 bit businterface
- 10-bit resolution A/D Converter: 10 channel
- I/O lines: 105
- External Interrupts: 15 + NMI
- Power supply voltage range:
  - Isolated Area: +4.5V to +5.5V
  - Main Area: +3.0 V to +3.6 V
- Frequencies:
  - Main CPU frequency: 80 MHz
  - Main OSC: 16MHz
  - Sub clock: 32KHz
  - Low-frequency internal oscillator:
    - 240KHz (-50 / +100%)
  - High-speed internal oscillator:
    - 6.8 MHz
- Power save mode support functionality
- Temperature range:
  - -40°C to +105°C
- μPD70F3461
- Package:
  - 144-pin plastic QFP, 0.5 mm pin-pitch (20 × 20 mm)

ORDERING INFORMATION

Device	Part Number	Package	Flash	RAM
V850E/CAG4-M	μPD70F3461	LQFP144 20 × 20 mm	512 KB	60 KB

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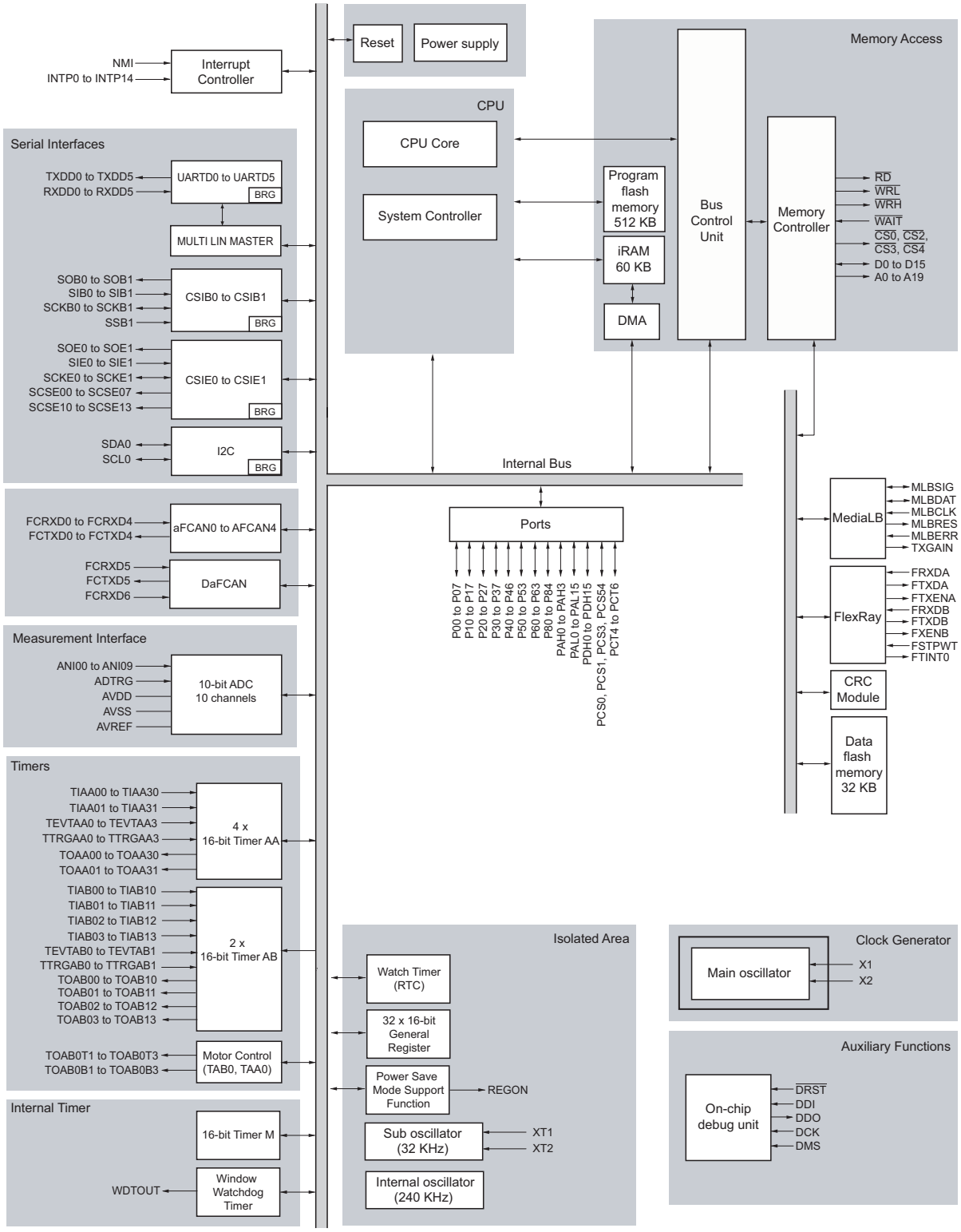
INTERNAL BLOCK DIAGRAM OF V850E/CAG4-M - μPD70F3461

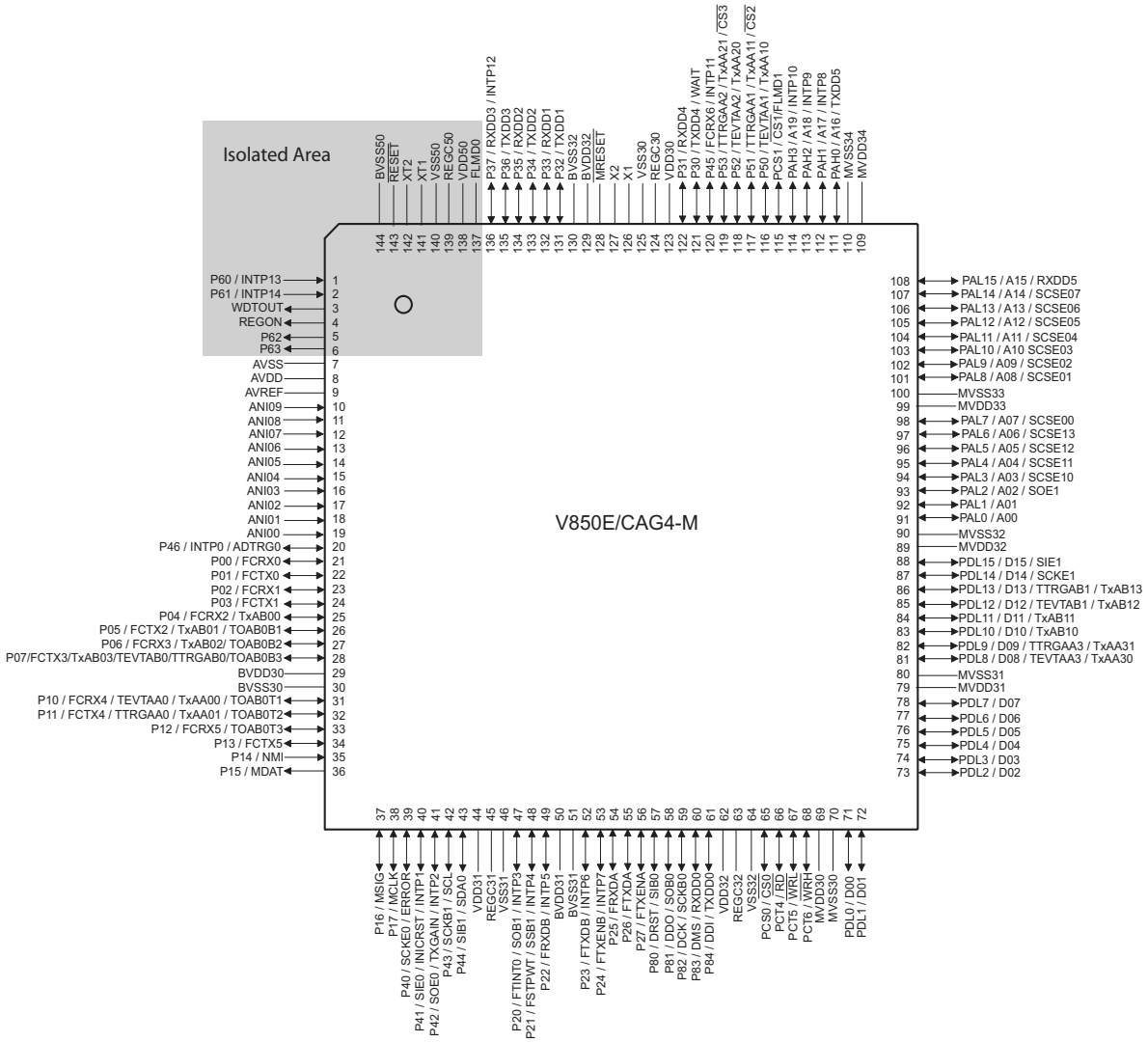


PIN IDENTIFICATION

A00-A19	External memory interface address bus
ADTRG0	ADC trigger input
ANI00-ANI09	ADC input
AVDD	ADC power supply
AVREF	ADC reference voltage
AVSS	Analog ground
BVDD30-BVDD32	3V I/O port supply voltage
BVSS30-BVSS32	3V I/O port ground
BVSS50	5V Isolated Area Ground
$\overline{CS0}$-$\overline{CS3}$	Ext. memory interface chip select signals
D00-D15	External memory interface data bus
DCK	N-Wire interface clock
DDI	N-Wire I/F debug data input
DDO	N-Wire interface debug data output
DMS	N-Wire I/F debug mode select input
$\overline{DRST}$	N-Wire debug interface reset
ERROR	MediaLB external ERROR status input
FCRX0-FCRX6	CAN0-CAN6 Receive Data
FCTX0-FCTX5	CAN0-CAN5 Transmit Data
FLMD0	Flash writing control
FLMD1	Mode control 1
FRXDA-FRXDB	FlexRay channel A&B receive data
FSTPWT	Interrupt signal from external FlexRay
FTINT0	Interrupt signal from internal FlexRay
FTXDA-FTXDB	FlexRay channel A&B transmit data
FTXENA-FTXENB	FlexRay channel A&B transmit perm.
ICL	IIC clock
IDAT	IIC data
INICRST	MediaLB RESET output
INTP0-INP14	External interrupts
MCLK	MediaLB clock input
MDAT	MediaLB data
$\overline{MRESET}$	Main Area RESET input
MSIG	MediaLB signal
MVDD	Memory interface power supply
MVSS	memory interface ground
NMI	Non-maskable interrupt
P60-P61	Isolated Area Wake-Up input
P62-P63	Isolated Area Output
$\overline{RD}$	External memory interface read strobe
REGC30-REGC32	3V Regulator Output
REGC50	5V Isolated Area Regulator output
REGON	Isolated Area Power Save Mode Control
$\overline{RESET}$	Isolated Area RESET input
RXDD0-RXDD5	UARTD0-UARTD5 receive data
SCKB0-SCKB1	Serial Interface CSIB0-CSIB1 clock line
SCKE0-SCKE1	Serial Interface CSIE0-CSIE1 clock line
SCSCE00-SCSCE07	CSIE0 chip select
SCSCE10-SCSCE13	CSIE1 chip select
SIB0-SIB1	CSIB0-CSIB1 data input
SIE0-SIE1	CSIE0-CSIE1 data input
SOB0-SOB1	CSIB0-CSIB1 data output
SOE0-SOE1	CSIE0-CSIE1 data output
SSB1	CSIB1 slave select input
TEVTAA0-TEVTAA3	Timer TAA0-TAA3 event input
TEVTAB0-TEVTAB1	Timer TAB0-TAB1 event input
TIAA00-TIAA30	Timer TAA00-TAA30 capture trigger
TIAA01-TIAA31	Timer TAA01-TAA31 capture trigger
TIAB00 - TIAB03	Timer TAB0 capture trigger input
TIAB10 - TIAB13	Timer TAB1 capture trigger input
TOAA00-TOAA30	Timer TAA00-TAA30 pulse signal output
TOAA01-TOAA31	Timer TAA00-TAA30 pulse signal output
TOAB00- TOAB03	Timer TAB0 pulse signal output
TOAB10- TOAB13	Timer TAB1 pulse signal output
TOAB0B1 - TOAB0B3	Motor Control ouput signal
TOAB0T1 - TOAB0T3	Motor Control ouput signal
TTRGAA0-TTRGAA3	Timer TAA0-TAA3 trigger input
TTRGAB0-TTRGAB1	Timer TAB0-TAB1 trigger input
TXDD0-TXDD5	UARTD0-UARTD5 transmit data
TXGAIN	MediaLB FOT TxGAIN output
VDD30-VDD32	3V Main Supply Voltage
VDD50	5V Isolated Area Supply Voltage
VSS30-VSS32	3V Main Ground
VSS50	5V Isolated Area Ground
$\overline{WAIT}$	Ext. memory interface data wait request
WDTOUT	Isolated Area Watchdog Timer Status
$\overline{WRH}$	Ext. memory interface write high strobe
$\overline{WRL}$	Ext. memory interface write high strobe
X1-X2	Main oscillator terminals
XT1-XT2	Subclock oscillator terminals

PIN CONFIGURATION

- 144-Pin Plastic LQFP (fine pitch) (20 mm × 20 mm) (Top View)



Pin Functions

Port group name	Port name	Alternative outputs	Alternative inputs	Pin group	Pin location
6[a]	P60	-	P60 / INTP13	10	1
	P61	-	P61 / INTP14		2
a		WDTOUT	-		3
		REGON	-		4
6[a]	P62	P62	-		5
	P63	P63	-		6
		-	AVSS		7
		-	AVDD		8
		-	AVREF		9
		-	ANI09	8	10
		-	ANI08		11
		-	ANI07		12
		-	ANI06		13
		-	ANI05		14
		-	ANI04		15
		-	ANI03		16
		-	ANI02		17
		-	ANI01		18
		-	ANI00		19
4	P46	-	AADTRG0 / INTP0	1A	20
0	P00	-	FCRX0		21
	P01	FCTX0	-		22
	P02	-	FCRX1		23
	P03	FCTX1	-		24
	P04	TOAB00	FCRX2 / TIAB00		25
	P05	FCTX2 / TOAB01 / TOAB0B1	TIAB01		26
	P06	TOAB02 / TOAB0B2	FCRX3 / TIAB02 / TEVTAB0		27
	P07	FCTX3 / TOAB03 / TOAB0B3	TIAB03 / TTRGAB0		28
		-	BVDD30		29
		-	BVSS30		30
1	P10	TOAA00 / TOAB0T1	FCRX4 / TIAA00 / TEVTAA0	1A	31
	P11	FCTX4 / TOAA01 / TOAB0T2	TIAA01 / TTRGAA0		32
	P12	TOAB0T3	FCRX5		33
	P13	FCTX5	-		34
	P14	-	NMI		35
	P15	MDAT	MDAT	2	36
	P16	MSIG	MSIG		37
	P17	-	MCLK		38

Port group name	Port name	Alternative outputs	Alternative inputs	Pin group	Pin location
4	P40	SCKE0	SCKE0 / ERROR	1B	39
	P41	INICRST	SIE0 / INTP1		40
	P42	SOE0/TXGAIN	INTP2		41
	P43	SCKB1 / ICL	ICL		42
	P44	IDAT	SIB1 / IDAT		43
		-	VDD31		44
		REGC31	-		45
		-	VSS31		46
2	P20	SOB1	FTINT0 / INTP3	3	47
	P21	-	FSTPWT / SSB1 / INTP4		48
	P22	-	FRXDB / INTP5		49
		-	BVDD31		50
		-	BVSS31		51
2	P23	FTXDB	INTP6	3	52
	P24	FTXENB	INTP7		53
	P25	-	FRXDA		54
	P26	FTXDA	-		55
	P27	FTXENA	-		56
8	P80[b]	-	DRST / SIB0	6	57
	P81	DDO / SOB0	-	1B	58
	P82	SCKB0	DCK / SCKB0		59
	P83	-	DMS / RXDD0		60
	P84	TXDD0	DDI		61
		-	VDD32		62
		REGC32	-		63
		-	VSS32		64
CS	PCS0	$\overline{CS0}$	-	5A	65
CT	PCT4	$\overline{RD}$	-		66
	PCT5	$\overline{WRL}$	-		67
	PCT6	$\overline{WRH}$	-		68
		-	MVDD30		69
		-	MVSS30		70
DL	PDL0	D00	D00	5A	71
	PDL1	D01	D01		72
	PDL2	D02	D02		73
	PDL3	D03	D03		74
	PDL4	D04	D04	5B	75
	PDL5	D05	D05		76
	PDL6	D06	D06		77
	PDL7	D07	D07		78

Port group name	Port name	Alternative outputs	Alternative inputs	Pin group	Pin location
		-	MVDD31		79
		-	MVSS30		80
DL	PDL8	D08 / TOAA30	D08 / TIAA30 / TEVTAA3	5B	81
	PDL9	D09 / TOAA31	D09 / TIAA31 / TTRGAA3		82
	PDL10	D10 / TOAB10	D10 / TIAB10		83
	PDL11	D11 / TIAB11	D11 / TOAB11		84
	PDL12	D12 / TOAB12	D12 / TIAB12 / TEVTAB1	5C	85
	PDL13	D13 / TOAB13	D13 / TIAB13 / TTRGAB1		86
	PDL14	D14 / SCKE1	D14 / SCKE1		87
	PDL15	D15	D15 / SIE1		88
		-	MVDD32		89
		-	MVSS32		90
AL	PAL0	A00	-	5C	91
	PAL1	A01	-		92
	PAL2	A02 / SOE1	-		93
	PAL3	A03 / SCSE10	-		94
	PAL4	A04 / SCSE11	-	5D	95
	PAL5	A05 / SCSE12	-		96
	PAL6	A06 / SCSE13	-		97
	PAL7	A07 / SCSE00	-		98
		-	MVDD33		99
		-	MVSS33		100
AL	PAL8	A08 / SCSE01	-	5D	101
	PAL9	A09 / SCSE02	-		102
	PAL10	A10 / SCSE03	-		103
	PAL11	A11 / SCSE04	-		104
	PAL12	A12 / SCSE05	-	5E	105
	PAL13	A13 / SCSE06	-		106
	PAL14	A14 / SCSE07	-		107
	PAL15	A15	RXDD5		108
		-	MVDD34		109
		-	MVSS34		110
AH	PAH0	A16 / TXDD5	-	5E	111
	PAH1	A17	INTP8		112
	PAH2	A18	INTP9		113
	PAH3	A19	INTP10		114
CS	PCS1	$\overline{CS1}$	FLMD1		115
5	P50	TOAA10	TIAA10 / TEVTAA1	1C	116
	P51	TOAA11 / $\overline{CS2}$	TIAA11 / TTRGAA1		117
	P52	TOAA20	TIAA20 / TEVTAA2		118
	P53	TOAA21 / $\overline{CS3}$	TIAA21 / TTRGAA2		119

Port group name	Port name	Alternative outputs	Alternative inputs	Pin group	Pin location
4	P45	-	INTP11 / FCRX6	1C	120
3	P30	TXDD4	$\overline{\text{WAIT}}$		121
	P31	-	RXDD4		122
		-	VDD30		123
		REGC30	-		124
		-	VSS30		125
		-	X1	7	126
		-	X2		127
		-	$\overline{\text{MRESET}}$	4	128
		-	BVDD32		129
		-	BVSS32		130
3	P32	TXDD1	-	1C	131
	P33	-	RXDD1		132
	P34	TXDD2	-		133
	P35	-	RXDD2		134
	P36	TXDD3	-		135
	P37	-	RXDD3 / INPT12		136
a		-	FLMD0	13	137
		-	VDD50		138
		REGC50	-		139
		-	VSS50		140
		-	XT1	12	141
		-	XT2		142
		-	$\overline{\text{RESET}}$	11	143
		-	BVSS50		144

a. Grey marked cells are located on the Isolated Area
b. P80 is an input only pin

Table of Contents

1. Electrical Specification : General

1.1 Absolute Maximum Ratings

T_A = -40 ~ 105°C,
Operation Modes: All
Duration: 15years
$V_{SS5x} = CV_{SS} = V_{SS3x} = AV_{SS0} = MV_{SS3X} = 0V$

Table 1-1: Absolute Maximum Ratings (1/2)

Parameter		Symbol	Test Conditions		Ratings	Unit
Supply voltage		V_{DD50}			-0.5 to +6.5	V
		V_{DD3X}			-0.5 to +4.6	V
		AV_{DD}			-0.5 to +4.6	V
		AV_{REF}			-0.5 to +4.6	V
		MV_{DD3}			-0.5 to +4.6	V
		BV_{DD3}			-0.5 to +4.6	V
		AV_{SS}			-0.5 to +0.5	V
		BV_{SS3}			-0.5 to +0.5	V
		BV_{SS5}			-0.5 to +0.5	V
		MV_{SS3}			-0.5 to +0.5	V
Input voltage	Group 1 to 4, 6	V_{I1}	$V_{I1} < BV_{DD3}+0.5V$		-0.5 to +4.6	V
	Group 5	V_{I5}	$V_{I5} < MV_{DD3}+0.5V$		-0.5 to +4.6	V
	Group 10, 11, 13	V_{IIA}	$V_{IIA} < V_{DD5}+0.5V$		-0.5 to +6.5	V
Analog input voltage	Group 8	V_{IAD}	$V_{IAD} < AV_{DD}+0.3V$ $V_{IAD} < AV_{REF}+0.3V$ $V_{IAD} > AV_{SS}-0.3V$		-0.5 to +4.6	V
Output voltage	Group 1 to 8	V_{O1}			-0.5 to +4.6	V
	Group 10	V_{O2}			-0.5 to +6.5	V
Operating ambient temperature		T_A	Normal operating mode		-40 to +105	°C
Storage temperature		T_{STGB}			-40 to +125	°C

Table 1-1: Absolute Maximum Ratings (2/2)

Parameter		Symbol	Test Conditions		Ratings	Unit
High level output current	Group 1	I_{OH13}		1 pin	-3.0	mA
	Group 1A	I_{OHA1A}		Total	-20	mA
	Group 1B	I_{OHA1B}		Total	-20	mA
	Group 1B	I_{OHA1C}		Total	-20	mA
	Group 2	I_{OH2}		1 pin	-6.0	mA
	Groups 1A & 2	I_{OHA1A2}		Total	-20.0	mA
	Group 3	I_{OH3}		1 pin	-3	mA
	Groups 1B & 3	I_{OHA1B3}		Total	-20	mA
	Groups 1,2 & 3	I_{OHA123}		Total	-60	mA
	Groups 5	I_{OH5}		1 pin	-3	mA
	Group 5A	I_{OHA5A}		Total	-20	mA
	Group 5B	I_{OHA5B}		Total	-20	mA
	Group 5C	I_{OHA5C}		Total	-20	mA
	Group 5D	I_{OHA5D}		Total	-20	mA
	Group 5E	I_{OHA5E}		Total	-20	mA
	Group 5	I_{OHA5}		Total	-100	mA
	Group 10	I_{OH10}		1 pin	-3	mA
	Group 10	I_{OHA10}		Total	-20	mA
Low level output current	Group 1	I_{OL13}		1 pin	3.0	mA
	Group 1A	I_{OLA1A}		Total	20	mA
	Group 1B	I_{OLA1B}		Total	20	mA
	Group 1B	I_{OLA1C}		Total	20	mA
	Group 2	I_{OL2}		1 pin	6.0	mA
	Groups 1A & 2	I_{OLA1A2}		Total	20.0	mA
	Group 3	I_{OL3}		1 pin	3	mA
	Groups 1B & 3	I_{OLA1B3}		Total	20	mA
	Groups 1,2 & 3	I_{OLA123}		Total	60	mA
	Groups 5	I_{OL5}		1 pin	3	mA
	Group 5A	I_{OLA5A}		Total	20	mA
	Group 5B	I_{OLA5B}		Total	20	mA
	Group 5C	I_{OLA5C}		Total	20	mA
	Group 5D	I_{OLA5D}		Total	20	mA
	Group 5E	I_{OLA5E}		Total	20	mA
	Group 5	I_{OLA5}		Total	100	mA
	Group 10	I_{OL10}		1 pin	3	mA
	Group 10	I_{OLA10}		Total	20	mA

Cautions: 1. Do not directly connect output (or I/O) pins of IC products to each other, or to V_{DD}, V_{SS}, and GND.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions shown below for DC characteristics and AC characteristics are within the range for normal operation and quality assurance.

1.1.1 Injected Current Absolute Maximum Ratings

T_A =-40 to +105°C

Table 1-2: Injected Current: Abdolute Maximum Ratings

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Positive overload current $V_{IN} > XV_{DDnx}$[a]	I_{INJPM}	Digital input pins	Per pin			4	mA
			Total V_{DDmx}[b]			100	mA
		Analog input pins	Per pin			4	mA
			Total AV_{DD}			9	mA
Positive overload current $V_{IN} < XV_{SSnx}$[c]	I_{INJnM}	Digital input pins	Per pin			-4	mA
			Total V_{DDmx}[b]			-100	mA
		Analog input pins	Per pin			-4	mA
			Total AV_{DD}			-9	mA

a. XV_{DDnx}: either BV_{DD3x} with x = 0 to 2, MV_{DD3x} with x = 0 to 4 or AV_{DD}.
b. V_{DDmx}: either V_{DD3x} with x = 0 to 2 or V_{DD50}
c. $XV_{SSnx:}$ either BV_{SS3x} with x = 0 to 2, MV_{SS3x} with x = 0 to 4, BV_{SS50} or AV_{SS}

Cautions: 1. The total current includes the ouput current.

2. Product quality may suffer if the absolute maximum ratings are exceeded even momentarily for any parameter.

1.2 Capacitance connected to REGCx

The device requires to connect capacitors with the following parameters to each of the pins REGC30, REGC31, REGC32 and REGC50 individually.

Table 1-3: External Capacitance Requirements for REGCX

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Capacitance	C_{REG}		3.3	4.7	10.0	µF
ESR of capacitance	C_{ESR}	F0 = 100KHz			0.6	Ω

Note: The pins REGC30, REGC31, REGC32 and REGC50 must not be loaded externally

1.3 I/O Capactitances

Ta =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 1-4: I/O Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	fC = 1MHz unmeasured pins returned to 0			10	pF
Input/output capacitance, all I/O pins	C_{IO}				15	pF

2. Electrical Specification : Device Clock Specifications

2.1 Main Oscillator Characteristics

Ta =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

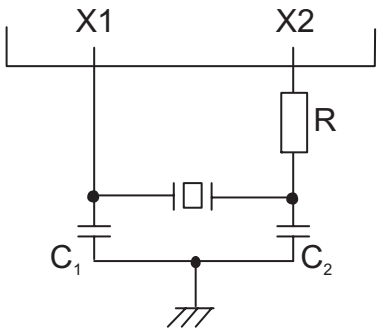


Figure 2-1: Main Oscillator Recommendations

Remark: Values of capacitors C_1, C_2 and the resistor R depend on used crystal and must be specified in cooperation with the manufacturer.

Cautions:
1. **External clock input is prohibited.**
2. **Wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.**
   - **Place the oscillation circuit as close as possible to X1 and X2 pins.**
   - **Keep the wiring length as short as possible.**
   - **Do not cross the wiring with the other signal lines.**
   - **Do not route the wiring near a signal line through which a high fluctuating current flows.**
   - **Always make the ground point of the oscillator capacitor the same potential as CVss.**
   - **Do not ground the capacitor to a ground pattern through which a high current flows.**
   - **Do not fetch signals from the oscillator.**

Table 2-1: Main Oscillator Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	fOSC			16[a]		MHz
Oscillation stabilization time [b]	TOST	OSC MODE		10		ms

a. With any other frequency Peripheral function can't be guaranteed
b. T_{OST} depends on the external crystal

Note: Please specify the oscillation stabilization time of the main oscillator T_{OST} with the manufacturer of the external quartz crystal.

2.2 Sub-Oscillator Characteristics

Ta =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

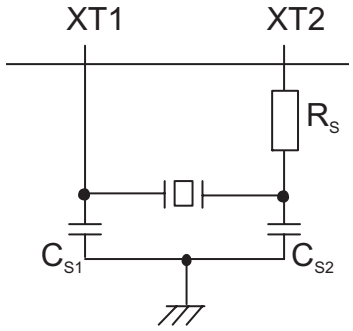


Figure 2-2: Sub-Oscillator Recommendations

Remark: Values of capacitors C_{S1}, C_{S2} and Resistor R_S depend on used crystal and must be specified in cooperation with the manufacturer.

Cautions:
1. **External clock input is prohibited.**
2. **Wire as follows in the area enclosed by the broken lines in the above figure to avoid an adverse effect from wiring capacitance.**
   - **Place the oscillation circuit as close as possible to X1 and X2 pins.**
   - **Keep the wiring length as short as possible.**
   - **Do not cross the wiring with the other signal lines.**
   - **Do not route the wiring near a signal line through which a high fluctuating current flows.**
   - **Always make the ground point of the oscillator capacitor the same potential as CVss.**
   - **Do not ground the capacitor to a ground pattern through which a high current flows.**
   - **Do not fetch signals from the oscillator.**

Table 2-2: Sub-Oscillator Operating Conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Oscillation frequency	fSOSC		32.500	32.768	33.000	KHz

Note: Please specify the oscillation stabilization time for the sub-oscillator TSOST with the manufacturer of the external quartz crystal.

2.3 Peripheral PLL Characteristics

Ta =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 2-3: Peripheral PLL Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Peripheral PLL lock-up time	T_{PLT}	OSC MODE			400	μs
Peripheral PLL Output period jitter[a]	T_{POPJ}		-100		100	ps

a. T_{POPJ} is not tested in production. It is specified by design and ensured by evaluation.

2.4 CPU PLL Characteristics

Ta =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 2-4: CPU PLL Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CPU PLL lock-up time	T_{CLT}	OSC MODE			400	μs
CPU PLL Output period jitter [a]	T_{COPJ}		-100		100	ps

a. T_{COPJ} is not tested in production. It is specified by design and ensured by evaluation.

2.5 Low-Frequency Internal Oscillator Characteristics

Ta =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 2-5: CPU PLL Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Low-frequency internal oscillator frequency	f_{LFIOSC}		120	240	480	KHz
Low-frequency internal oscillator stabilization time [a]	T_{LFIOST}				20	μs

a. T_{LFROST} is not tested in production. It is specified by design and ensured by evaluation.

2.6 High-Frequency Internal Oscillator Characteristics

Ta =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 2-6: CPU PLL Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-frequency internal oscillator frequency	f_{HFIOSC}		5.88	6.78	8.00	MHz
High-frequency internal oscillator stabilization time[a]	T_{HFIOST}				200	µs

a. T_{HFROST} is not tested in production. It is specified by design and ensured by evaluation.

2.7 CPU Clock

Ta =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 2-7: CPU clock frequency

Clock Mode	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
OSC mode, PLL					80	MHz

2.8 PLL Clock

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 2-8: PLL clock frequency

Clock Mode	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Peripheral Clock	f_{Perph}			80		MHz

3. Electrical Specification : DC Characteristics

3.1 General DC Characteristics

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 3-1: Input Leakage Current

Parameter	Symbol	Pin group	Conditions	MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	1	$0 \le V_I \le BV_{DD3X}$			3	μA
	I_{LIH2}	2	$0 \le V_I \le BV_{DD30}$			2	μA
	I_{LIH3}	3	$0 \le V_I \le BV_{DD31}$			3	μA
	I_{LIH4}	4	$0 \le V_I \le BV_{DD32}$			3	μA
	I_{LIH5}	5	$0 \le V_I \le MV_{DD3X}$			3	μA
	I_{LIH6}	6	$0 \le V_I \le BV_{DD31}$			500[a]	μA
	I_{LIH8}	8	$0 \le V_I \le AV_{DD}$			3	μA
	I_{LIH10}	10	$0 \le V_I \le V_{DD50}$			3	μA
	I_{LIH11}	11	$0 \le V_I \le V_{DD50}$			3	μA
	I_{LIH13}	13	$0 \le V_I \le V_{DD50}$			3	μA
Input leakage current, low	I_{LIL1}	1	$0 \le V_I \le BV_{DD3X}$			-3	μA
	I_{LIL2}	2	$0 \le V_I \le BV_{DD30}$			-2	μA
	I_{LIL3}	3	$0 \le V_I \le BV_{DD31}$			-3	μA
	I_{LIL4}	4	$0 \le V_I \le BV_{DD32}$			-3	μA
	I_{LIL5}	5	$0 \le V_I \le MV_{DD3X}$			-3	μA
	I_{LIL6}	6	$0 \le V_I \le MV_{DD31}$			-3	μA
	I_{LIL8}	8	$0 \le V_I \le AV_{DD}$			-3	μA
	I_{LIL10}	10	$0 \le V_I \le V_{DD50}$			-3	μA
	I_{LIL11}	11	$0 \le V_I \le V_{DD50}$			-3	μA
	I_{LIL13}	13	$0 \le V_I \le V_{DD50}$			-3	μA

a. High input current is caused by permanent pull-down resistor at the input.

3.2 Input/Output Level of pin groups

Following conditions are valid for all listed pin group input/output level:

- T_A =-40 to +105°C
- V_{DD5X} = 4.5 to 5.5V
- $V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
- $V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Note: Internally all BV_{DD3x} (x=0 to 2) and MV_{DD3y} (y= 0 to 4) are connected. All mentioned supply pins in this chapter has to be seen as main contribution and not as single supply!

3.2.1 Input/Output Level Pin Group 1: Main Area General Purpose Ports

These pins are supplied with BV_{DD3X} with the same I/O characteristics.
Pins of this pin group are:

- Group 1A (supplied by BV_{DD30}):
  - P00 to P07
  - P46
  - P10 to P14
- Group 1B (supplied by BV_{DD31}):
  - P40 to P44
  - P81 to P84
- Group 1C (supplied by BV_{DD32}):
  - P30 to P37
  - P45
  - P50 to P53

Table 3-2: Input/Output Level Pin Group 1

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage,high	V_{IH1}		0.7 x BV_{DD3X}		BV_{DD3X}+0.3	V
Input voltage,low	V_{IL1}		-0.5		0.3 x BV_{DD3X}	V
Output voltage, high	V_{OH1}	I_{OH} = -3mA	BV_{DD3X} -1.0			V
Output voltage, low	V_{OL1}	I_{OL} = 3mA			0.4	V
Pull-up resistor[a]	R_{PU1}		10	50	100	KΩ

a. Soft pull-up resistor

3.2.2 Input/Output Level Pin Group 2: MediaLB Ports

These pins are supplied with B_{VDD30} with special MediaLB buffer characteristics.
Pins of this pin group are:

- P15 to P17

Table 3-3: Input/Output Level Pin Group 2

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage,high	V_{IH2}		1.7		BV_{DD30}+0.3	V
Input voltage,low	V_{IL2}		-0.5		0.7	V
Output voltage, high	V_{OH2}	I_{OH} = -6mA	2.0			V
Output voltage, low	V_{OL2}	I_{OL} = 6mA			0.4	V
Pull-up resistor[a]	R_{PU2}		10	50	100	KΩ

a. Soft pull-up resistor

3.2.3 Input/Output Level Pin Group 3: FlexRay Ports

These pins are supplied with BV_{DD31} with the same I/O characteristics.
Pins of this pin group are:

- P20 to P27

Table 3-4: Input/Output Level Pin Group 3

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage,high	V_{IH3}		0.7 x BV_{DD31}		BV_{DD31}+0.3	V
Input voltage,low	V_{IL3}		-0.5		0.3 x BV_{DD31}	V
Output voltage, high	V_{OH3}	I_{OH} = -3mA	BV_{DD31} -1.0			V
Output voltage, low	V_{OL3}	I_{OL} = 3mA			0.4	V
Pull-up resistor[a]	R_{PU3}		10	50	100	KΩ

a. Soft pull-up resistor

3.2.4 Input/Output Level Pin Group 4: $\overline{\text{MRESET}}$ Pin

These pins are supplied with BV_{DD32} with the same I/O characteristics.
Pin of this pin group is:

- $\overline{\text{MRESET}}$

Table 3-5: Input/Output Level Pin Group 4

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage,high	V_{IH4}		0.8 x BV_{DD32}		BV_{DD32}+0.3	V
Input voltage,low	V_{IL4}		-0.5		0.2 x BV_{DD32}	V

3.2.5 Input/Output Level Pin Group 5: External Bus Interface Ports

These pins are supplied with MV_{DD3X} with the same I/O characteristics.
Pins of this pin group are:

- Group 5A (supplied by MV_{DD30}):
  - PCS0
  - PCT4 to PCT6
  - PDL0 to PDL3
- Group 5B (supplied by MV_{DD31}):
  - PDL4 to PDL11
- Group 5C (supplied by MV_{DD32}):
  - PDL12 to PDL15
  - PAL0 to PAL3
- Group 5D (supplied by MV_{DD33}):
  - PAL4 to PAL11
- Group 5E (supplied by MV_{DD34}):
  - PAL12 to PAL15
  - PAH0 to PAH3
  - PCS1
  - FLMD1

Table 3-6: Input/Output Level Pin Group 5

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage,high	V_{IH5}		0.7 x MV_{DD3X}		MV_{DD3X}+0.3	V
Input voltage,low	V_{IL5}		-0.5		0.3 x MV_{DD3X}	V
Output voltage, high	V_{OH5}	I_{OH5} = -3mA	MV_{DD3X} -1.0			V
Output voltage, low	V_{OL5}	I_{OL5} = 3mA			0.4	V
Pull-up resistor[a]	R_{PU5}		10	50	100	KΩ

a. Soft pull-up resistor

3.2.6 Input/Output Level Pin Group 6: Input-Only Port P80

This pin is supplied with BV_{DD31} .
Pin of this pin group is:

- P80, this pin is shared with N-Wire Reset (DRST)

Table 3-7: Input/Output Level Pin Group 6

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage,high	V_{IH6}		0.7 x BV_{DD3X}		BV_{DD3X}+0.3	V
Input voltage,low	V_{IL6}		-0.5		0.3 x BV_{DD3X}	V
Pull-down resistor[a]	R_{PD6}		10	50	100	KΩ

a. Permanent pull-down resistor

3.2.7 Input/Output Level Pin Group 10: Isolated Area General Purpose Ports

These pins are supplied with V_{DD50} with the same I/O characteristics.
Pins of this pin group are:

- P60 to P63
- WDTOUT
- REGON

Table 3-8: Input/Output Level Pin Group 10

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage,high	V_{IH10}		0.7 x V_{DD50}		V_{DD50}+0.3	V
Input voltage,low	V_{IL10}		-0.5		0.3 x V_{DD50}	V
Output voltage, high	V_{OH10}	I_{OH} = -3mA	V_{DD50} -1.0			V
Output voltage, low	V_{OL10}	I_{OL} = 3mA			0.4	V
Pull-up resistor[a]	R_{PU10}		10	30	100	KΩ

a. Soft pull-up resistor

3.2.8 Input/Output Level Pin Group 11: Isolated $\overline{\text{RESET}}$ Pin

These pins are supplied with V_{DD5X} with the same I/O characteristics.
Pin of this pin group is:

- $\overline{\text{RESET}}$

Table 3-9: Input/Output Level Pin Group 11

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage,high	V_{IH11}		0.8 x V_{DD50}		V_{DD50}+0.3	V
Input voltage,low	V_{IL11}		-0.5		0.25 x V_{DD50}	V

3.2.9 Input/Output Level Pin Group 13: Isolated Area FLMD0

These pins are supplied with V_{DD5X} with the same I/O characteristics.
Pin of this pin group is:

- FLMD0

Table 3-10: Input/Output Level Pin Group 13

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage,high	V_{IH13}		0.8 x V_{DD50}		V_{DD50}+0.3	V
Input voltage,low	V_{IL13}		-0.5		0.2 x V_{DD50}	V

3.3 Supply Current

T_A =-40 to +105°C
V_{DD50} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 3-11: Power Supply Current

Parameter	Conditions		Supply Pins[a]	Symbol	MIN.	TYP.[b]	MAX.	Unit
Supply current[c]	RUN mode (f_{CPU} = 80MHz, PLL: on)	T_A= 85°C	VDD3n	I_{DD1MA}		170	210	mA
		T_A= 105°C					260	mA
		T_A= 105°C	VDD50	I_{DD1IA}			1.2	mA
	IDLE mode (f_{OSC} = 16MHz)		VDD3n	I_{DD4MA}			65	mA
	Power down mode main area power-off isolated area stand-by	T_A= 25°C	VDD50	I_{DD5IA}			55	μA
		T_A= 85°C					300	μA
		T_A= 105°C					600	μA

a. n= 0 to 2
b. The typical value refers to Ta = 25°C, V_{DD50} = 5V and V_{DD3n} = 3.3V
c. The port output current resulting from built-in pull-up or pull-down resistances is not included.

3.4 Injected Current

3.4.1 DC Characteristics of Overload Current

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 3-12: Injected Current: DC Characteristics of Overload Current

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Positive overload current $V_{IN} > XV_{DDn}$[a]	I_{INJP}	Digital input pins	Per pin			1	mA
			Total V_{DDmx}[b]			16	mA
		Analog input pins	Per pin			1	mA
			Total AV_{DD}			4	mA
Positive overload current $V_{IN} < XV_{SSnx}$[c]	I_{INJnM}	Digital input pins	Per pin			-1	mA
			Total V_{DDmx}[b]			-16	mA
		Analog input pins	Per pin			-0.1	mA
			Total AV_{DD}			-1	mA

a. XV_{DDnx}: either BV_{DD3x} with x = 0 to 2, MV_{DD3x} with x = 0 to 4 or AV_{DD}.
b. V_{DDmx}: either V_{DD3x} with x = 0 to 2 or V_{DD50}
c. $XV_{SSnx:}$ either BV_{SS3x} with x = 0 to 2, MV_{SS3x} with x = 0 to 4, BV_{SS50} or AV_{SS}

3.4.2 A/D Converter Influenced by Injected Current on Adjacent Pin

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 3-13: Injected Current: DC Characteristics of Overload Current

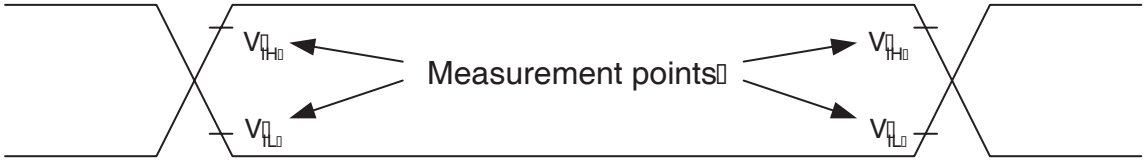
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Degradation of overall error[a]	I_{INJPAD}	b			±5	LSB
	I_{INJNAD}				±5	LSB

a. These specifications are not tested in the outgoing inspection, but specified based on the device characterization
b. Measurement condition: Current is injected into one pin of the DUT. Measurement of effect of this injected current is measured at adjacent pin.

Caution: The value given in table 3-13 stands for the degration by injected current on an adjacent pin. Therefore, this value is added to the specification of A/D converters overall error defined seperatly as the electrical specifications (5. "Electrical Specification : AD Converter" on page 47)
If there is an increase leakage current, based on the negative currents injected into the pin adjacent to the converted channel, the effect on the A/D converters accuracy depends on the external analog source impedance.

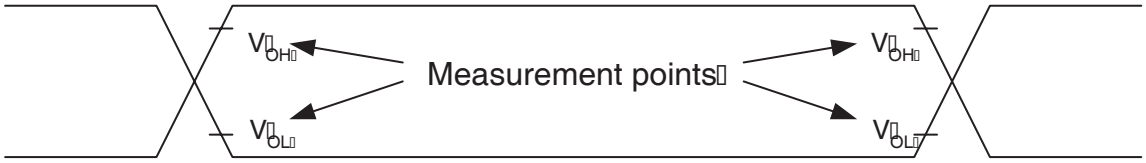
4. Electrical Specification : AC Characteristics

AC Test Input Measurement Points,



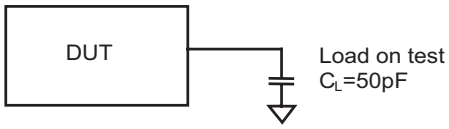
$V_{IH} = 0.7 \times V_{DDxy}$
$V_{IL} = 0.3 \times V_{DDxy}$

AC Test Output Measurement Points



$V_{OH} = 0.7 \times V_{DDxy}$
$V_{OL} = 0.3 \times V_{DDxy}$

Load Conditions



Caution: If the load capacitance exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

4.1 Reset of Main Area: $\overline{\text{MRESET}}$ Timing

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 4-1: Turning On / Interception Timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{MRESET}}$ high-level width [a]	t_{WMRSH}		200			ns
$\overline{\text{MRESET}}$ low-level width [b]	$t_{WMRSLIL}$		200			ns
$\overline{\text{MRESET}}$ pulse rejection [c]	t_{WMRRJ}		50	100	200	ns
$\overline{\text{MRESET}}$ power up delay [d]	t_{WMRPD}		$2 + T_{OST}$			ms

a. This signal high time is needed to ensure that the internal $\overline{\text{MRESET}}$ release operation starts.
b. This signal low time is needed to ensure that the internal $\overline{\text{MRESET}}$ is activated. Reset pulses shorter than the given value may not be recognized by the device
c. The $\overline{\text{MRESET}}$ input incorporates an analog filter. Pulses shorter than this value will be ignored. Characteristic is not tested during production, it is ensured by design and will be evaluated.
d. During ramp-up of the internal power supply (VDD of the main area) the release of $\overline{\text{MRESET}}$ has to be delayed until VDD and the main oscillator are stabilized.
Please also refer to chapter 2.1 on page 16.

Figure 4-1: $\overline{\text{MRESET}}$ timing

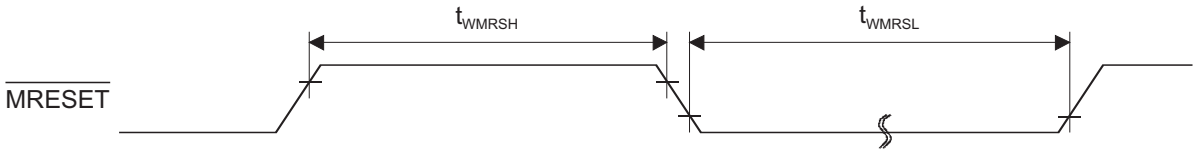
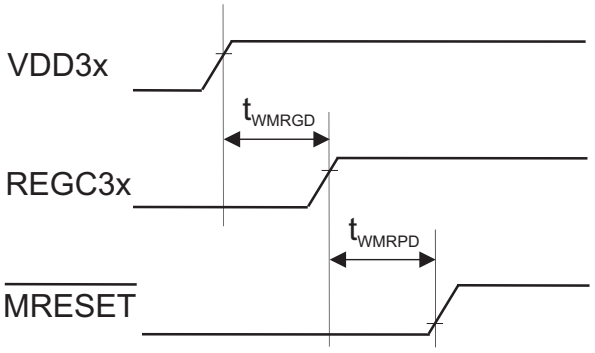


Figure 4-2: $\overline{\text{MRESET}}$ delay during VDD ramp-up



4.2 Reset of Isolated Area: $\overline{\text{RESET}}$ Timing

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 4-2: Turning On / Interception Timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width [a]	t_{WRSH}		300			ns
$\overline{\text{RESET}}$ low-level width [b]	t_{WRSLIL}		300			ns
$\overline{\text{RESET}}$ pulse rejection [c]	t_{WRRJ}		140	200	350	ns
$\overline{\text{RESET}}$ power up delay [d]	t_{WRPD}		2			ms

a. This signal high time is needed to ensure that the internal $\overline{\text{RESET}}$ release operation starts.
b. This signal low time is needed to ensure that the internal $\overline{\text{RESET}}$ is activated.
c. The $\overline{\text{RESET}}$ input incorporates an analog filter. Pulses shorter than this value will be ignored. Characteristic is not tested during production, it is ensured by design and will be evaluated.
d. During ramp-up of the internal power supply (VDD of the main area) the release of $\overline{\text{RESET}}$ has to be delayed until VDD is stabilized.

Figure 4-3: $\overline{\text{RESET}}$ timing

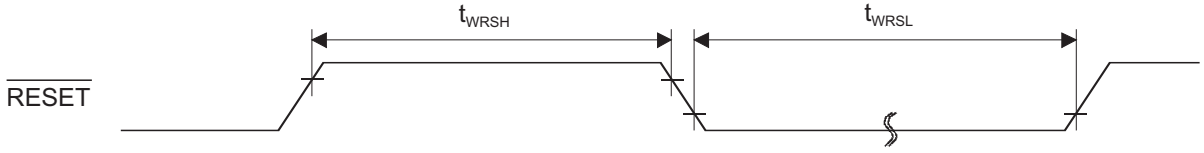
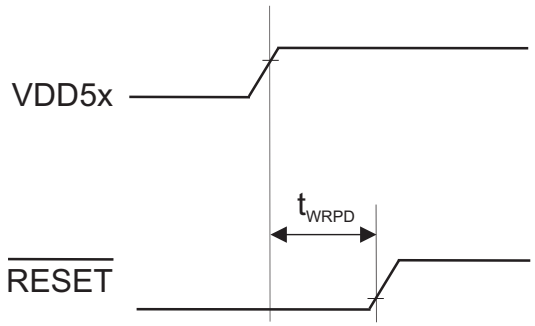


Figure 4-4: $\overline{\text{RESET}}$ delay during VDD ramp-up



4.3 Interrupt Timing

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

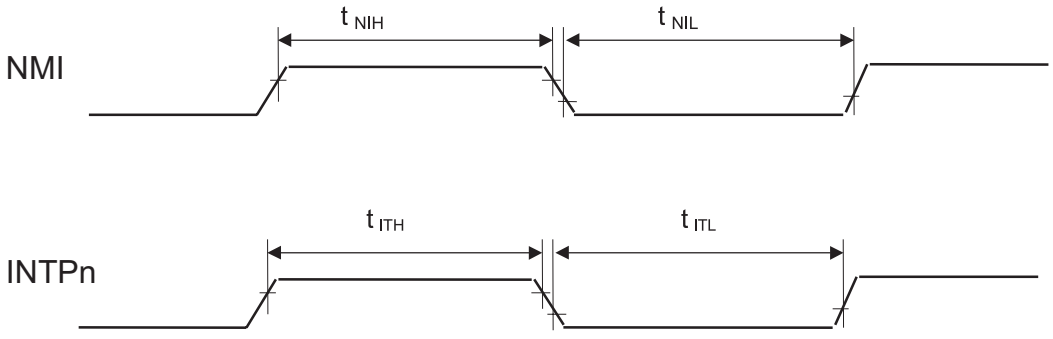
Table 4-3: Interrupt Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
NMI input high level width [a]	t_{NIH}		150		ns
NMI input low level width [a]	t_{NIL}		150		ns
NMI pulse rejection [b]	t_{NIRJ}		50	150	ns
INTPn input high level width [a]	t_{ITH}		150		-
INTPn input low level width [a]	t_{ITL}		150		ns
INTPn pulse rejection [b]	t_{ITRJ}		50	150	-

a. Pulses longer than this value will pass hte analog filter
b. Pulses shorter than this value do not pass the analog input filter. This characteristic is not tested in production, it is ensured by design and evaluated.

Remark: n = 0 to 14

Figure 4-5: Interrupt Timing



4.4 Clocked Serial Interface B (CSIB) Characteristics

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 4-4: CSIB Characteristics (Master Mode)

CBnSCK2 to CBnSCK0 ≠ 111B

Parameter	Symbol	MIN.	MAX.	Unit
$\overline{SCKBn}$ output clock cycle time	t_{CYSKM}	125		ns
$\overline{SCKBn}$ output high level width	t_{WSKHM}	0.5 t_{CYSKM} - 10		ns
$\overline{SCKBn}$ output low level width	t_{WSKLM}	0.5 t_{CYSKM} - 10		ns
SIBn input setup time (vs. $\overline{SCKBn}$↑)	t_{SSISKM}	20		ns
SIBn input hold time (vs. $\overline{SCKBn}$↑)	t_{HSKSIM}	10		ns
SOBn output delay (vs. $\overline{SCKBn}$↓)	t_{DSKSOM}		10	ns
SOBn output hold time (vs. $\overline{SCKBn}$↑)	t_{HSKSOM}	0.5 t_{CYSKM} - 10		ns

Remark: n = 0, 1

Table 4-5: CSIB Characteristics (Slave Mode)

CBnSCK2 to CBnSCK0 = 111B

Parameter	Symbol	MIN.	MAX.	Unit
$\overline{SCKBn}$ input clock cycle time	t_{CYSKS}	125		ns
$\overline{SCKBn}$ input high level width	t_{WSKHS}	0.5 t_{CYSKM} - 10		ns
$\overline{SCKBn}$ input low level width	t_{WSKLS}	0.5 t_{CYSKM} - 10		ns
SIBn input setup time (vs. $\overline{SCKBn}$↑)	t_{SSISKS}	5		ns
SIBn input hold time (vs. $\overline{SCKBn}$↑)	t_{HSKSIS}	10		ns
SOBn output delay (vs. $\overline{SCKBn}$↓)	t_{DSKSOS}		25	ns
SOBn output hold time (vs. $\overline{SCKBn}$↑)	t_{HSKSOS}	t_{WSKHS}		ns

Remark: n = 0, 1

Figure 4-6: CSIB Timing In Master Mode (CKP, DAP bits = 00B or 11B)

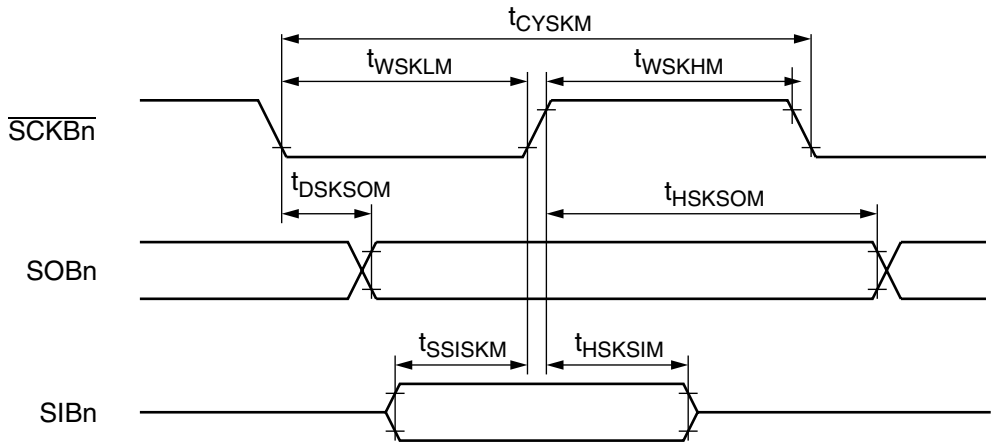


Figure 4-7: CSIB Timing In Master Mode (CKP, DAP bits = 01B or 10B)

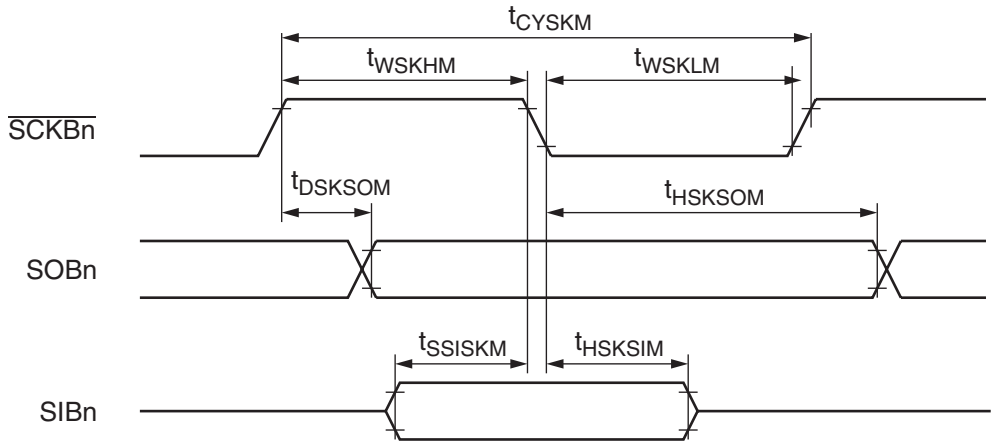


Figure 4-8: CSIB Timing In Slave Mode (CKP, DAP bits = 00B or 11B)

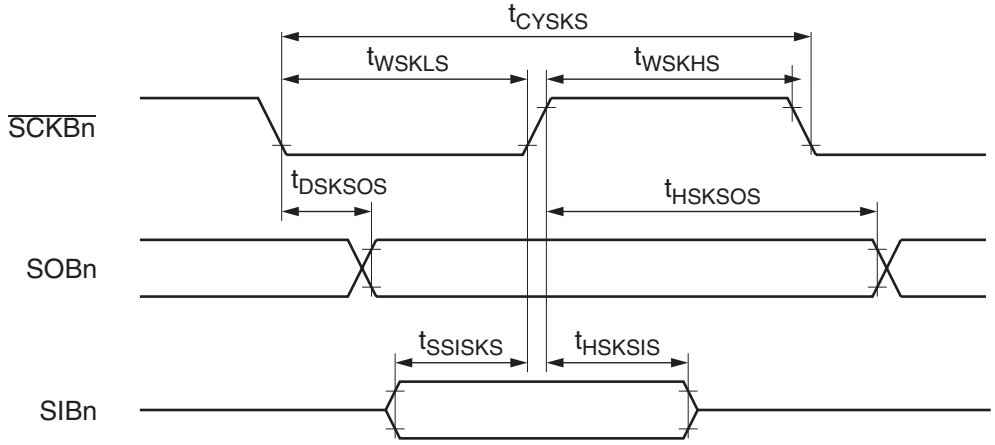
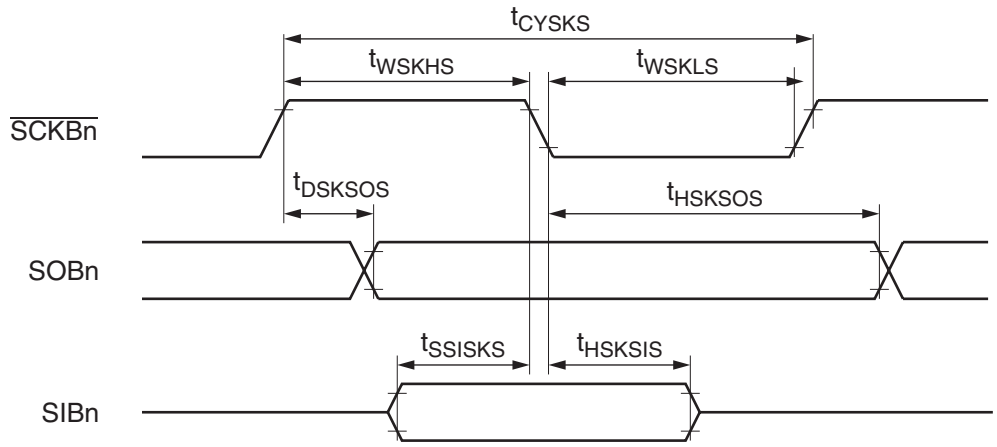


Figure 4-9: CSIB Timing In Slave Mode (CKP, DAP bits = 01B or 10B)



4.5 Enhanced Queued Clocked Serial Interface (CSIE) Timing

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Cautions: 1. All output pins used for CSIE application (CSIE0 [ports P40, P41] and CSIE1 [PDL14, PDL15] are connected to an external load of 50pF.
2. All chip select output pins for the CSIE (SCSE00 to 07 [PAL7 to 14] and SCSE10 to 13 [PAL3 to 6] are connected to an external load of 25pF.

Figure 4-10: CSIE AC Load Condition

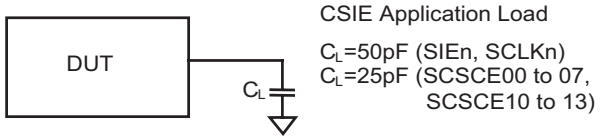


Table 4-6: CSIE Characteristics (Master Mode)

Parameter		Symbol	MIN.	MAX.	Unit
Macro operation clock, cycle time		t_{KCY}	31.25		ns
$\overline{SCKEn}$ cycle time		t_{KCYM}	125		ns
$\overline{SCKEn}$ high level width		t_{KWHM}	t_{KCYM}/2 - 10		ns
$\overline{SCKEn}$ low level width		t_{KWLM}	t_{KCYM}/2 - 10		ns
SIEn input setup time (vs. $\overline{SCKEn}$)		t_{SSI}	20		ns
SIEn input hold time (vs. $\overline{SCKEn}$)		t_{HSIM}	10		ns
SOEn output delay (vs. $\overline{SCKEn}$)		t_{DSOM}		20	ns
SOEn output hold time (vs. $\overline{SCKEn}$)		t_{HSOM}	t_{KCYM}/2 - 10		ns
SCSEnm inactive (High) width	CEnSIT=x CEnOPE=0 CEnMD=x	t_{WSCSB0}	t_{KCYM}/2 - 10		ns
	CEnSIT=x CEnOPE=1 CEnMD=x	t_{WSCSB1}	$(CS_{IDLE} + 0.5)*t_{KCYM}$ - 10		ns

Table 4-6: CSIE Characteristics (Master Mode)

Parameter		Symbol	MIN.	MAX.	Unit
SCSEnm setup time (vs. SCKEn)	CEnSIT=x CEnOPE=0 CEnIDL=x CEnMD=0	t_{SSCSB0}	t_{KCY} - 10		ns
	CEnSIT=x CEnOPE=1 CEnIDL=0 CEnMD=0	t_{SSCSB1}	t_{KCYM} + t_{KCY} - 10		ns
	CEnSIT=x CEnOPE=0 CEnWE=1 CEnCSM=1 CEnIDL=x CEnMD=x	t_{SSCSB2}	t_{KCYM} / 2 + t_{KCY} - 10		ns
	CEnSIT=x CEnOPE=1 (CEnIDL=0 and CS change) CEnMD=X		CS_{SETUP} * t_{KCYM} + t_{KCY} - 10		ns
	CEnSIT=x CEnOPE=1 CEnIDL=1 CEnMD=X				
SCSEnm hold time (vs. SCKEn)	CEnSIT=0 CEnOPE=0 CEnMD=x	t_{HSCSB0}	t_{KCY} - 10		ns
	CEnSIT=1 CEnOPE=0 CEnMD=x	t_{HSCSB1}	t_{KCYM}/2 + t_{KCY} - 10		ns
	CEnSIT=0 CEnOPE=1 CEnMD=x	t_{HSCSB2}	CS_{HOLD} * t_{KCYM} + t_{KCY} - 10		ns
	CEnSIT=1 CEnOPE=1 CEnMD=x	t_{HSCSB3}	(CS_{HOLD} + 0.5)* t_{KCYM} + t_{KCY} - 10		ns
SCSEnm interframe time	CEnSIT=x CEnOPE=1 CEnMD=x	t_{INTER}	CS_{INTER} * t_{KCYM} - 5		ns
	CEnSIT=x CEnOPE=0 CEnMD=x	-	Not Applicable		ns

Remark: n=0,1
m=7-0(n=0),3-0(n=1)
CS_{SETUP},CS_{INTER}: are set by register CEnOPT0
CS_{IDLE},CS_{HOLD}: are set by register CEnOPT1

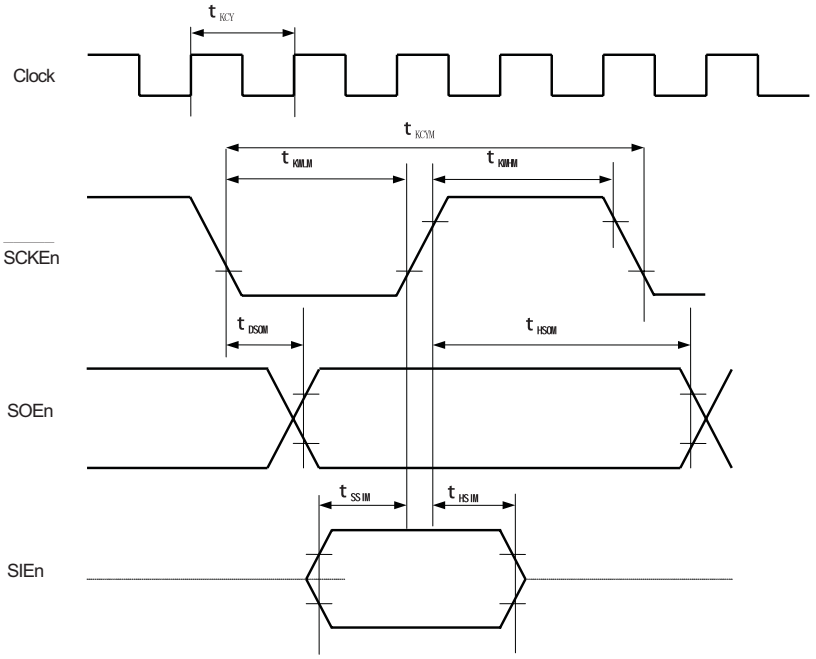
Table 4-7: CSIE Characteristics (Slave Mode)

Parameter	Symbol	MIN.	MAX.	Unit
Macro operation clock, cycle time	t_{KCY}	31.25		ns
$\overline{SCKEn}$ cycle time	t_{KCYS}	125		ns
$\overline{SCKEn}$ high level width	t_{KWHS}	$t_{KCYS}/2$ - 10		ns
$\overline{SCKEn}$ low level width	t_{KWLS}	$t_{KCYS}/2$ - 10		ns
SIEn input setup time (vs. $\overline{SCKEn}$)	t_{SSIS}	10		ns
SIEn input hold time (vs. $\overline{SCKEn}$)	t_{HSIS}	t_{KCY} x 1.5 +10		ns
SOEn output delay (vs. $\overline{SCKEn}$)	t_{DSOS}		20	ns
SOEn output hold time (vs. $\overline{SCKEn}$)	t_{HSOS}	$t_{KCYS}/2$ - 10		ns

Remark: n= 0,1

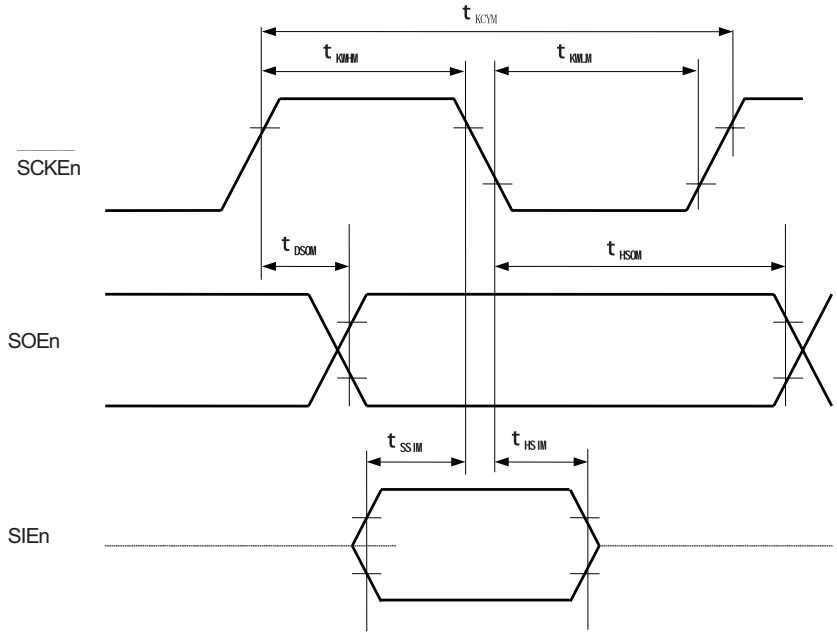
Figure 4-11: CSIEn Timings

(a) [$\overline{\text{SCKEn}}$/SIEn/SOEn] Pins In Master Mode: (CEnCTL1: CEnCKP/CEnDAP=0/0 or 1/1)



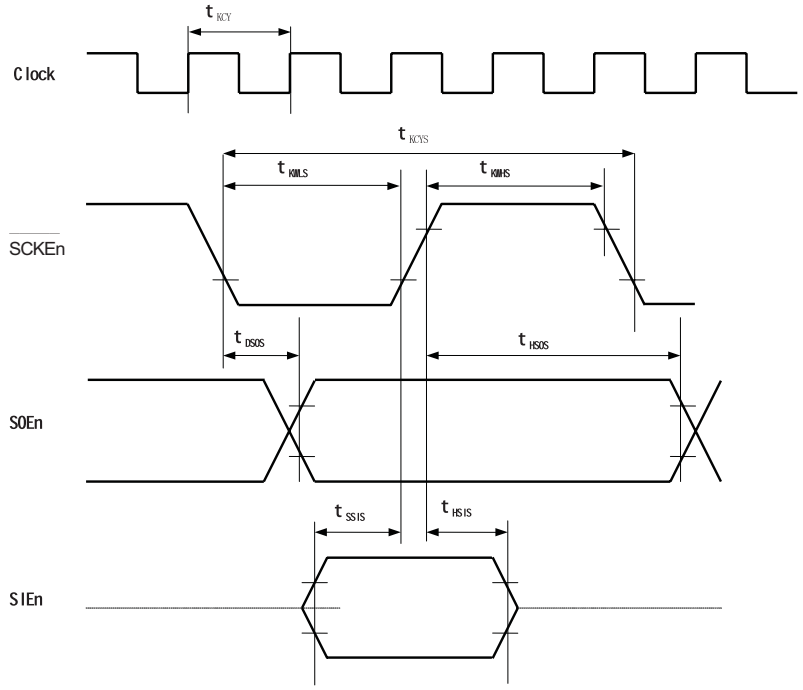
Remark: n= 0-1

(b) [$\overline{\text{SCKEn}}$/SIEn/SOEn] Pins In Master Mode: (CEnCTL1: CEnCKP/CEnDAP=1/0 or 0/1)



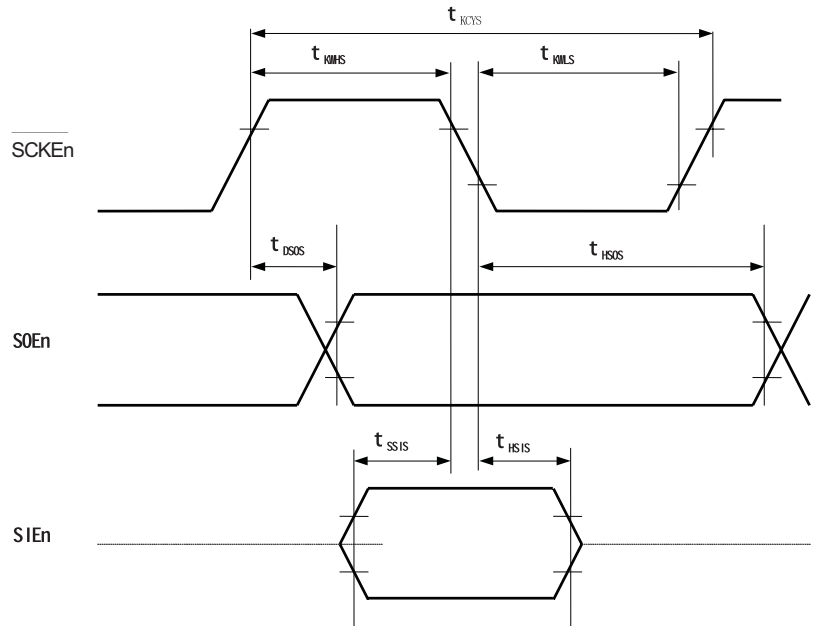
Remark: n= 0-1

(c) [$\overline{\text{SCKEn}}$/SIEn/SOEn] Pins In Slave Mode: (CEnCTL1: CEnCKP/CEnDAP=0/0 or 1/1)



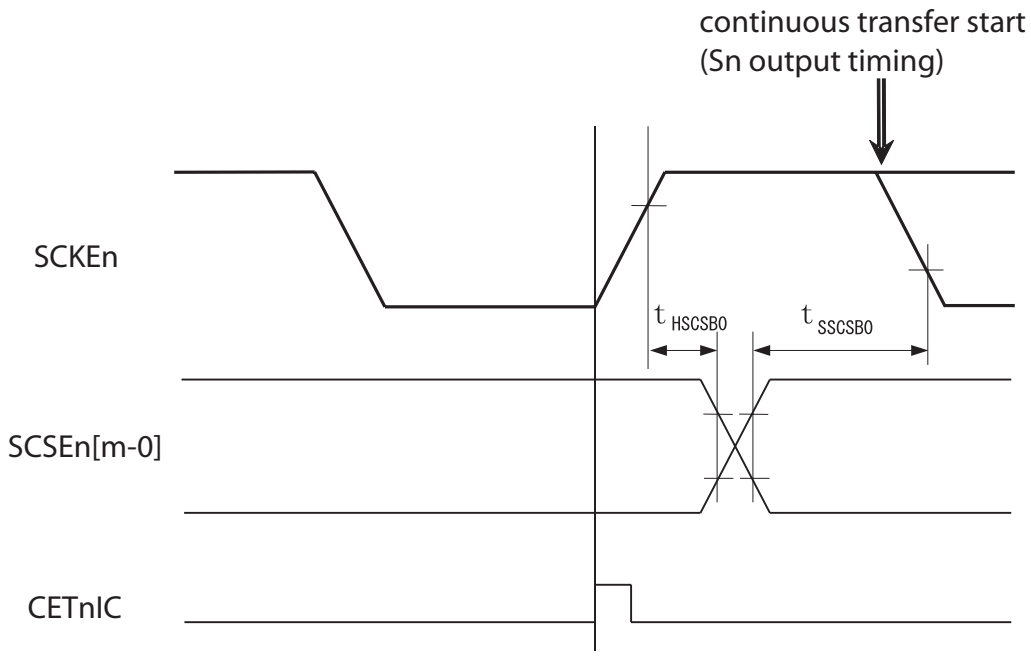
Remark: n= 0-1

(d) [$\overline{\text{SCKEn}}$/SIEn/SOEn] Pins In Slave Mode: (CEnCTL1: CEnCKP/CEnDAP=1/0 or 0/1)



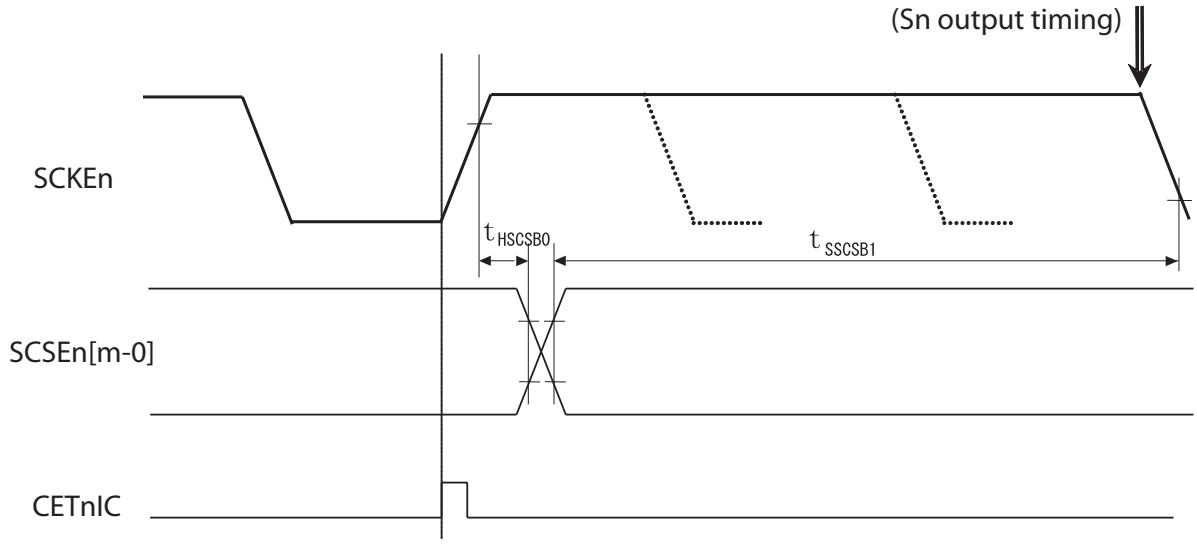
Remark: n= 0-1

(e) Only In Master Mode (CEnCTL0:CEnSIT=0 & CEnCTL4:CEnOPE/CEnMD=0/0)



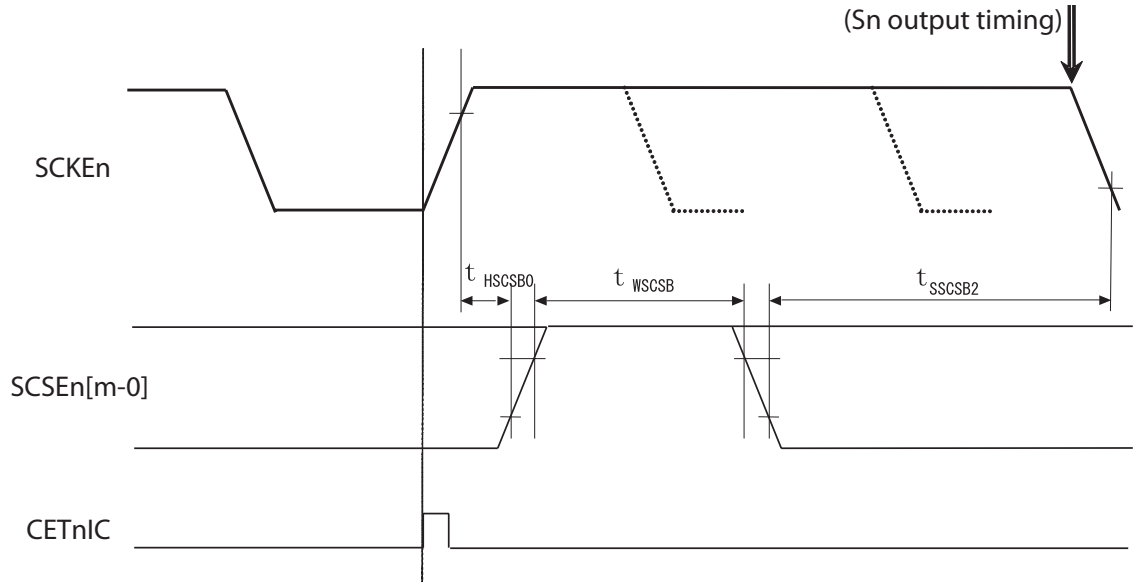
Remark: n= 0-1
m= 7(n=0),3(n=1)
CETnIC: CSIEn transfer end interrupt

(f) Only In Master Mode (CEnCTL0:CEnSIT=0 & CEnCTL4:CEnOPE/CEnMD=1/0)



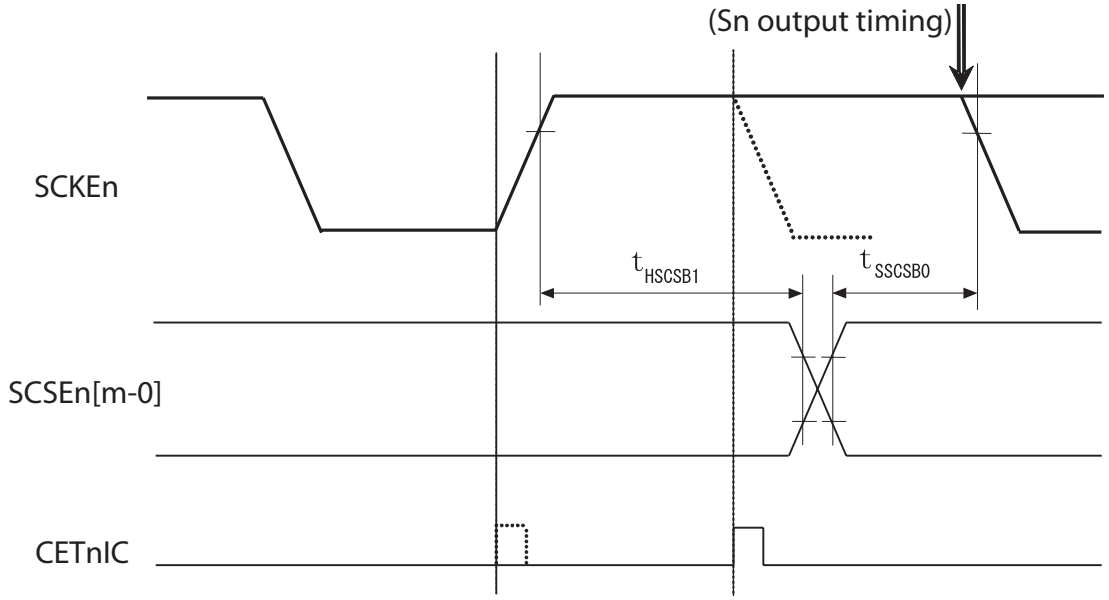
Remark: n= 0-1
m= 7(n=0),3(n=1)
CETnIC: CSIEn transfer end interrupt

(g) Only In Master Mode (CEnCTL0:CEnSIT=0 & CEnCTL4:CEnOPE/CEnMD=1/1)



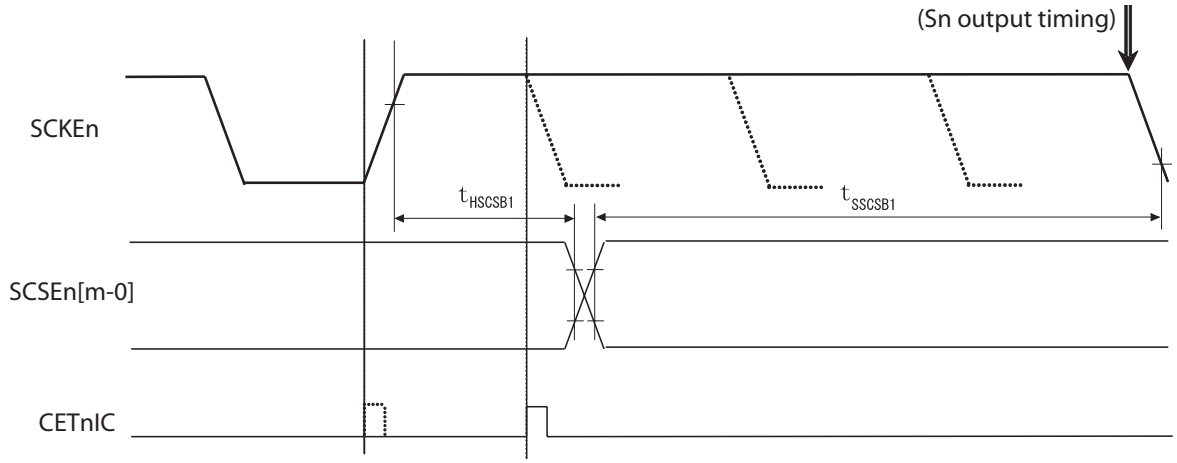
Remark: n= 0-1
m= 7(n=0),3(n=1)
CETnIC: CSIEn transfer end interrupt

(h) Only In Master Mode (CEnCTL0:CEnSIT=1 & CEnCTL4:CEnOPE/CEnMD=0/0)



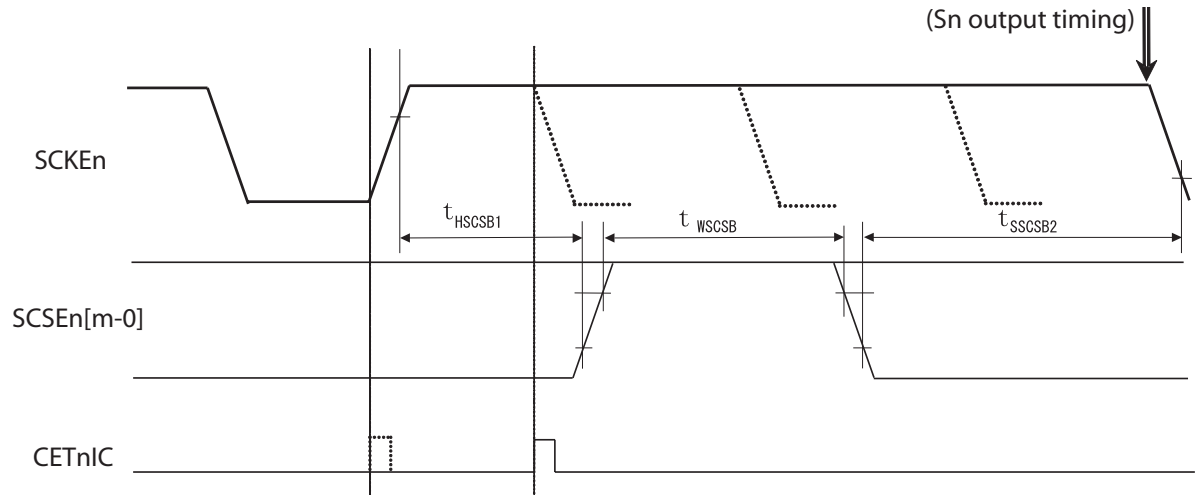
Remark: n= 0-1
m= 7(n=0),3(n=1)
CETnIC: CSIEn transfer end interrupt

(i) Only In Master Mode (CEnCTL0:CEnSIT=1 & CEnCTL4:CEnOPE/CEnMD=1/0)



Remark: n= 0-1
m= 7(n=0),3(n=1)
CETnIC: CSIEn transfer end interrupt

(j) Only In Master Mode (CEnCTL0:CEnSIT=1 & CEnCTL4:CEnOPE/CEnMD=1/1)



Remark: n= 0-1
m= 7(n=0),3(n=1)
CETnIC: CSIEn transfer end interrupt

4.6 I^2C Characteristics

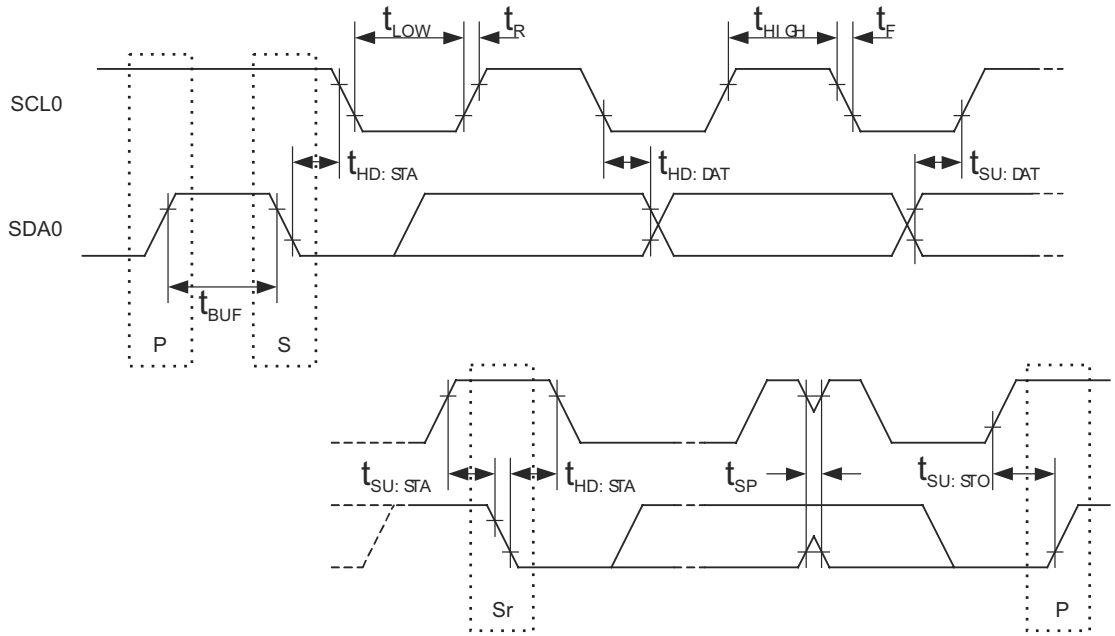
T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 4-8: I^2C Characteristics

Parameter		Symbol	Normal Mode		Fast Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCL0 clock frequency		f_{CLK}	0	100	0	400	kHz
Bus-free time (between stop/start conditions)		t_{BUF}	4.7		1.3		μs
Hold time [a]		$t_{HD:STA}$	4.0		0.6		μs
SCL0 clock low-level width		t_{LOW}	4.7		1.3		μs
SCL0 clock high-level width		t_{HIGH}	4.0		0.6		μs
Setup time for start/restart conditions		$t_{SU:STA}$	4.7		0.6		μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	5.0				μs
	I^2C mode		0 [b]	3.45 [c]	0 [b]	0.9 [c]	μs
Data setup time		$t_{SU:DAT}$	250		100 [d]		ns
STOP condition setup time		$t_{SU:STO}$	4.0		0.6		μs
Noise suppression [e]		t_{SP}				t_{IICLK} [f]	μs
Capacitive load of each bus line		C_b		400		400	pF

a. At the start condition, the first clock pulse is generated after the hold time.
b. The system requires a minimum of 300ns hold time internally for the SDA signal (at V_{IHmin} of SCL0 signal) in order to occupy the undefined area at falling edge of SCL0.
c. If the system does not extend the SCL0 signal low time (t_{low}), only the maximum data hold time ($t_{HD:DAT}$) needs to be satisfied.
d. The fast-speed-mode IIC bus can be used in a normal-mode IIC bus system. In this case, set the fast-speed-mode IIC bus so that it meets the following conditions:
   - If the system does not extend the SCL0 signals low state hold time:
     $t_{SU:DAT} \geq$250ns
   - If the system extends the SCL0 signal low state hold time:
     Transmit the following data bit to the SDA0 line prior to releasing the SCL0 line ($t_{Rmax} + t_{SU:DAT}$ = 1000+250 ns = 1250ns : Normal mode IIC bus specification).
e. Noise suppresion is only available in fast-speed mode.
f. t_{IICLK} is the period of the IICLK supplied by the clock controller.

Figure 4-12: I^2C Timing



4.7 UARTD Timing

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 4-9: UARTD Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate	T_{UARTDn}			312.5	Kbps

4.8 CAN Timing

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 4-10: CAN Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate	T_{aFCAN}			1	Mbps

4.9 FlexRay Timing

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 4-11: FlexRay Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transfer rate	$T_{FlexRay}$			10	Mbps

4.10 MediaLB Timing

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

The AC characterics of the MediaLB of following table is considered with a load capaticance of 40 pF.

Table 4-12: MediaLB Timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
MLBCLK operating frequencies	f_{MCK}	256 x FS at 44.0 KHz	11.264			MHz
		256 x FS at 48.0 KHz		12.228		
		512 x FS at 44.0 KHz		24.576		
		512 x FS at 48.1 KHz			24.627	
		512 x FS PLL unlocked			25.600	
MLBCLK rise time	t_{MCKR}			3		ns
MLBCLK fall time	t_{MCKF}			3		ns
MLBCLK cycle time	t_{MCKC}	256 x FS		81		ns
		512 x FS		40		
MLBCLK low time	t_{MCKL}	256 x FS	31.5	37		ns
		256 x FS PLL unlocked	30	35.5		
		512 x FS	14.5	17		ns
		512 x FS PLL unlocked	14	16.5		
MLBCLK high time	t_{MCKH}	256 x FS	31.5	38		ns
		256 x FS PLL unlocked	30	36.5		
		512 x FS	14.5	17		ns
		512 x FS PLL unlocked	14	16.5		
MLBCLK pulse width variation	t_{MPWV}	a			2	ns pp
MLBSIG/MLBDAT input valid (vs. MLBCLK falling)	t_{DSMCF}		1			ns
MLBSIG/MLBDAT input hold (vs. MLBCLK low)	t_{DHMCF}		0			ns
MLBSIG/MLBDAT output high impedance (vs. MLBCLK low)	t_{MCFDZ}		0		t_{MCKL}	ns
Bus hold time	t_{MDZH}		4			ns
MLBSIG/MLBDAT output valid (vs. MLBCLK rising)	t_{DSMCH}				13	ns

a. Pulse width variation is measured at 1.25V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (pp)

Figure 4-13: MediaLB Timing

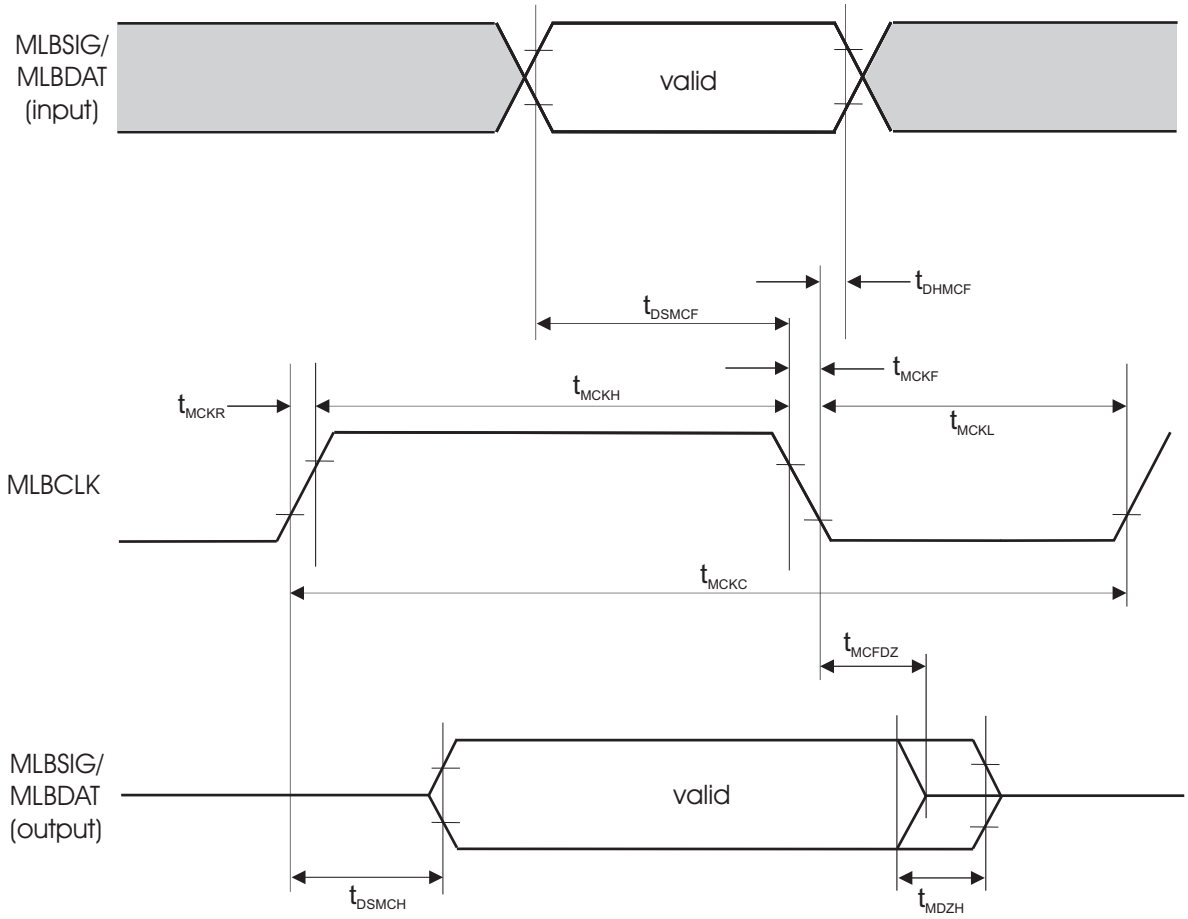
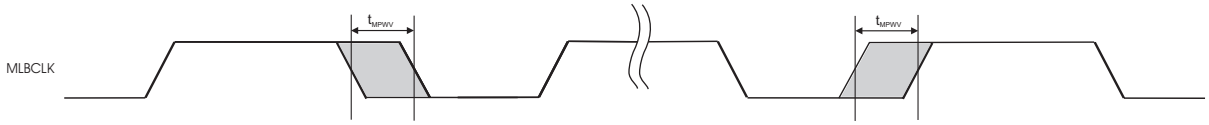


Figure 4-14: MediaLB Pulse Width Variation Timing



4.11 Timer AA Timing

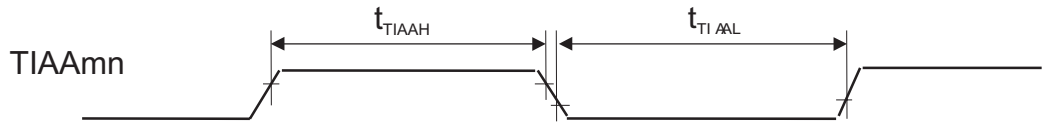
T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 4-13: Timer AA Timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TIAAmn high-level width	$t_{TIAAHNB}$	react on both edges	150			ns
	$t_{TIAAHNS}$	react on single edge	150			ns
TIAAmn low-level width	$t_{TIAALNB}$	react on both edges	150			ns
	$t_{TIAALNS}$	react on single edge	150			ns

Remark: m = 0 to 3 ; n = 0,1

Figure 4-15: Timer AA Input Timing



4.12 Timer AB Timing

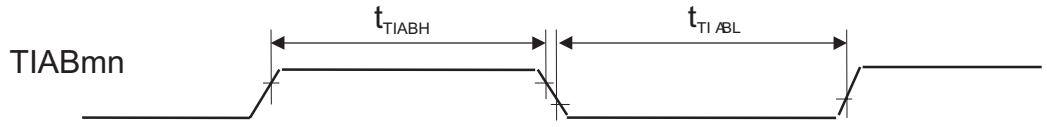
T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 4-14: Timer AB Timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
TIABmn high-level width	$t_{TIABHNB}$	react on both edges	150			ns
	$t_{TIABHNS}$	react on single edge	150			ns
TIABmn low-level width	$t_{TIABLNB}$	react on both edges	150			ns
	$t_{TIABLNS}$	react on single edge	150			ns

Remark: m = 0, 1 ; n = 0 to 3

Figure 4-16: Timer AB Input Timing



5. Electrical Specification : AD Converter

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 5-1: AD Converter

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution					10	bit
Reference volatge			AV_{SS}		AV_{DD}	V
Overall error[a]	TOE	$AV_{SS} \leq AIN \leq AV_{REF0} = AV_{DD}$			±4	LSB
Quantization error					±0.5	LSB
Conversion time [b]	t_{CONV}		2.0		20.0	µs
Analog input voltage	V_{IAN}		AV_{SS}		AV_{REF}	V
Analog input equivalent circuit resistance[c]	R_{INA}			0.5	0.8	KΩ
Analog input equivalent circuit capacitance[c]	C_{INA}			10	12	pF
Analog supply current	I_{AVDD}			1.5	3	mA
Analog reference supply current [d]	I_{AVREF}			60	150	µA

a. The quantization error of ±0.5 LSB is not included.
b. The conversion time only in the analog part. The conversion time depends on register setting ADMn1. For ADMn1 register setting please refer to the users manual
c. These values are not tested during production. They are ensured by design and evaluated.
d. The analog reference supply current is mainly transient current, which is influenced by the conversion time. The given value is not tested during production. It is ensured by design and evaluated.

6. Electrical Specification : Flash Memory Characteristics

6.1 Code Flash Memory Characteristics

6.1.1 Code Flash General Characteristics

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 6-1: Code Flash General Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Number of rewrites	c_{CFWRT}				1000	times
Data retention	t_{CFRET}		15			years
Write current (DC)[a]	I_{CFWRT}				30	mA
Erase current (DC)[a]	I_{CFER}				28	mA

a. Total 3V DC current of the code flash which is supplied by pins V_{DD30}, V_{DD31} and V_{DD32}.

6.1.2 Code Flash Self-Programming Characteristics over Lifetime

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Cautions: 1. The values given in Table 6-2 are only valid for a CPU frequency of 80MHz.
2. The following pre-compile option was used to determine these values: STATUS_CHECK_USER (in SelfLibSetup.h)

Table 6-2: Code Flash Self-Programming Characteristics over Lifetime

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Blank Check Time	$t_{CFLBL,4K}$	One memory block (4K)		0.66	0.79	ms
	$t_{CFVBL,256K}$	64 memory blocks (256K)		21.67	26.00	ms
Erase Time	$t_{CFLER,4K}$	One memory block (4K)		13.97	279.40	ms
	$t_{CFLER,256K}$	64 memory blocks (256K)		34.76	695.20	ms
Write Time	$t_{CFLWR,2W}$	Write two words[a]		0.33	1.10	ms
	$t_{CFLWR,4K}$	One memory block (4K) @ 256 Bytes[b]		29.48	423.72	ms
Internal Verify Time	$t_{CFLVR,4K}$	One memory block (4K)		2.86	3.43	ms
	$t_{CFLVR,256K}$	64 memory blocks (256K)		171.38	205.66	ms

a. The corresponding library call is configured for 2 words per call.
b. The corresponding library call uses a 256 Bytes (= 64 words) source buffer.

6.1.3 Code Flash End-of-Line On-Board Programming Characteristics (PG-FP4: CSI)

T_A =-40 to +40°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 6-3: Code Flash End-of-Line On-Board Programming Characteristics (PG-FP4: CSI)

Parameter[a]	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Blank Check Time	t_{CFECBL}	W/E cycles ≤ 5 f_{OSC} = 16MHz f_{CSICLK} = 2.5MHz		0.08	0.10	s
Erase Time	t_{CFECER}			0.20	0.40	s
Write Time	t_{CFECWR}			13	22	s
Read Verify Time	t_{CFECVR}			8	10	s

a. All parameters apply to the code flash area, i.e. all code flash blocks (0 to 127).

Note: The specified value does not include the time needed to establish the connection to the device.

6.1.4 Code Flash End-of-Line Self-Programming Characteristics

T_A =-40 to +40°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Cautions: 1. The values given in Table 6-4 are only valid for a CPU frequency of 80MHz.
2. The following pre-compile option was used to determine these values: STATUS_CHECK_USER (in SelfLibSetup.h)

Table 6-4: Code Flash End-of-Line Self-Programming Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Blank Check Time	$t_{CFLBL,4K}$	One memory block (4K)		0.66	0.79	ms
	$t_{CFVBL,256K}$	64 memory blocks (256K)		21.67	26.00	ms
Erase Time	$t_{CFLER,4K}$	One memory block (4K)		13.97	55.88	ms
	$t_{CFLER,256K}$	64 memory blocks (256K)		34.76	139.04	ms
Write Time	$t_{CFLWR,2W}$	Write two words[a]		0.33	0.50	ms
	$t_{CFLWR,4K}$	One memory block (4K) @ 256 Bytes[b]		29.48	117.09	ms
Internal Verify Time	$t_{CFLVR,4K}$	One memory block (4K)		2.86	3.43	ms
	$t_{CFLVR,256K}$	64 memory blocks (256K)		171.38	205.66	ms

a. The corresponding library call is configured for 2 words per call.
b. The corresponding library call uses a 256 Bytes (= 64 words) source buffer.

6.2 Data Flash Memory Characteristics

6.2.1 Data Flash General Characteristics

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 6-5: Data Flash General Characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Size of one data flash section	S_{DFS}				2	KBytes
Number of data flash sections	c_{DFS}				16	sections
Number of rewrites of one data flash section	c_{DFWRT}				10000	times
Data retention	t_{DFRET}	after 1000 rewrite cycles	15			years
		after 10000 rewrite cycles	5			years
Write current (DC)[a]	I_{DFWRT}				15	mA
Erase current (DC)[a]	I_{DFER}				14	mA

a. Total 3V DC current of the data flash which is supplied by pins V_{DD30}, V_{DD31} and V_{DD32}.

6.2.2 Data Flash Self-Programming Characteristics over Lifetime

T_A =-40 to +105°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Cautions: 1. The values given in Table 6-6 are only valid for a CPU frequency of 80MHz.
2. The following pre-compile option was used to determine these values: STATUS_CHECK_USER (in SelfLibSetup.h)

Table 6-6: Data Flash Self-Programming Characteristics over Lifetime

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Blank Check Time[a]	$t_{DFLBL,2k}$	One memory block (2k)		0.39	0.47	ms
Erase Time[b]	$t_{DFLER,2k}$			13.46	269.15	ms
Write Time	$t_{DFLWR,1W}$	Write one word		0.13	1.54	ms
	$t_{DFLWR,4W}$	Write four words		0.25	5.89	ms
Internal Verify Time[c]	$t_{DFLVR,2k}$	One memory block (2k)		2.71	3.26	ms

a. Scales approximately linear with the number of memory blocks checked.
b. Values increase only slightly if two, four, eight memory blocks are erased.
c. Scales approximately linear with the number of memory blocks verified.

6.2.3 Data Flash End-of-Line On-Board Programming Characteristics (PG-FP4: CSI)

T_A =-40 to +40°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 6-7: Data Flash End-of-Line On-Board Programming Characteristics (PG-FP4: CSI)

Parameter[a]	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Blank Check Time	t_{DFECBL}	W/E cycles ≤ 5 f_{OSC} = 16MHz f_{CSICLK} = 2.5MHz		0.01	0.02	s
Erase Time	t_{DFECER}			0.20	0.40	s
Write Time	t_{DFECWR}			2	4	s
Read Verify Time	t_{DFECVR}			1	2	s

a. All parameters apply to the data flash area, i.e. all code flash blocks (0 to 15).

Note: The specified value does not include the time needed to establish the connection to the device.

6.2.4 Data Flash End-of-Line Self-Programming Characteristics

T_A =-40 to +40°C
V_{DD5X} = 4.5 to 5.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V
W/E cycles ≤ 5

Table 6-8: Data Flash End-of-Line Self-Programming Characteristics

Parameter[a]	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Blank Check Time[b]	$t_{DFESBL,2k}$	One memory block (2k)		0.39	0.47	ms
Erase Time[c]	$t_{DFESER,2k}$			13.46	53.86	ms
Write Time	$t_{DFESWR,1W}$	Write one word		0.13	0.44	ms
	$t_{DFESWR,4W}$	Write four words		0.25	1.50	ms
Internal Verify Time[d]	$t_{DFESVR,2k}$	One memory block (2k)		2.71	3.26	ms

a. All parameters apply to the data flash area, i.e. all code flash blocks (0 to 15).
b. Scales approximately linear with the number of memory blocks checked.
c. Values increase only slightly if two, four, eight memory blocks are erased.
d. Scales approximately linear with the number of memory blocks verified.

Note: The specified value does not include the time needed to establish the connection to the device.

7. Requirements for a supply voltage V_{DD50} below 4.5V

Please notice! Important to read!
This chapter contains important pieces of information on the special requirements for an extended range of operating voltage supply for the device for **V_{DD50}: 3.15V to 4.5V**

All conditions given in the following sub-chapters have to be considered if the device shall be operated at the (low) supply voltage of V_{DD50} = 3.15 to 4.5V.

All conditions mentioned in these chapters must be applied along with every other parameter that has been specified above, i.e. from Chapter 1 to Chapter 6. In case one of these parameter is mentioned in the following chapter it subtitutes the specification mentioned in Chapter 1 to Chapter 6.

In all conditions mentioned in Chapter 1 to Chapter 6 the statement VDD50 = 4.5 to 5.5V can be substituted by the statement VDD50 = 3.15 to 4.5V while applying the specification mentioned below. For each parameter that is not mentioned in the present chapter, the specifications of Chapter 1 to Chapter 6 remains valid.

(1) Absolute Maximum Ratings

T_A = -40 ~ 105°C,
Operation Modes: All
Duration: 15years
$V_{SS5x} = BV_{SS} = V_{SS3x} = AV_{SS0} = MV_{SS3X}$ = 0V

Table 7-1: Absolute Maximum Ratings

Parameter		Symbol	Test Conditions		Ratings	Unit
Operating ambient temperature		T_A	Normal operating mode		-40 to +105	°C
Storage temperature		T_{STGB}			-40 to +125	°C
High level output current	Group 10	I_{OH10}		1 pin	-0.5	mA
	Group 10	I_{OHA10}		Total	-1	mA
Low level output current	Group 10	I_{OL10}		1 pin	0.5	mA
	Group 10	I_{OLA10}		Total	1	mA

(2) General DC Characteristics

T_A =-40 to +105°C
V_{DD5X} = 3.15 to 4.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 7-2: Pin Leak Current

Parameter	Symbol	Pin group	Conditions	MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH10}	10	$0 \le V_I \le V_{DD50}$			3	µA
	I_{LIH11}	11	$0 \le V_I \le V_{DD50}$			3	µA
	I_{LIH13}	13	$0 \le V_I \le V_{DD50}$			3	µA
Input leakage current, low	I_{LIL10}	10	$0 \le V_I \le V_{DD50}$			-3	µA
	I_{LIL11}	11	$0 \le V_I \le V_{DD50}$			-3	µA
	I_{LIL13}	13	$0 \le V_I \le V_{DD50}$			-3	µA

(3) Input/Output Level Pin Group 10: Isolated Area General Purpose Ports

These pins are supplied with V_{DD50} with the same I/O characteristics.
Pins of this pin group are:

- P60 to P63
- WDTOUT
- REGON

Table 7-3: Input/Output Level Pin Group 10

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage,high	V_{IH10}		0.7 x V_{DD5X}		V_{DD5X}+0.3	V
Input voltage,low	V_{IL10}		-0.5		0.3 x V_{DD5X}	V
Output voltage, high	V_{OH10}	I_{OH} = -0.5mA	V_{DD5X} -1.0			V
Output voltage, low	V_{OL10}	I_{OL} = +0.5mA			0.4	V
Pull-up resistor[a]	R_{PU10}		10	30	100	KΩ

a. Soft pull-up resistor

(4) Input/Output Level Pin Group 11: Isolated $\overline{\text{RESET}}$

These pins are supplied with V_{DD5X} with the same I/O characteristics.
Pin of this pin group is:

- $\overline{\text{RESET}}$

Table 7-4: Input/Output Level Pin Group 11

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage,high	V_{IH11}		0.8 x V_{DD50}		V_{DD5X}+0.3	V
Input voltage,low	V_{IL11}		-0.5		0.25 x V_{DD50}	V

(5) Input/Output Level Pin Group 13: Isolated Area FLMD0

These pins are supplied with V_{DD5X} with the same I/O characteristics.
Pin of this pin group is:

- FLMD0

Table 7-5: Input/Output Level Pin Group 13

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage,high	V_{IH13}		0.8 x V_{DD50}		V_{DD5X}+0.3	V
Input voltage,low	V_{IL13}		-0.5		0.2 x V_{DD50}	V

(6) Supply Current

T_A =-40 to +105°C
V_{DD50} = 3.15 to 4.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 7-6: Power Supply Current

Parameter	Conditions		Supply Pins[a]	Symbol	MIN.	TYP.[b]	MAX.	Unit
Supply current[c]	RUN mode (f_{CPU} = 80MHz, PLL: on)		VDD50	I_{DD1IA}			1.2	mA
	Power down mode main area power-off isolated area stand-by	T_A= 25°C	VDD50	I_{DD5IA}			55	μA
		T_A= 85°C					300	μA
		T_A= 105°C					600	μA

a. n= 0 to 2
b. The typical value refers to Ta = 25°C, V_{DD50} = 5V and V_{DD3n}
c. The port output current resulting from built-in pull-up or pull-down resistances is not included.

(7) AC Characteristic: $\overline{\text{RESET}}$ Timing

T_A =-40 to +105°C
V_{DD5X} = 3.15 to 4.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 7-7: Turning On / Interception Timing

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ high-level width [a]	t_{WRSH}		300			ns
$\overline{\text{RESET}}$ low-level width [b]	t_{WRSLIL}		300			ns
$\overline{\text{RESET}}$ pulse rejection [c]	t_{WRRJ}		140	200	350	ns
$\overline{\text{RESET}}$ power up delay [d]	t_{WRPD}		2			ms

a. This signal high time is needed to ensure that the internal $\overline{\text{RESET}}$ release operation starts.
b. This signal low time is needed to ensure that the internal $\overline{\text{RESET}}$ is activated.
c. The $\overline{\text{RESET}}$ input incorporates an analog filter. Pulses shorter than this value will be ignored. Characteristic is not tested during production, it is ensured by design and will be evaluated.
d. During ramp-up of the internal power supply (VDD of the main area) the release of $\overline{\text{RESET}}$ has to be delayed until VDD and the main oscillator are stabilized.

Note: For figures please refer to 4.2 ”Reset of Isolated Area: RESET Timing” on page 28

(8) AC Characteristic: Interrupt Timing

T_A =-40 to +105°C
V_{DD5X} = 3.15 to 4.5V
$V_{DD3x} = AV_{DD} = BV_{DD3x} = MV_{DD3x}$ = 3.0 to 3.6V
$V_{SS5X} = V_{SS3x} = AV_{SS} = BV_{SS5X} = BV_{SS3X} = MV_{SS3X}$ = 0V

Table 7-8: Interrupt Timing

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
INTPn input high level width [a]	t_{ITH}		150		-
INTPn input low level width [b]	t_{ITL}		150		ns
INTPn pulse rejection [b]	t_{ITRJ}		50	150	-

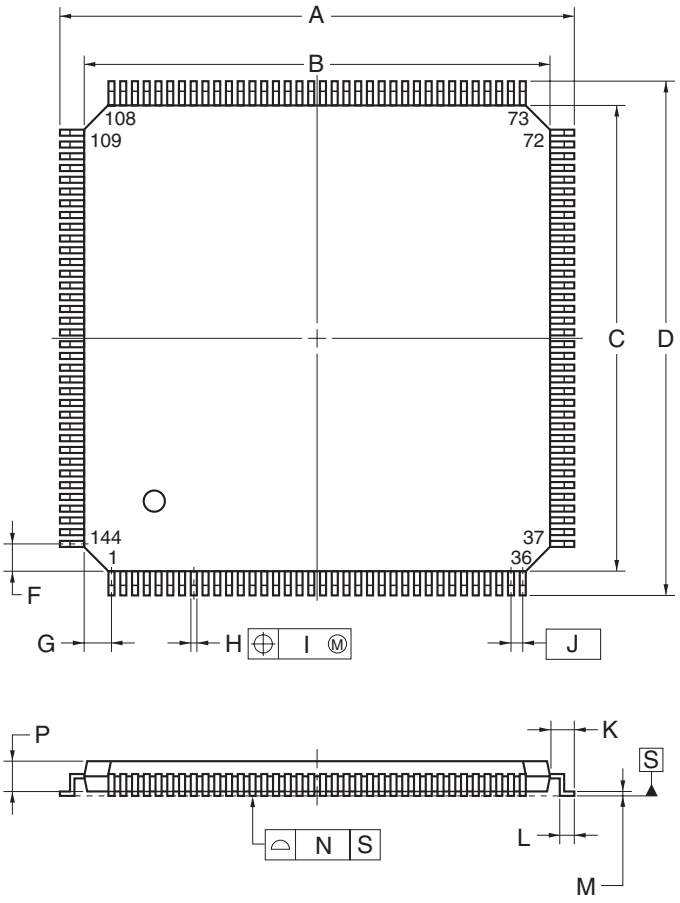
a. Pulses longer than this value will pass hte analog filter
b. Pulses shorter than this value do not pass the analog input filter. This characteristic is not tested in production, it is ensured by design and evaluated.

Notes: 1. These settings refer to INTP13 and INTP14 located on the isolated area
2. For figures please refer to 4.3 ”Interrupt Timing” on page 29

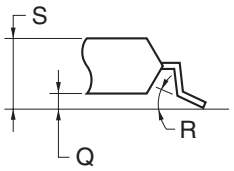
8. Package Drawings

Figure 8-1: V850E/CAG4-M

144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



detail of lead end



ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	20.0±0.2
D	22.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.4
Q	0.10±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.5±0.1

S144GJ-50-UEN

NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

Note: Copper lead frame with NiPdAu plating

[MEMO]

9. Revision History

This document is the first release of the V850CAG4-M Datasheet. The revision history of U18578EE1V0DS00 refers to the V850E/CAG4-M Electrical Target Specification EASE-ES-0009 V0.4.

Version	Chapter	Page	Remarks
	1	12	• Specification for storage temperature in Table 1-1 added
V.1.0	2	16	• Max. value for T_{OST} removed, replaced by typ. • Note regarding T_{OST} added
		17	• Specification for T_{SOST} removed from Table 2-2 • Note regarding T_{SOST} added
		18	CPU PLL output period jitter added to Table 2-4
	3	25	Chapter 'DC Characteristics for Pins Influenced by Injected Current on Adjacent Pin' removed
	4	27	Table 4-1: Turning On / Interception Timing • t_{WMRGD} removed, not applicable, timing included in t_{WMRPD} • t_{WMRPD} min. timing added
		28	Table 4-2: Turning On / Interception Timing • t_{WRPD} min. timing added • Table footer d) reference to main oscillator removed; not applicable for RESET
		30	CSIB Table 4-4 and Table 4-5 timings added
		33	CSIE timings • Caution regarding load added • Figure 4-12 CSIE AC Load Condition added
		33 - 35	Table 4-6 and Table 4-7 timings added
		-	Chapter 'External Asynchronous Memory' removed
	6	48-51	Flash Memory Characteristics; complete chapter extended • Code Flash Memory Characteristics • Data Flash Memory Characteristics
	7	52	• Specification for storage temperature in Table 7-1 added • Restriction for use of 32KHz sub-oscillator bellow 4.5V removed
		54	Table 7-7: Turning On / Interception Timing • t_{WRPD} min. timing added

Notes for CMOS Devices

1. **Precaution against ESD for semiconductors**
   Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

2. **Handling of unused input pins for CMOS**
   No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

3. **Status before initialization of MOS devices**
   Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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