NCV890103

1.2 A, 2 MHz Automotive Buck Switching Regulator with RSTB

The NCV890103 is a fixed−frequencyThrulatorThthat mtri operate th RSup to fi36 V input suppc63 2 isTJ21.00033Tc-..3560 [(Thsui systems. The NCV890103 is capable of converting the typical 4.5 V to 18 V automotive input voltage range to outputs as low as 3.3 V at a constant switching frequency above the sensitive AM band, eliminating the need for costly filters and EMI countermeasures. A Reset pin signals when the output is in regulation, and a pin is provided to adjust the delay before the RSTB signal goes high. The NCV890103 also provides several protection features expected in Automotive power supply systems such as current limit, short circuit protection, and thermal shutdown. In addition, the high switching frequency produces low output voltage ripple even when using small inductor values and an all−ceramic output filter capacitor − forming a space−efficient switching regulator solution.

Features

- Internal N−Channel Power Switch
- Low V_{IN} Operation Down to 4.5 V
- High V_{IN}

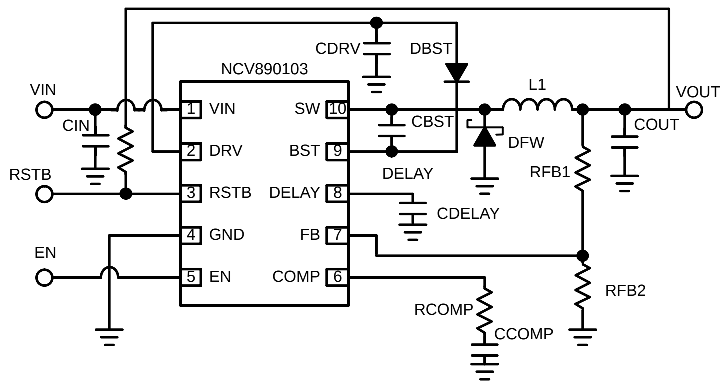


Figure 1. Typical Application

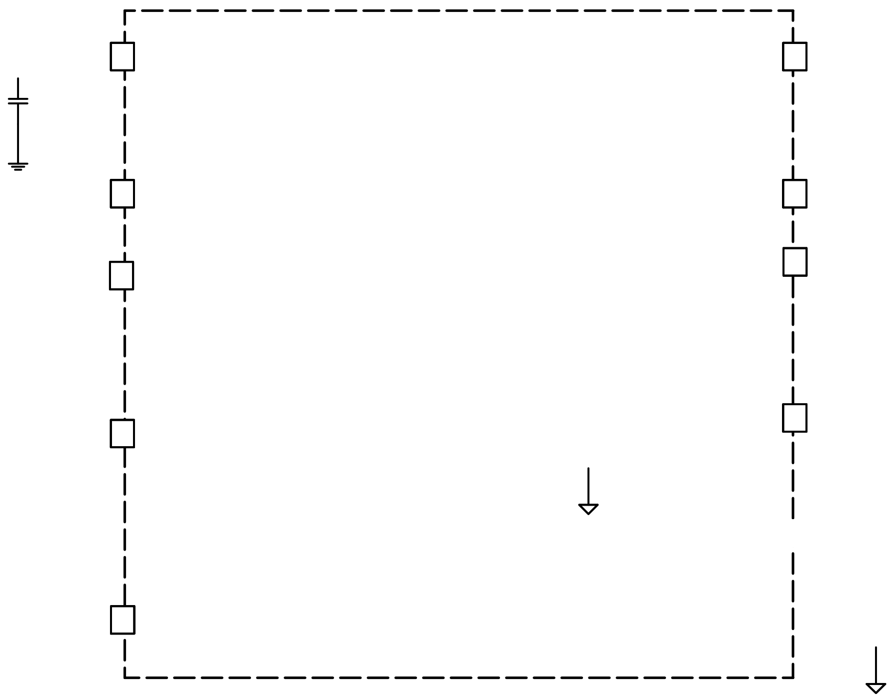
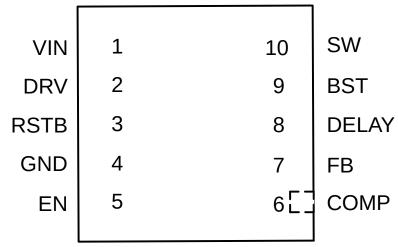


Figure 2. NCV890103 Block Diagram

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Min/Max Voltage VIN, BST		−0.3 to 40	V
Max Voltage VIN to SW		40	V
Min/Max Voltage SW		−0.7 to 40	V
Min Voltage SW − 20ns		−3.0	V
Min/Max Voltage BST to SW		−0.3 to 3.6	V
Min/Max Voltage on EN		−0.3 to 40	V
Min/Max Voltage COMP		−0.3 to 2	V
Min/Max Voltage FB		−0.3 to 18	V
Min/Max Voltage DRV, DELAY		−0.3 to 3.6	V
Min/Max Voltage RSTB		−0.3 to 6	V
Thermal Resistance, 3x3 DFN Junction−to−Ambient*	$R_{\theta JA}$	50	°C/W
Storage Temperature Range		−55 to +150	°C
Operating Junction Temperature Range	T_J	−40 to +150	°C
ESD withstand Voltage Human Body Model	V_{ESD}	 2.0	kV
Moisture Sensitivity	MSL	Level 1	
Peak Reflow Soldering Temperature		260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Mounted on 1 sq. in. of a 4−layer PCB with 1 oz. copper thickness.



(Top View)

Figure 3. Pin Connections

ELECTRICAL CHARACTERISTICS

(V_{IN} = 4.5 V to 28 V, V_{EN} = 5 V, V_{BST} = V_{SW} + 3.0 V, C_{DRV} = 0.1 μF, Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
QUIESCENT CURRENT						
Quiescent Current, shutdown	I_{qSD}	V_{IN} = 13.2 V, V_{EN} = 0 V, T_J = 25°C			5	μA
Quiescent Current, enabled	I_{qEN}	V_{IN} = 13.2 V			3	mA
UNDERVOLTAGE LOCKOUT − VIN (UVLO)						
UVLO Start Threshold	V_{UVLSTT}	V_{IN} rising	4.1		4.5	V
UVLO Stop Threshold	V_{UVLSTP}	V_{IN} falling	3.2		3.6	V
UVLO Hysteresis	V_{UVLOHY}		0.5		1.3	V
ENABLE (EN)						
Logic Low (Voltage input needed to guarantee logic low)	V_{ENLO}				0.8	V
Logic High (Voltage input needed to guarantee logic high)	V_{ENHI}					

ELECTRICAL CHARACTERISTICS (continued)
(V_{IN} = 4.5 V to 28 V, V_{EN} = 5 V, V_{BST} = V_{SW} + 3.0 V, C_{DRV} = 0.1 μF, Min/Max values are valid for the temperature range −40°C ≤ T_J ≤ 150°C unless noted otherwise, and are guaranteed by test, design or statistical correlation.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit

TYPICAL CHARACTERISTICS CURVES

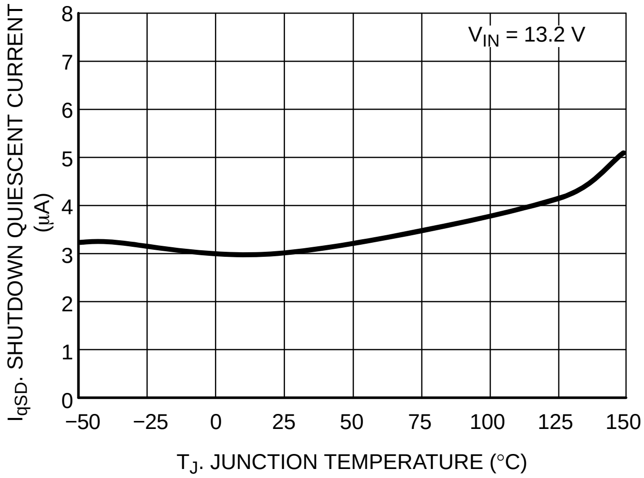


Figure 4. Shutdown Quiescent Current vs. Junction Temperature

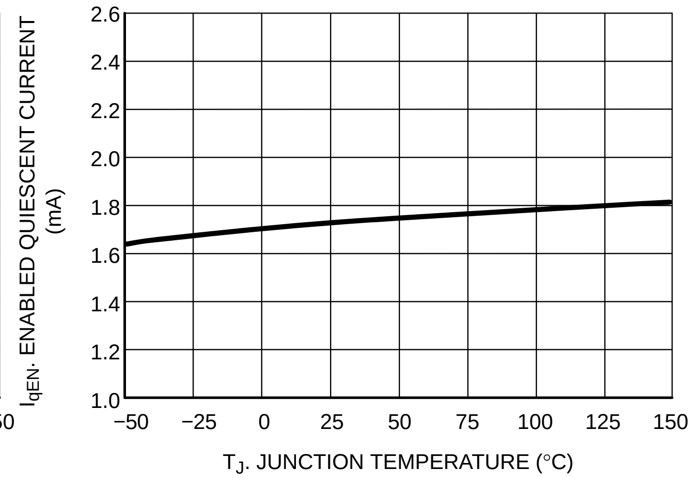


Figure 5. Enabled Quiescent Current vs. Junction Temperature

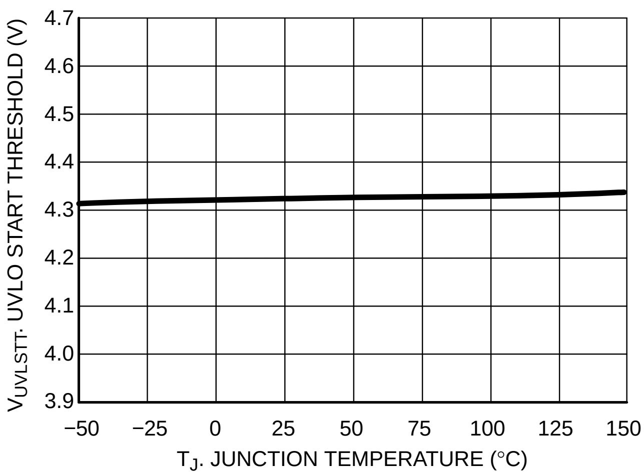


Figure 6. UVLO Start Threshold vs. Junction Temperature

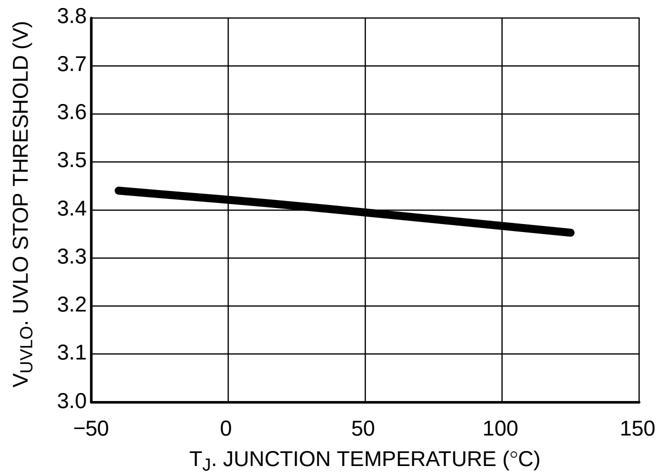


Figure 7. UVLO Stop Threshold vs. Junction Temperature

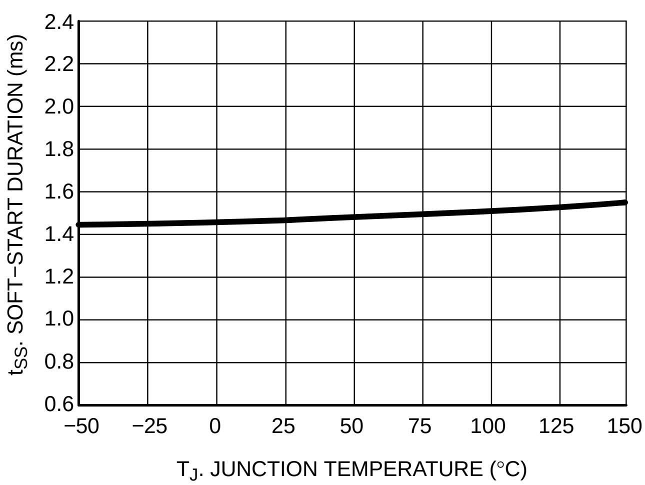


Figure 8. Soft−Start Duration vs. Junction Temperature

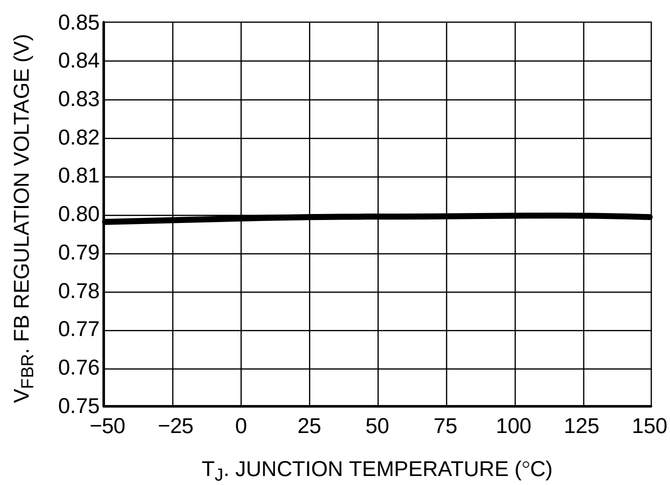
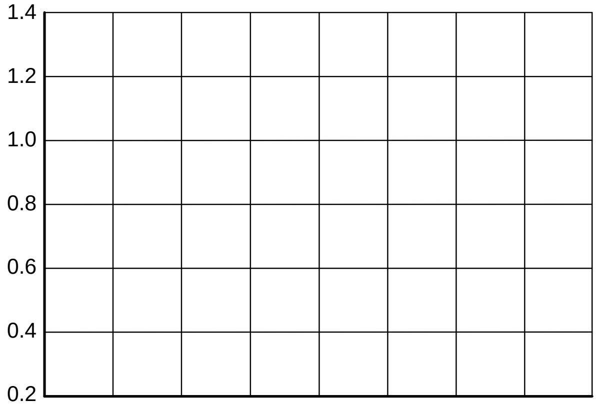


Figure 9. FB Regulation Voltage vs. Junction Temperature

TYPICAL CHARACTERISTICS CURVES



TYPICAL CHARACTERISTICS CURVES

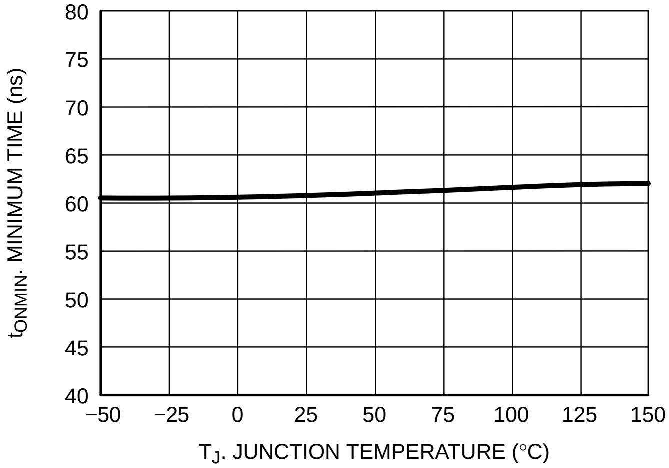


Figure 16. Minimum On Time vs. Junction Temperature

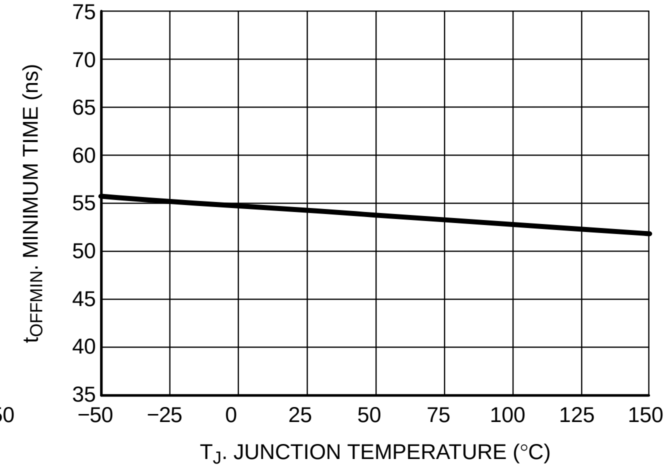


Figure 17. Minimum Off Time vs. Junction Temperature

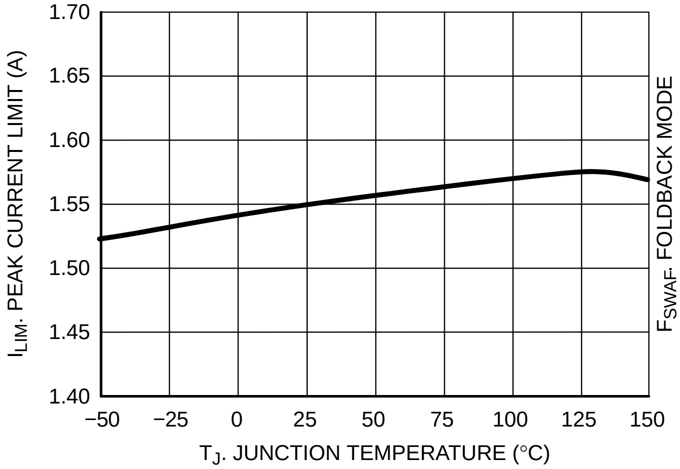


Figure 18. Current Limit Threshold vs. Junction Temperature

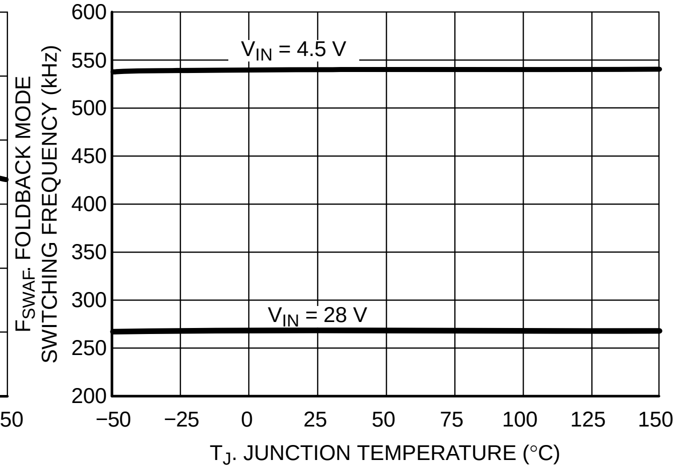
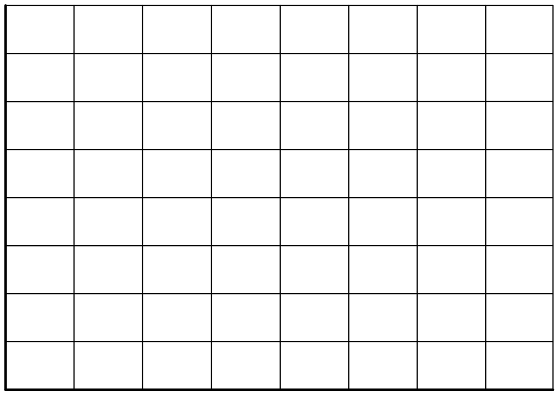


Figure 19. Short−Circuit Foldback Frequency vs. Junction Temperature



TYPICAL CHARACTERISTICS CURVES

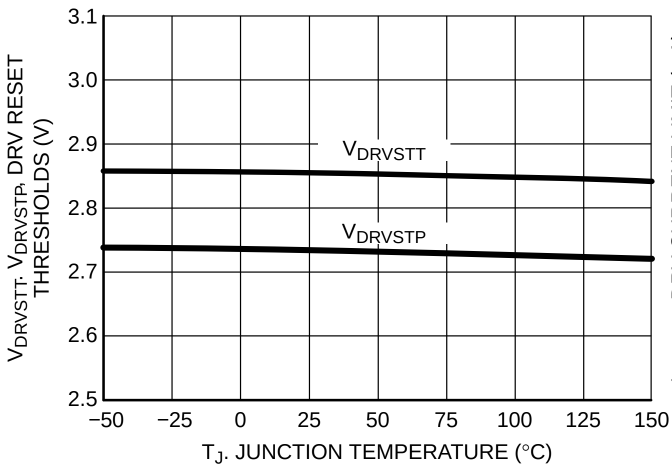


Figure 22. DRV Reset Threshold vs. Junction Temperature

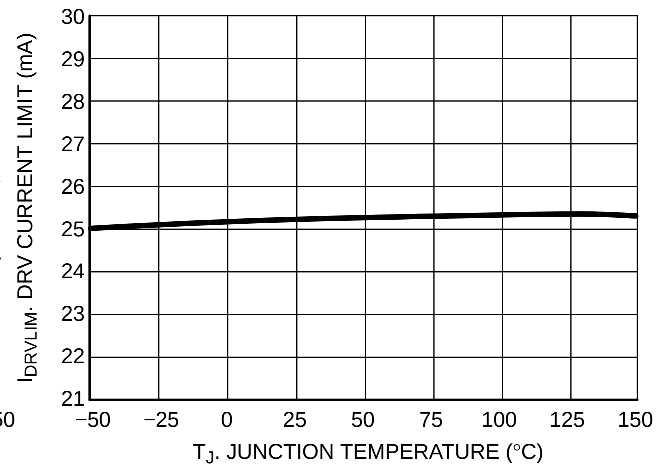


Figure 23. DRV Current Limit vs. Junction Temperature

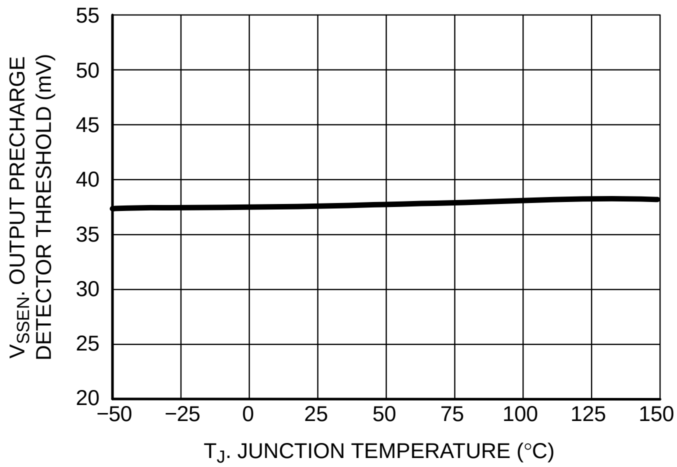


Figure 24. Output Precharge Detector Threshold vs. Junction Temperature

GENERAL INFORMATION

INPUT VOLTAGE

An Undervoltage Lockout (UVLO) circuit monitors the input, and inhibits switching and resets the Soft−start circuit if there is insufficient voltage for proper regulation. The NCV890103 can regulate a 3.3 V output with input voltages above 4.5 V and a 5.0 V output with an input above 6.5 V.

The NCV890103 withstands input voltages up to 40 V.

To limit the power lost in generating the drive voltage for the Power Switch, the switching frequency is reduced by a factor of 2 when the input voltage exceeds the V_{IN} Frequency Foldback threshold V_{FLDUP} (see Figure 25). Frequency reduction is automatically terminated when the input voltage drops back below the V_{IN} Frequency Foldback threshold V_{FLDDN}.

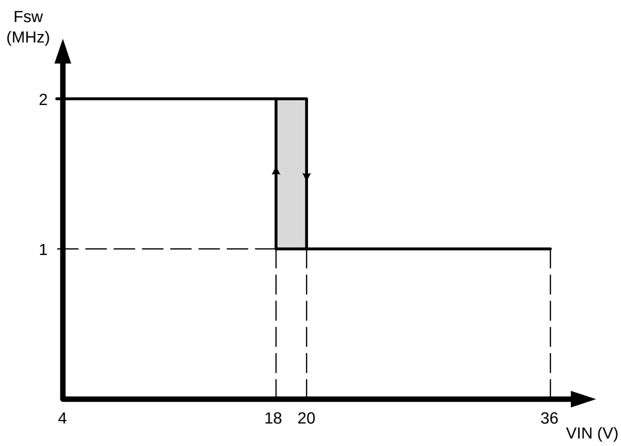
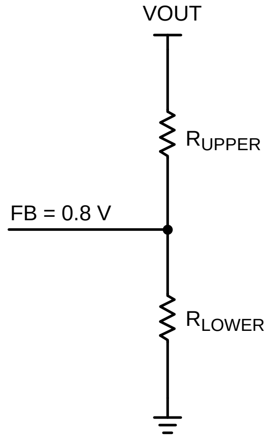


Figure 25. NCV890103 Switching Frequency Reduction at High Input Voltage

ENABLE

The NCV890103 is designed to accept either a logic level signal or battery voltage as an Enable signal. EN low induces a ’sleep mode’ whic282.82 -.9264oicietor a2-.0198 Tw(NCV8905 1 Tf10 0 0Tm86-.019856.7VIN (A typ termin(I0 0 8 203.300 cm 5.3623



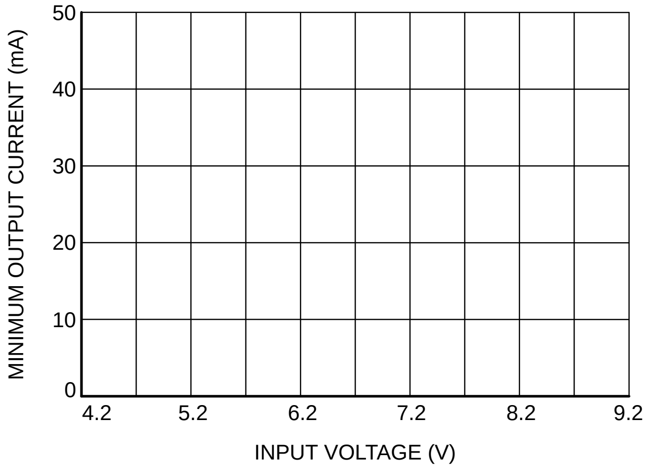
Use the following equation:

R

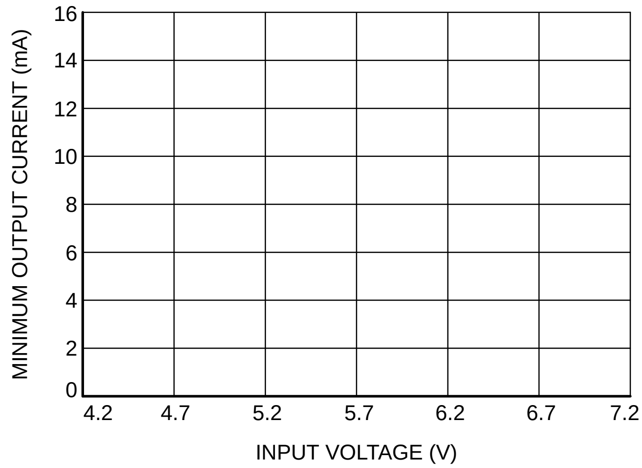
BOOTSTRAP

At the DRV pin an internal regulator provides a ground−referenced voltage to an external capacitor (C_{DRV}), to allow fast recharge of the external bootstrap capacitor (C_{BST}) used to supply power to the power switch gate driver. If the voltage at the DRV pin goes below the DRV UVLO Threshold V_{DRVSTP}, switching is inhibited and the Soft−start circuit is reset, until the DRV pin voltage goes back up above V_{DRVSTT}.

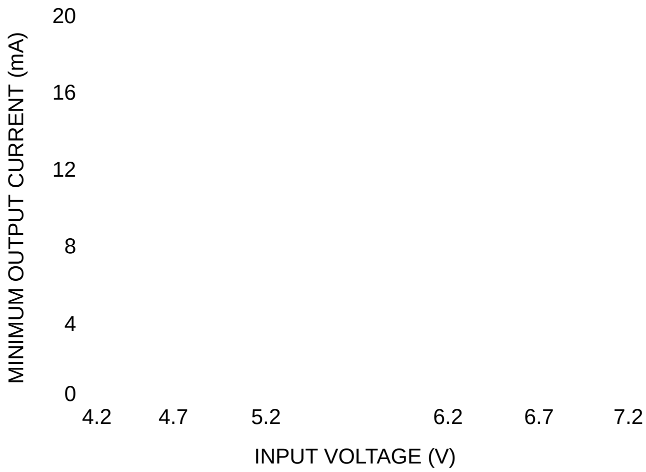
In order for the bootstrap capacitor to stay charged, the Switch node needs to be pulled down to ground regularly. In very light load condition, the NCV890103 skips switching cycles to ensure the output voltage stays regulated. When the skip cycle repetition frequency gets too low, the bootstrap voltage collapses and the regulator stops switching. Practically, this means that the NCV890103 needs a minimum load to operate correctly. Figure 28 shows the minimum current requirements for different input and output voltages.



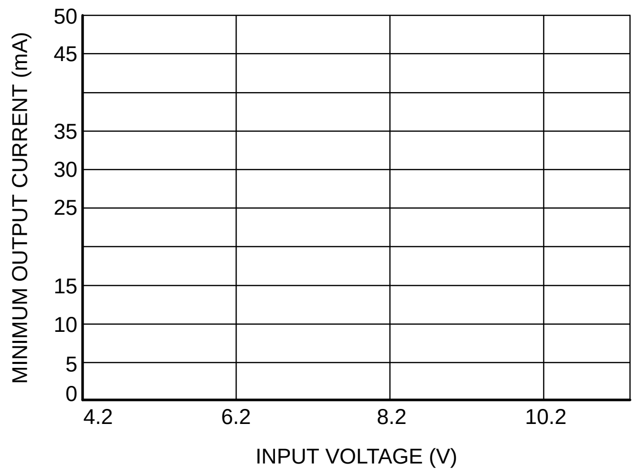
Minimum Load 5 V Out



Minimum Load 3.3 V Out



Minimum Load 3.7 V Out



Minimum Load 5.5 V Out

OUTPUT PRECHARGE DETECTION

Prior to Soft−start, the FB pin is monitored to ensure the SW voltage is low enough to have charged the external bootstrap capacitor (C_{BST}). If the FB pin is higher than V_{SSEN}, restart is delayed until the output has discharged. Figure 29 shows the IC starts to switch after the voltage on FB pin reaches VSSEN, even the EN pin is high. After the IC is switching, the FB pin follows the soft starts reference to reach the final set point.

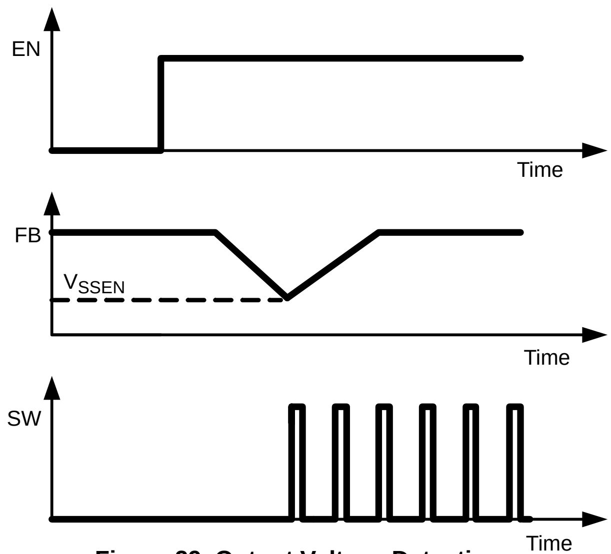


Figure 29. Output Voltage Detection

THERMAL SHUTDOWN

A thermal shutdown circuit inhibits switching, resets the Soft−start circuit, and removes DRV voltage if internal temperature exceeds a safe level. Switching is automatically restored when temperature returns to a safe level.

MINIMUM DROPOUT VOLTAGE

When operating at low input voltages, two parameters play a major role in imposing a minimum voltage drop across the regulator: the minimum off time (that sets the

As far as max ratings are concerned, the maximum reverse voltage the diode sees is the maximum input voltage (with some margin in case of ringing on the Switch node), and the maximum forward current the peak current limit of the NCV890103, I_{LIM}.

The power dissipated in the diode is P_{Dloss}:

$$P_{Dloss} = I_{OUT} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \cdot V_F + I_{DRMS} \cdot R_D \quad \text{(eq. 5)}$$

with:

- I_{OUT} the average (dc) output current
- V_F the forward voltage of the diode
- I_{DRMS} the RMS current in the diode:

$$I_{DRMS} = \sqrt{(1 - D)\left({I_{OUT}}^2 + \frac{{\Delta I_L}^2}{12}\right)} \quad \text{(eq. 6)}$$

- R_D the dynamic resistance of the diode (extracted from the V/I curve of the diode in its datasheet).

Then, knowing the thermal resistance of the package and the amount of heatsinking on the PCB, the temperature rise corresponding to this power dissipation can be estimated.

Input capacitor:

The input capacitor must sustain the RMS input ripple current I_{INac}:

$$I_{INac} = \frac{\Delta I_L}{2}\sqrt{\frac{D}{3}} \quad \text{(eq. 7)}$$

It can be designed in combination with an inductor to build an input filter to filter out the ripple current in the source, in order to reduce EMI conducted emissions.

For example, using a 4.7 μH input capacitor, it is easy to calculate that an inductor of 200 nH will ensure that the input filter has a cut−off frequency below 200 kHz (low enough to attenuate the 2 MHz ripple).

Error Amplifier and Loop Transfer Function

The error amplifier is a transconductance type amplifier. The output voltage of the error amplifier controls the peak inductor current at which the power switch shuts off. The Current Mode control method employed allows the use of a simple, type II compensation to optimize the dynamic response according to system requirements.

Figure 30 shows the error amplifier with the compensation components and the voltage feedback divider.

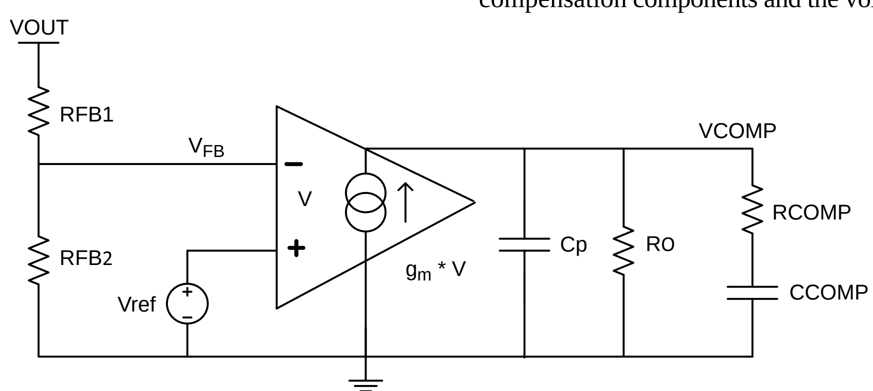


Figure 30. Feedback Compensator Network Model

The transfer function from VOUT to VCOMP is the product of the feedback voltage divider and the error amplifier.

$$\text{Gdivider}(s) = \frac{RFB2}{RFB1 + RFB2} \quad \text{(eq. 8)}$$

$$Gerr_{amp(s)} = gm \cdot Ro \cdot \frac{1 + \frac{s}{\omega z}}{\left(1 + \frac{s}{\omega pl}\right)\left(1 + \frac{s}{\omega ph}\right)} \quad \text{(eq. 9)}$$

$$\omega z = \frac{1}{RCOMP \cdot CCOMP} \quad \text{(eq. 10)}$$

$$\omega pl = \frac{1}{Ro \cdot CCOMP} \quad \text{(eq. 11)}$$

$$\omega ph = \frac{1}{RCOMP \cdot Cp} \quad \text{(eq. 12)}$$

The output resistor Ro of the error amplifier is 1.4 MΩ and gm is 1 mA/V. The capacitor Cp is for rejecting noise at high frequency and is integrated inside the IC with a value of 18 pF.

The power stage transfer function (from Vcomp to output) is shown below:

$$Gps(s) = \frac{Rload}{Ri} \cdot \frac{1}{1 + \frac{Rload \cdot Tsw}{L} \cdot [Mc \cdot (1 - D) - 0.5]} \cdot \frac{1 + \frac{s}{\omega z}}{\left(1 + \frac{s}{\omega p}\right)} \cdot Fh(s) \quad \text{(eq. 13)}$$

$$\omega z = \frac{1}{Resr \cdot Cout} \quad \text{(eq. 14)}$$

$$\omega p = \frac{1}{Rload \cdot Cout} + \frac{Mc \cdot (1 - D) - 0.5}{L \cdot Cout \cdot Fsw} \quad \text{(eq. 15)}$$

where

$$Mc = 1 + \frac{Se}{Sn} \quad \text{(eq. 16)}$$

$$Sn = \frac{Vin - Vout}{L} \cdot Ri \quad \text{(eq. 17)}$$

Ri represents the equivalent sensing resistor which has a value of 0.31 Ω, Se is the compensation slope which is 700 kV/S, Sn is the slope of the sensing resistor current during on time. Fh(s) represents the sampling effect from the current loop which has two poles at one half of the switching frequency:

$$Fh(s) = \frac{1}{1 + \frac{s}{\omega n \cdot Qp}}$$

From the calculation:

RCOMP = 11.3 KΩ, CCOMP = 2 nF, Cp = 28 pF

So the feedback compensation network is as below:

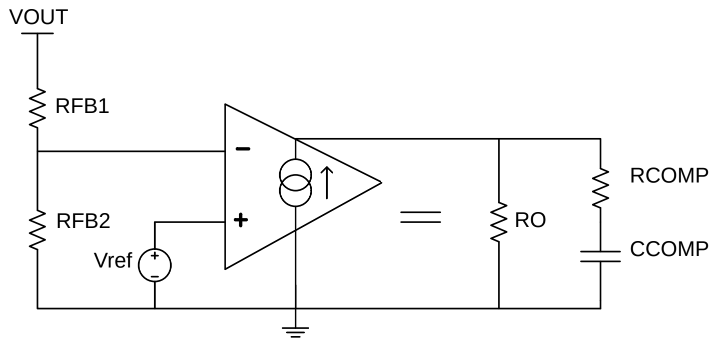


Figure 32. Example of the Feedback Compensation Network

PCB LAYOUT RECOMMENDATION

As with any switching power supplies, there are some guidelines to follow to optimize the layout of the printed circuit board for the NCV890103. However, because of the high switching frequency extra care has to be taken.

− Minimize the area of the power current loops:
  - Input capacitor → NCV890103 switch → Inductor → output capacitor → return through Ground
  - Freewheeling diode → inductor → Output capacitor → return through ground

− Minimize the length of high impedance signals, and route them far away from the power loops:
  - Feedback trace
  - Comp trace

ORDERING INFORMATION

Device	Package	Shipping†
NCV890103MWTXG	DFN10 with wettable flanks (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DFN10, 3x3, 0.5P
CASE 485C
ISSUE C