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**PRELIMINARY DATASHEET**

**DATASHEET**

**PRODUCT :**

64M (x16) Flash + 64M (x16) Flash  
32M (x16) SCRAM + 8M (x16) SRAM

**MODEL No :**

***LRS1B12***

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## LRS1B12

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## 1. Description

The LRS1B12 is a combination memory organized as 4,194,304 x16 bit flash memory, 4,194,304 x16 bit flash memory, 2,097,152 x16 bit Smartcombo RAM and 524,288 x16 bit static RAM in one package.

### Features

- Power supply . . . . . 2.7V to 3.1V
- Operating temperature . . . . . -25°C to +85°C
- Not designed or rated as radiation hardened
- 72 pin CSP(LCSP072-P-0811) plastic package
- Flash memory has P-type bulk silicon, and Smartcombo RAM has P-type bulk silicon, and SRAM has P-type bulk silicon
- Flash memory and Smartcombo RAM share one power supply pin (F/SC-V<sub>CC</sub>)
- For specifications of Flash memory, Smartcombo RAM and SRAM, refer to specification of each chip

### Standby current of Flash memory and Smartcombo RAM

- Power supply current . . . . . 150  $\mu$ A (Max.)

### Flash Memory 1 (F<sub>1</sub>: 64M (x16) bit Flash Memory)

- Access Time (Address) . . . . . 65 ns (Max.)
- Power supply current (The current for F/SC-V<sub>CC</sub> pin and V<sub>PP</sub> pin)
  - Read . . . . . 25 mA (Max. t<sub>CYCLE</sub> = 200ns, CMOS Input)
  - Word write . . . . . 60 mA (Max.)
  - Block erase . . . . . 30 mA (Max.)

### Flash Memory 2 (F<sub>2</sub>: 64M (x16) bit Flash Memory)

- Access Time (Address) . . . . . 65 ns (Max.)
- Power supply current (The current for F/SC-V<sub>CC</sub> pin and V<sub>PP</sub> pin)
  - Read . . . . . 25 mA (Max. t<sub>CYCLE</sub> = 200ns, CMOS Input)
  - Word write . . . . . 60 mA (Max.)
  - Block erase . . . . . 30 mA (Max.)

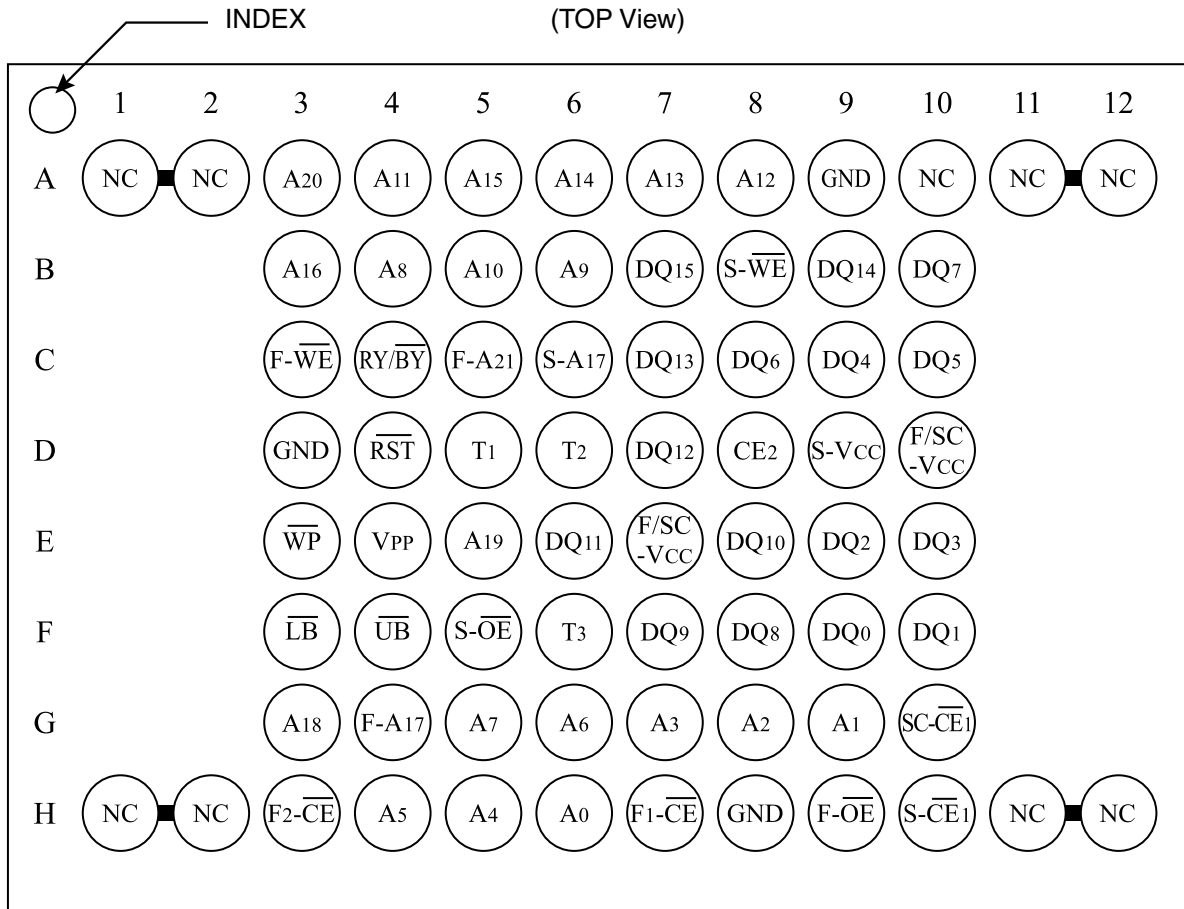
### Smartcombo RAM (32M (x16) bit Smartcombo RAM)

- Access Time (Address) . . . . . 65 ns (Max.)
- Cycle time . . . . . 65 ns (Min.)
- Power Supply current
  - Operating current . . . . . 50 mA (Max. t<sub>RC</sub>, t<sub>WC</sub> = Min.)

### SRAM (8M (x16) bit SRAM)

- Access Time (Address) . . . . . 65 ns (Max.)
- Power Supply current
  - Operating current . . . . . 45 mA (Max. t<sub>RC</sub>, t<sub>WC</sub> = Min.)
  - Standby current . . . . . 15  $\mu$ A (Max.)

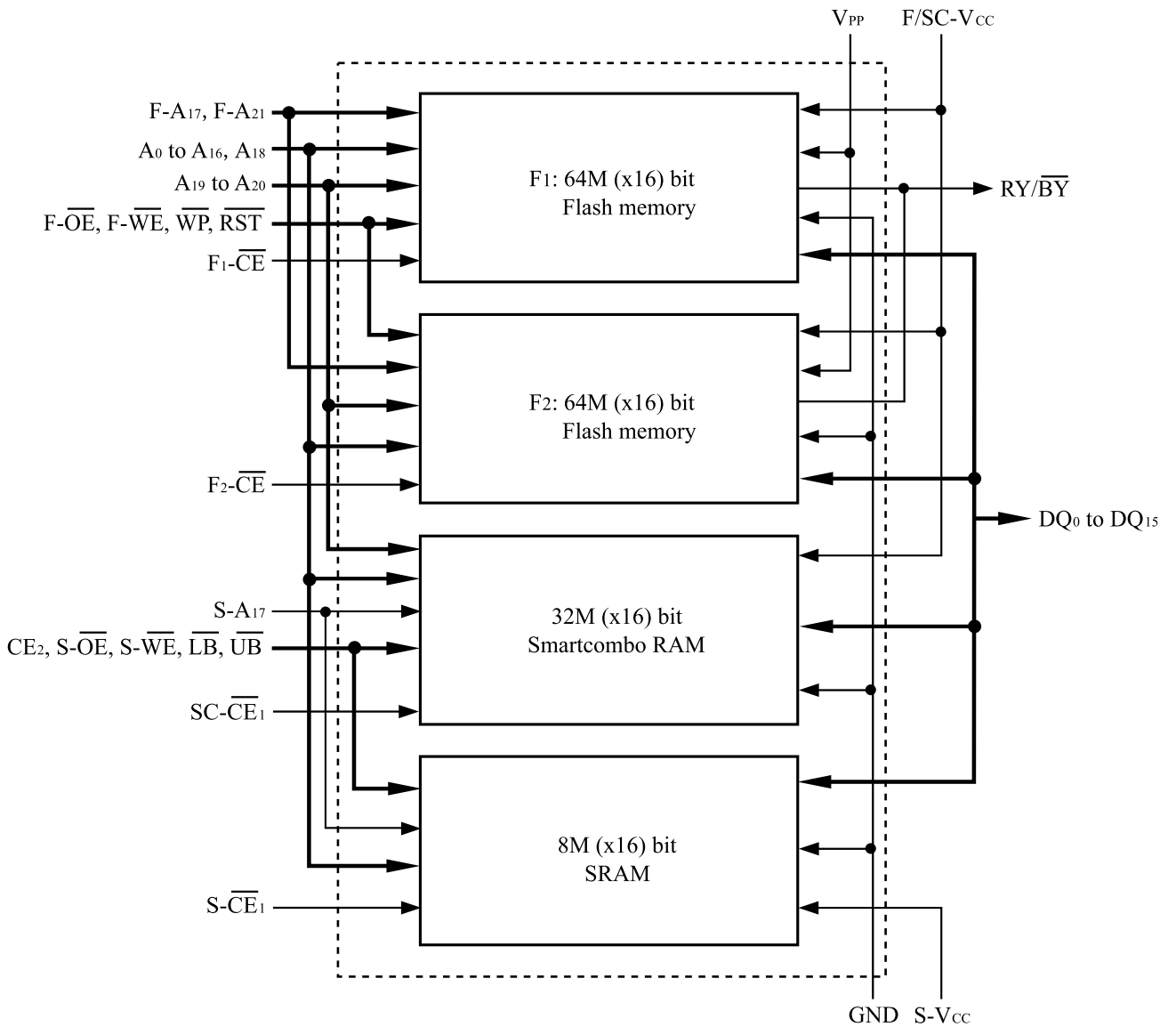
## 2. Pin Configuration



Note) From T1 to T3 pins are needed to be open.  
 Two NC pins at the corner are connected.  
 Do not float any GND pins.

Pin	Description	Type
A <sub>0</sub> to A <sub>16</sub> , A <sub>18</sub>	Address Inputs (Common)	Input
A <sub>19</sub> to A <sub>20</sub>	Address Inputs (Flash, Smartcombo RAM)	Input
F-A <sub>17</sub> , F-A <sub>21</sub>	Address Inputs (Flash)	Input
S-A <sub>17</sub>	Address Input (SRAM, Smartcombo RAM)	Input
F <sub>1</sub> - $\overline{\text{CE}}$	Chip Enable Input (Flash - F <sub>1</sub> Selected)	Input
F <sub>2</sub> - $\overline{\text{CE}}$	Chip Enable Input (Flash - F <sub>2</sub> Selected)	Input
SC- $\overline{\text{CE}}_1$	Chip Enable Input (Smartcombo RAM)	Input
S- $\overline{\text{CE}}_1$	Chip Enable Input (SRAM)	Input
CE <sub>2</sub>	Chip Enable Input (SRAM), Sleep State Input (Smartcombo RAM) * See Chapter B-1	Input
F- $\overline{\text{WE}}$	Write Enable Input (Flash)	Input
S- $\overline{\text{WE}}$	Write Enable Input (SRAM, Smartcombo RAM)	Input
F- $\overline{\text{OE}}$	Output Enable Input (Flash)	Input
S- $\overline{\text{OE}}$	Output Enable Input (SRAM, Smartcombo RAM)	Input
$\overline{\text{LB}}$	SRAM, Smartcombo RAM Byte Enable Input (DQ <sub>0</sub> to DQ <sub>7</sub> )	Input
$\overline{\text{UB}}$	SRAM, Smartcombo RAM Byte Enable Input (DQ <sub>8</sub> to DQ <sub>15</sub> )	Input
$\overline{\text{RST}}$	Reset Power Down Input (Flash) Block erase and Write : V <sub>IH</sub> Read : V <sub>IH</sub> Reset Power Down : V <sub>IL</sub>	Input
$\overline{\text{WP}}$	Write Protect Input (Flash) When $\overline{\text{WP}}$ is V <sub>IL</sub> , locked-down blocks cannot be unlocked. Erase or program operation can be executed to the blocks which are not locked and locked-down. When $\overline{\text{WP}}$ is V <sub>IH</sub> , lock-down is disabled.	Input
RY/ $\overline{\text{BY}}$	Ready/Busy Output (Flash) During an Erase or Write operation : V <sub>OL</sub> Block Erase and Write Suspend : High-Z (High impedance)	Open Drain Output
DQ <sub>0</sub> to DQ <sub>15</sub>	Data Inputs and Outputs (Common)	Input / Output
F/SC-V <sub>CC</sub>	Power Supply (Flash, Smartcombo RAM)	Power
S-V <sub>CC</sub>	Power Supply (SRAM)	Power
V <sub>PP</sub>	Monitoring Power Supply Voltage (Flash) Block Erase and Write : V <sub>PP</sub> = V <sub>PPH</sub> All Blocks Locked : V <sub>PP</sub> < V <sub>PPLK</sub>	Input
GND	GND (Common)	Power
NC	Non Connection	-
T <sub>1</sub> to T <sub>3</sub>	Test pins (Should be all open)	-

## 3. Block Diagram



Note: Only one among F1-CE, F2-CE, SC-CE<sub>1</sub> and S-CE<sub>1</sub> can be "low".  
Two or more should not be "low".



## 4. Absolute Maximum Ratings

Symbol	Parameter	Notes	Ratings	Unit
$V_{CC}$	Supply Voltage	1	-0.2 to +3.9	V
$V_{IN}$	Input Voltage	1,2,3	-0.5 to $V_{CC} + 0.3$	V
$T_A$	Operating Temperature		-25 to +85	°C
$T_{STG}$	Storage Temperature		-55 to +125	°C
$V_{PP}$	$V_{PP}$ Voltage	1,2	-0.2 to +3.6	V

Notes:

1. The maximum applicable voltage on any pins with respect to GND.
2. -1.0V undershoot is allowed when the pulse width is less than 5 nsec.
3.  $V_{IN}$  should not be over  $V_{CC} + 0.3V$ .

## 5. Recommended DC Operating Conditions

 $(T_A = -25^{\circ}C$  to  $+85^{\circ}C)$ 

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit
$V_{CC}$	Supply Voltage	3	2.7		3.1	V
$V_{PP}$	$V_{PP}$ Voltage (Write Operation)		1.65		3.1	V
	$V_{PP}$ Voltage (Read Operation)		0		3.1	V
$V_{IH}$	Input Voltage		$V_{CC} - 0.4$ <sup>(2)</sup>		$V_{CC} + 0.3$ <sup>(1)</sup>	V
$V_{IL}$	Input Voltage		-0.3		0.4	V

Notes:

1.  $V_{CC}$  is the lower of F/SC- $V_{CC}$  or S- $V_{CC}$ .
2.  $V_{CC}$  is the higher of F/SC- $V_{CC}$  or S- $V_{CC}$ .
3.  $V_{CC}$  includes both F/SC- $V_{CC}$  and S- $V_{CC}$ .

## 6. Flash Memory 1

## 6.1 Truth Table

6.1.1 Bus Operation <sup>(1)</sup>

Flash	Notes	F <sub>1</sub> - $\overline{\text{CE}}$	$\overline{\text{RST}}$	F- $\overline{\text{OE}}$	F- $\overline{\text{WE}}$	DQ <sub>0</sub> to DQ <sub>15</sub>
Read	3,5	L	H	L	H	(7)
Output Disable	5			H		High - Z
Write	2,3,4,5			L	D <sub>IN</sub>	
Standby	5	H	H	X	X	High - Z
Reset Power Down	5,6	X	L			

## Notes:

1. L = V<sub>IL</sub>, H = V<sub>IH</sub>, X = H or L, High-Z = High impedance. Refer to the DC Characteristics.
2. Command writes involving block erase, full chip erase, (page buffer) program are reliably executed when V<sub>PP</sub> = V<sub>PPH</sub> and V<sub>CC</sub> = 2.7V to 3.1V.  
Block erase, full chip erase, (page buffer) program with V<sub>PP</sub> < V<sub>PPH</sub> (Min.) produce spurious results and should not be attempted.
3. Never hold F- $\overline{\text{OE}}$  low and F- $\overline{\text{WE}}$  low at the same timing.
4. Refer to Section 6.2 Command Definitions for Flash Memory valid D<sub>IN</sub> during a write operation.
5.  $\overline{\text{WP}}$  set to V<sub>IL</sub> or V<sub>IH</sub>.
6. Electricity consumption of Flash Memory is lowest when  $\overline{\text{RST}}$  = GND ±0.2V.
7. Flash Read Mode

Mode	Address	DQ <sub>0</sub> to DQ <sub>15</sub>
Read Array	X	D <sub>OUT</sub>
Read Identifier Codes	See 6.2.2	See 6.2.2
Read Query	Refer to the Appendix	Refer to the Appendix

6.1.2 Simultaneous Operation Modes Allowed with Four Planes <sup>(1,2)</sup>

IF ONE PARTITION IS:	THEN THE MODES ALLOWED IN THE OTHER PARTITION IS:									
	Read Array	Read ID	Read Status	Read Query	Word Program	Page Buffer Program	Block Erase	Full Chip Erase	Program Suspend	Block Erase Suspend
Read Array	X	X	X	X	X	X	X		X	X
Read ID	X	X	X	X	X	X	X		X	X
Read Status	X	X	X	X	X	X	X	X	X	X
Read Query	X	X	X	X	X	X	X		X	X
Word Program	X	X	X	X						X
Page Buffer Program	X	X	X	X						X
Block Erase	X	X	X	X						
Full Chip Erase			X							
Program Suspend	X	X	X	X						X
Block Erase Suspend	X	X	X	X	X	X			X	

## Notes:

1. "X" denotes the operation available.
2. Configurative Partition Dual Work Restrictions:  
 Status register reflects partition state, not WSM (Write State Machine) state - this allows a status register for each partition.  
 Only one partition can be erased or programmed at a time - no command queuing.  
 Commands must be written to an address within the block targeted by that command.

6.2 Command Definitions for Flash Memory <sup>(11)</sup>

## 6.2.1 Command Definitions

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper <sup>(1)</sup>	Address <sup>(2)</sup>	Data	Oper <sup>(1)</sup>	Address <sup>(2)</sup>	Data <sup>(3)</sup>
Read Array	1		Write	PA	FFH			
Read Identifier Codes	≥ 2	4	Write	PA	90H	Read	IA	ID
Read Query	≥ 2	4	Write	PA	98H	Read	QA	QD
Read Status Register	2		Write	PA	70H	Read	PA	SRD
Clear Status Register	1		Write	PA	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Full Chip Erase	2	5, 9	Write	X	30H	Write	X	D0H
Program	2	5, 6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥ 4	5, 7	Write	WA	E8H	Write	WA	N-1
Block Erase and (Page Buffer) Program Suspend	1	8, 9	Write	PA	B0H			
Block Erase and (Page Buffer) Program Resume	1	8, 9	Write	PA	D0H			
Set Block Lock Bit	2		Write	BA	60H	Write	BA	01H
Clear Block Lock Bit	2	10	Write	BA	60H	Write	BA	D0H
Set Block Lock-down Bit	2		Write	BA	60H	Write	BA	2FH
Set Partition Configuration Register	2		Write	PCRC	60H	Write	PCRC	04H

## Notes:

- Bus operations are defined in 6.1.1 Bus Operation.
- All addresses which are written at the first bus cycle should be the same as the addresses which are written at the second bus cycle.  
X=Any valid address within the device.  
PA=Address within the selected partition.  
IA=Identifier codes address (See 6.2.2 Identifier Codes for Read Operation).  
QA=Query codes address. Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.  
BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.  
WA=Address of memory location for the Program command or the first address for the Page Buffer Program command.  
PCRC=Partition configuration register code presented on the address A<sub>0</sub>-A<sub>15</sub>.
- ID=Data read from identifier codes (See 6.2.2 Identifier Codes for Read Operation).  
QD=Data read from query database. Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.  
SRD=Data read from status register. See 6.3 Register Definition for a description of the status register bits.  
WD=Data to be programmed at location WA. Data is latched on the rising edge of F- $\overline{WE}$  or F<sub>1</sub>- $\overline{CE}$  (whichever goes high first) during command write cycles.  
N-1=N is the number of the words to be loaded into a page buffer.
- Following the Read Identifier Codes command, read operations access manufacturer code, device code, block lock configuration code, partition configuration register code (See 6.2.2 Identifier Codes for Read Operation).  
The Read Query command is available for reading CFI (Common Flash Interface) information.
- Block erase, full chip erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when  $\overline{RST}$  is V<sub>IH</sub>.
- Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
- Following the third bus cycle, input the program sequential address and write data of "N" times. Finally, input the any valid address within the target block to be programmed and the confirm command (D0H). Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.

8. If the program operation in one partition is suspended and the erase operation in other partition is also suspended, the suspended program operation should be resumed first, and then the suspended erase operation should be resumed next.
9. Full chip erase operation can not be suspended.
10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when  $\overline{WP}$  is  $V_{IL}$ .  
When  $\overline{WP}$  is  $V_{IH}$ , lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
11. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

## 6.2.2 Identifier Codes for Read Operation

	Code	Address [A <sub>15</sub> -A <sub>0</sub> ]	Data [DQ <sub>15</sub> -DQ <sub>0</sub> ]	Notes
Manufacturer Code	Manufacturer Code	0000H	00B0H	4
Device Code	64M (x16) Bottom Parameter Device Code	0001H	00B1H	1, 4
Block Lock Configuration Code	Block is Unlocked	Block Address + 2	DQ <sub>0</sub> = 0	2
	Block is Locked		DQ <sub>0</sub> = 1	2
	Block is not Locked-Down		DQ <sub>1</sub> = 0	2
	Block is Locked-Down		DQ <sub>1</sub> = 1	2
Device Configuration Code	Partition Configuration Register	0006H	PCRC	3, 4

## Notes:

1. Bottom parameter device has its parameter blocks in the plane 0 (The lowest address).
2. Block Address = The beginning location of a block address within the partition to which the Read Identifier Codes command (90H) has been written.  
DQ<sub>15</sub>-DQ<sub>2</sub> is reserved for future implementation.
3. PCRC = Partition Configuration Register Code.
4. The address A<sub>21</sub>-A<sub>16</sub> are shown in below table for reading the manufacturer, device, device configuration code.  
The address to read the identifier codes is dependent on the partition which is selected when writing the Read Identifier Codes command (90H).  
See Section 6.3 Partition Configuration Register Definition (P.17) for the partition configuration register.

## Identifier Codes for Read Operation on Partition Configuration (64M (x16)-bit device)

Partition Configuration Register			Address (64M (x16)-bit device)
PCR.10	PCR.9	PCR.8	[A <sub>21</sub> -A <sub>16</sub> ]
0	0	0	00H
0	0	1	00H or 10H
0	1	0	00H or 20H
1	0	0	00H or 30H
0	1	1	00H or 10H or 20H
1	1	0	00H or 20H or 30H
1	0	1	00H or 10H or 30H
1	1	1	00H or 10H or 20H or 30H

## 6.2.3 Functions of Block Lock and Block Lock-Down

Current State					Erase/Program Allowed <sup>(2)</sup>
State	$\overline{WP}$	$DQ_1^{(1)}$	$DQ_0^{(1)}$	State Name	
[000]	0	0	0	Unlocked	Yes
[001] <sup>(3)</sup>	0	0	1	Locked	No
[011]	0	1	1	Locked-down	No
[100]	1	0	0	Unlocked	Yes
[101] <sup>(3)</sup>	1	0	1	Locked	No
[110] <sup>(4)</sup>	1	1	0	Lock-down Disable	Yes
[111]	1	1	1	Lock-down Disable	No

## Notes:

- $DQ_0 = 1$ : a block is locked;  $DQ_0 = 0$ : a block is unlocked.  
 $DQ_1 = 1$ : a block is locked-down;  $DQ_1 = 0$ : a block is not locked-down.
- Erase and program are general terms, respectively, to express: block erase, full chip erase and (page buffer) program operations.
- At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] ( $\overline{WP} = 0$ ) or [101] ( $\overline{WP} = 1$ ), regardless of the states before power-off or reset operation.
- When  $\overline{WP}$  is driven to  $V_{IL}$  in [110] state, the state changes to [011] and the blocks are automatically locked.

6.2.4 Block Locking State Transitions upon Command Write <sup>(4)</sup>

Current State				Result after Lock Command Written (Next State)		
State	$\overline{WP}$	$DQ_1$	$DQ_0$	Set Lock <sup>(1)</sup>	Clear Lock <sup>(1)</sup>	Set Lock-down <sup>(1)</sup>
[000]	0	0	0	[001]	No Change	[011] <sup>(2)</sup>
[001]	0	0	1	No Change <sup>(3)</sup>	[000]	[011]
[011]	0	1	1	No Change	No Change	No Change
[100]	1	0	0	[101]	No Change	[111] <sup>(2)</sup>
[101]	1	0	1	No Change	[100]	[111]
[110]	1	1	0	[111]	No Change	[111] <sup>(2)</sup>
[111]	1	1	1	No Change	[110]	No Change

## Notes:

- “Set Lock” means Set Block Lock Bit command, “Clear Lock” means Clear Block Lock Bit command and “Set Lock-down” means Set Block Lock-Down Bit command.
- When the Set Block Lock-Down Bit command is written to the unlocked block ( $DQ_0 = 0$ ), the corresponding block is locked-down and automatically locked at the same time.
- “No Change” means that the state remains unchanged after the command written.
- In this state transitions table, assumes that  $\overline{WP}$  is not changed and fixed  $V_{IL}$  or  $V_{IH}$ .

6.2.5 Block Locking State Transitions upon  $\overline{WP}$  Transition <sup>(4)</sup>

Previous State	Current State				Result after $\overline{WP}$ Transition (Next State)	
	State	$\overline{WP}$	DQ <sub>1</sub>	DQ <sub>0</sub>	$\overline{WP} = 0 \rightarrow 1$ <sup>(1)</sup>	$\overline{WP} = 1 \rightarrow 0$ <sup>(1)</sup>
-	[000]	0	0	0	[100]	-
-	[001]	0	0	1	[101]	-
[110] <sup>(2)</sup>	[011]	0	1	1	[110]	-
Other than [110] <sup>(2)</sup>					[111]	-
-	[100]	1	0	0	-	[000]
-	[101]	1	0	1	-	[001]
-	[110]	1	1	0	-	[011] <sup>(3)</sup>
-	[111]	1	1	1	-	[011]

Notes:

1. " $\overline{WP} = 0 \rightarrow 1$ " means that  $\overline{WP}$  is driven to  $V_{IH}$  and " $\overline{WP} = 1 \rightarrow 0$ " means that  $\overline{WP}$  is driven to  $V_{IL}$ .
2. State transition from the current state [011] to the next state depends on the previous state.
3. When  $\overline{WP}$  is driven to  $V_{IL}$  in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.



## 6.3 Register Definition

## Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BEFCES	PBPS	VPPS	PBPSS	DPS	R
7	6	5	4	3	2	1	0

SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

SR.7 = WRITE STATE MACHINE STATUS (WSMS)

- 1 = Ready
- 0 = Busy

SR.6 = BLOCK ERASE SUSPEND STATUS (BESS)

- 1 = Block Erase Suspended
- 0 = Block Erase in Progress/Completed

SR.5 = BLOCK ERASE AND FULL CHIP ERASE STATUS (BEFCES)

- 1 = Error in Block Erase or Full Chip Erase
- 0 = Successful Block Erase or Full Chip Erase

SR.4 = (PAGE BUFFER) PROGRAM STATUS (PBPS)

- 1 = Error in (Page Buffer) Program
- 0 = Successful (Page Buffer) Program

SR.3 = V<sub>PP</sub> STATUS (VPPS)

- 1 = V<sub>PP</sub> LOW Detect, Operation Abort
- 0 = V<sub>PP</sub> OK

SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS)

- 1 = (Page Buffer) Program Suspended
- 0 = (Page Buffer) Program in Progress/Completed

SR.1 = DEVICE PROTECT STATUS (DPS)

- 1 = Erase or Program Attempted on a Locked Block, Operation Abort
- 0 = Unlocked

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

Notes:

Status Register indicates the status of the partition, not WSM (Write State Machine). Even if the SR.7 is "1", the WSM may be occupied by the other partition when the device is set to 2, 3 or 4 partitions configuration.

Check SR.7 or RY/ $\overline{\text{BY}}$  to determine block erase, full chip erase, (page buffer) program completion. SR.6 - SR.1 are invalid while SR.7 = "0".

If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (page buffer) program, set/clear block lock bit, set block lock-down bit or set partition configuration register attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of V<sub>PP</sub> level. The WSM interrogates and indicates the V<sub>PP</sub> level only after Block Erase, Full Chip Erase, (Page Buffer) Program command sequences. SR.3 is not guaranteed to report accurate feedback when V<sub>PP</sub> ≠ V<sub>PPH</sub> or V<sub>PPLK</sub>.

SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, (Page Buffer) Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes command indicates block lock bit status.

SR.15 - SR.8 and SR.0 are reserved for future use and should be masked out when polling the status register.

## Extended Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

XSR.15-8 = RESERVED FOR FUTURE  
ENHANCEMENTS (R)

XSR.7 = STATE MACHINE STATUS (SMS)  
1 = Page Buffer Program available  
0 = Page Buffer Program not available

XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

## Notes:

After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not.

XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.

## Partition Configuration Register Definition

R	R	R	R	R	PC2	PC1	PC0
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

PCR.15-11 = RESERVED FOR FUTURE ENHANCEMENTS (R)

PCR.10-8 = PARTITION CONFIGURATION (PC2-0)

000 = No partitioning. Dual Work is not allowed.

001 = Plane1-3 are merged into one partition.  
(default in a bottom parameter device)

010 = Plane 0-1 and Plane 2-3 are merged into one partition respectively.

100 = Plane 0-2 are merged into one partition.  
(default in a top parameter device)

011 = Plane 2-3 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.

110 = Plane 0-1 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.

101 = Plane 1-2 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.

111 = There are four partitions in this configuration.

Each plane corresponds to each partition respectively. Dual work operation is available between any two partitions.

PCR.7-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

Notes:

After power-up or device reset, PCR 10-8 (PC2-0) is set to "001" in a bottom parameter device and "100" in a top parameter device.

See the table below for more details.

PCR.15-11 and PCR.7-0 are reserved for future use and should be masked out when checking the partition configuration register.

## Partition Configuration

PC2 PC1 PC0	PARTITIONING FOR DUAL WORK	PC2 PC1 PC0	PARTITIONING FOR DUAL WORK
0 0 0	PARTITION0 	0 1 1	PARTITION2 PARTITION1 PARTITION0 
0 0 1	PARTITION1 PARTITION0 	1 1 0	PARTITION2 PARTITION1 PARTITION0 
0 1 0	PARTITION1 PARTITION0 	1 0 1	PARTITION2 PARTITION1 PARTITION0 
1 0 0	PARTITION1 PARTITION0 	1 1 1	PARTITION3 PARTITION2 PARTITION1 PARTITION0 

## 6.4 Memory Map for Flash Memory

## Bottom Parameter

Bottom Parameter			
	BLOCK NUMBER	ADDRESS RANGE	
PLANE3 (UNIFORM PLANE)	134	32K-WORD	3F8000H - 3FFFFFFH
	133	32K-WORD	3F0000H - 3F7FFFH
	132	32K-WORD	3E8000H - 3EFFFFH
	131	32K-WORD	3E0000H - 3E7FFFH
	130	32K-WORD	3D8000H - 3DFFFFH
	129	32K-WORD	3D0000H - 3D7FFFH
	128	32K-WORD	3C8000H - 3CFFFFH
	127	32K-WORD	3C0000H - 3C7FFFH
	126	32K-WORD	3B8000H - 3BFFFFH
	125	32K-WORD	3B0000H - 3B7FFFH
	124	32K-WORD	3A8000H - 3AFFFFH
	123	32K-WORD	3A0000H - 3A7FFFH
	122	32K-WORD	398000H - 39FFFFH
	121	32K-WORD	390000H - 397FFFH
	120	32K-WORD	388000H - 38FFFFH
	119	32K-WORD	380000H - 387FFFH
	118	32K-WORD	378000H - 377FFFH
	117	32K-WORD	370000H - 377FFFH
	116	32K-WORD	368000H - 36FFFFH
	115	32K-WORD	360000H - 367FFFH
114	32K-WORD	358000H - 35FFFFH	
113	32K-WORD	350000H - 357FFFH	
112	32K-WORD	348000H - 34FFFFH	
111	32K-WORD	340000H - 347FFFH	
110	32K-WORD	338000H - 33FFFFH	
109	32K-WORD	330000H - 337FFFH	
108	32K-WORD	328000H - 32FFFFH	
107	32K-WORD	320000H - 327FFFH	
106	32K-WORD	318000H - 317FFFH	
105	32K-WORD	310000H - 317FFFH	
104	32K-WORD	308000H - 30FFFFH	
103	32K-WORD	300000H - 307FFFH	

PLANE2 (UNIFORM PLANE)	102	32K-WORD	2F8000H - 2FFFFFFH
	101	32K-WORD	2F0000H - 2F7FFFH
	100	32K-WORD	2E8000H - 2EFFFFH
	99	32K-WORD	2E0000H - 2E7FFFH
	98	32K-WORD	2D8000H - 2DFFFFH
	97	32K-WORD	2D0000H - 2D7FFFH
	96	32K-WORD	2C8000H - 2CFFFFH
	95	32K-WORD	2C0000H - 2C7FFFH
	94	32K-WORD	2B8000H - 2BFFFFH
	93	32K-WORD	2B0000H - 2B7FFFH
	92	32K-WORD	2A8000H - 2AFFFFH
	91	32K-WORD	2A0000H - 2A7FFFH
	90	32K-WORD	298000H - 29FFFFH
	89	32K-WORD	290000H - 297FFFH
	88	32K-WORD	288000H - 28FFFFH
	87	32K-WORD	280000H - 287FFFH
	86	32K-WORD	278000H - 277FFFH
	85	32K-WORD	270000H - 277FFFH
	84	32K-WORD	268000H - 26FFFFH
	83	32K-WORD	260000H - 267FFFH
82	32K-WORD	258000H - 25FFFFH	
81	32K-WORD	250000H - 257FFFH	
80	32K-WORD	248000H - 24FFFFH	
79	32K-WORD	240000H - 247FFFH	
78	32K-WORD	238000H - 23FFFFH	
77	32K-WORD	230000H - 237FFFH	
76	32K-WORD	228000H - 22FFFFH	
75	32K-WORD	220000H - 227FFFH	
74	32K-WORD	218000H - 217FFFH	
73	32K-WORD	210000H - 217FFFH	
72	32K-WORD	208000H - 20FFFFH	
71	32K-WORD	200000H - 207FFFH	

BLOCK NUMBER ADDRESS RANGE			
PLANE1 (UNIFORM PLANE)	70	32K-WORD	1F8000H - 1FFFFFFH
	69	32K-WORD	1F0000H - 1F7FFFH
	68	32K-WORD	1E8000H - 1EFFFFH
	67	32K-WORD	1E0000H - 1E7FFFH
	66	32K-WORD	1D8000H - 1DFFFFH
	65	32K-WORD	1D0000H - 1D7FFFH
	64	32K-WORD	1C8000H - 1CFFFFH
	63	32K-WORD	1C0000H - 1C7FFFH
	62	32K-WORD	1B8000H - 1BFFFFH
	61	32K-WORD	1B0000H - 1B7FFFH
	60	32K-WORD	1A8000H - 1AFFFFH
	59	32K-WORD	1A0000H - 1A7FFFH
	58	32K-WORD	198000H - 19FFFFH
	57	32K-WORD	190000H - 197FFFH
	56	32K-WORD	188000H - 18FFFFH
	55	32K-WORD	180000H - 187FFFH
	54	32K-WORD	178000H - 177FFFH
	53	32K-WORD	170000H - 177FFFH
	52	32K-WORD	168000H - 16FFFFH
	51	32K-WORD	160000H - 167FFFH
50	32K-WORD	158000H - 15FFFFH	
49	32K-WORD	150000H - 157FFFH	
48	32K-WORD	148000H - 14FFFFH	
47	32K-WORD	140000H - 147FFFH	
46	32K-WORD	138000H - 13FFFFH	
45	32K-WORD	130000H - 137FFFH	
44	32K-WORD	128000H - 12FFFFH	
43	32K-WORD	120000H - 127FFFH	
42	32K-WORD	118000H - 11FFFFH	
41	32K-WORD	110000H - 117FFFH	
40	32K-WORD	108000H - 10FFFFH	
39	32K-WORD	100000H - 107FFFH	

PLANE0 (PARAMETER PLANE)	38	32K-WORD	0F8000H - 0FFFFFFH
	37	32K-WORD	0F0000H - 0F7FFFH
	36	32K-WORD	0E8000H - 0EFFFFH
	35	32K-WORD	0E0000H - 0E7FFFH
	34	32K-WORD	0D8000H - 0DFFFFH
	33	32K-WORD	0D0000H - 0D7FFFH
	32	32K-WORD	0C8000H - 0CFFFFH
	31	32K-WORD	0C0000H - 0C7FFFH
	30	32K-WORD	0B8000H - 0BFFFFH
	29	32K-WORD	0B0000H - 0B7FFFH
	28	32K-WORD	0A8000H - 0AFFFFH
	27	32K-WORD	0A0000H - 0A7FFFH
	26	32K-WORD	098000H - 09FFFFH
	25	32K-WORD	090000H - 097FFFH
	24	32K-WORD	088000H - 08FFFFH
	23	32K-WORD	080000H - 087FFFH
	22	32K-WORD	078000H - 077FFFH
	21	32K-WORD	070000H - 077FFFH
	20	32K-WORD	068000H - 06FFFFH
	19	32K-WORD	060000H - 067FFFH
18	32K-WORD	058000H - 05FFFFH	
17	32K-WORD	050000H - 057FFFH	
16	32K-WORD	048000H - 04FFFFH	
15	32K-WORD	040000H - 047FFFH	
14	32K-WORD	038000H - 03FFFFH	
13	32K-WORD	030000H - 037FFFH	
12	32K-WORD	028000H - 02FFFFH	
11	32K-WORD	020000H - 027FFFH	
10	32K-WORD	018000H - 01FFFFH	
9	32K-WORD	010000H - 017FFFH	
8	32K-WORD	008000H - 00FFFFH	
7	4K-WORD	007000H - 007FFFH	
6	4K-WORD	006000H - 006FFFH	
5	4K-WORD	005000H - 005FFFH	
4	4K-WORD	004000H - 004FFFH	
3	4K-WORD	003000H - 003FFFH	
2	4K-WORD	002000H - 002FFFH	
1	4K-WORD	001000H - 001FFFH	
0	4K-WORD	000000H - 000FFFH	

## 6.5 DC Electrical Characteristics for Flash Memory

## DC Electrical Characteristics

(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

Symbol	Parameter		Notes	Min.	Typ.	Max.	Unit	Test Conditions
C <sub>IN</sub>	Input Capacitance		5			7	pF	V <sub>IN</sub> = 0V, f = 1MHz, T <sub>A</sub> = 25°C
C <sub>IO</sub>	I/O Capacitance		5			10	pF	V <sub>I/O</sub> = 0V, f = 1MHz, T <sub>A</sub> = 25°C
I <sub>LI</sub>	Input Leakage Current					±1	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>LO</sub>	Output Leakage Current					±1	μA	V <sub>OUT</sub> = V <sub>CC</sub> or GND
I <sub>CCS</sub>	V <sub>CC</sub> Standby Current		1, 8		4	20	μA	V <sub>CC</sub> = V <sub>CC</sub> Max., F <sub>1-CE</sub> = RST = V <sub>CC</sub> ±0.2V, WP = V <sub>CC</sub> or GND
I <sub>CCAS</sub>	V <sub>CC</sub> Automatic Power Savings Current		1, 4		4	20	μA	V <sub>CC</sub> = V <sub>CC</sub> Max., F <sub>1-CE</sub> = GND ±0.2V, WP = V <sub>CC</sub> or GND
I <sub>CCD</sub>	V <sub>CC</sub> Reset Power-Down Current		1		4	20	μA	RST = GND ±0.2V I <sub>OUT</sub> (RY/BY) = 0mA
I <sub>CCR</sub>	Average V <sub>CC</sub> Read Current Normal Mode		1, 7		15	25	mA	V <sub>CC</sub> = V <sub>CC</sub> Max., F <sub>1-CE</sub> = V <sub>IL</sub> , F- <u>OE</u> = V <sub>IH</sub> , f = 5MHz I <sub>OUT</sub> = 0mA
	Average V <sub>CC</sub> Read Current Page Mode	8 Word Read	1, 7		5	10	mA	
I <sub>CCW</sub>	V <sub>CC</sub> (Page Buffer) Program Current		1, 5, 7		20	60	mA	V <sub>PP</sub> = V <sub>PPH</sub>
I <sub>CCE</sub>	V <sub>CC</sub> Block Erase, Full Chip Erase Current		1, 5, 7		10	30	mA	V <sub>PP</sub> = V <sub>PPH</sub>
I <sub>CCWS</sub> I <sub>CCES</sub>	V <sub>CC</sub> (Page Buffer) Program or Block Erase Suspend Current		1, 2, 7		10	200	μA	F <sub>1-CE</sub> = V <sub>IH</sub>
I <sub>PPS</sub> I <sub>PPR</sub>	V <sub>PP</sub> Standby or Read Current		1, 6, 7		2	5	μA	V <sub>PP</sub> ≤ V <sub>CC</sub>
I <sub>PPW</sub>	V <sub>PP</sub> (Page Buffer) Program Current		1,5,6,7		2	5	μA	V <sub>PP</sub> = V <sub>PPH</sub>
I <sub>PPE</sub>	V <sub>PP</sub> Block Erase, Full Chip Erase Current		1,5,6,7		2	5	μA	V <sub>PP</sub> = V <sub>PPH</sub>
I <sub>PPWS</sub>	V <sub>PP</sub> (Page Buffer) Program Suspend Current		1, 6, 7		2	5	μA	V <sub>PP</sub> = V <sub>PPH</sub>
I <sub>PPES</sub>	V <sub>PP</sub> Block Erase Suspend Current		1, 6, 7		2	5	μA	V <sub>PP</sub> = V <sub>PPH</sub>

## DC Electrical Characteristics (Continue)

 $(T_A = -25^{\circ}\text{C to } +85^{\circ}\text{C}, V_{CC} = 2.7\text{V to } 3.1\text{V})$ 

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
$V_{IL}$	Input Low Voltage	5	-0.3		0.4	V	
$V_{IH}$	Input High Voltage	5	$V_{CC}$ -0.4		$V_{CC}$ +0.3	V	
$V_{OL}$	Output Low Voltage	5, 8			$0.2V_{CC}$	V	$I_{OL} = 0.5\text{mA}$
$V_{OH}$	Output High Voltage	5	2.2			V	$I_{OH} = -0.5\text{mA}$
$V_{PPLK}$	$V_{PP}$ Lockout during Normal Operations	3,5,6			0.4	V	
$V_{PPH}$	$V_{PP}$ during Block Erase, Full Chip Erase, (Page Buffer) Program Operations	6	1.65	3	3.1	V	
$V_{LKO}$	$V_{CC}$ Lockout Voltage		1.5			V	

## Notes:

- All currents are in RMS unless otherwise noted. Typical values are the reference values at  $V_{CC} = 3.0\text{V}$  and  $T_A = +25^{\circ}\text{C}$  unless  $V_{CC}$  is specified.
- $I_{CCWS}$  and  $I_{CCES}$  are specified with the device de-selected. If read or (page buffer) program is executed while in block erase suspend mode, the device's current draw is the sum of  $I_{CCES}$  and  $I_{CCR}$  or  $I_{CCW}$ . If read is executed while in (page buffer) program suspend mode, the device's current draw is the sum of  $I_{CCWS}$  and  $I_{CCR}$ .
- Block erase, full chip erase, (page buffer) program are inhibited when  $V_{PP} \leq V_{PPLK}$ , and not guaranteed outside the specified voltage.
- The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings ( $t_{AVQV}$ ) provide new data when addresses are changed.
- Sampled, not 100% tested.
- $V_{PP}$  is not used for power supply pin. With  $V_{PP} \leq V_{PPLK}$ , block erase, full chip erase, (page buffer) program cannot be executed and should not be attempted.
- The operating current in dual work is the sum of the operating current (read, erase, program) in each plane.
- Includes  $\overline{\text{RY}}/\overline{\text{BY}}$

## 6.6 AC Electrical Characteristics for Flash Memory

### 6.6.1 AC Test Conditions

Input Pulse Level	0 V to 2.7 V
Input Rise and Fall Time	5 ns
Input and Output Timing Ref. level	1.35 V
Output Load	1TTL +C <sub>L</sub> (50pF)

### 6.6.2 Read Cycle

(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t <sub>AVAV</sub>	Read Cycle Time		65		ns
t <sub>AVQV</sub>	Address to Output Delay			65	ns
t <sub>ELQV</sub>	F <sub>1</sub> - $\overline{\text{CE}}$ to Output Delay	2		65	ns
t <sub>APA</sub>	Page Address Access Time			25	ns
t <sub>GLQV</sub>	F- $\overline{\text{OE}}$ to Output Delay	2		20	ns
t <sub>PHQV</sub>	$\overline{\text{RST}}$ High to Output Delay			150	ns
t <sub>EHQZ</sub> , t <sub>GHQZ</sub>	F <sub>1</sub> - $\overline{\text{CE}}$ or F- $\overline{\text{OE}}$ to Output in High-Z, Whichever Occurs First	1		20	ns
t <sub>ELQX</sub>	F <sub>1</sub> - $\overline{\text{CE}}$ to Output in Low-Z	1	0		ns
t <sub>GLQX</sub>	F- $\overline{\text{OE}}$ to Output in Low-Z	1	0		ns
t <sub>OH</sub>	Output Hold from First Occurring Address, F <sub>1</sub> - $\overline{\text{CE}}$ or F- $\overline{\text{OE}}$ Change	1	0		ns
t <sub>AVEL</sub> , t <sub>AVGL</sub>	Address Setup to F <sub>1</sub> - $\overline{\text{CE}}$ and F- $\overline{\text{OE}}$ Going Low for Reading Status Register	3,5	10		ns
t <sub>ELAX</sub> , t <sub>GLAX</sub>	Address Hold from F <sub>1</sub> - $\overline{\text{CE}}$ and F- $\overline{\text{OE}}$ Going Low for Reading Status Register	4,5	30		ns
t <sub>EHGL</sub> , t <sub>GHGL</sub>	F <sub>1</sub> - $\overline{\text{CE}}$ and F- $\overline{\text{OE}}$ Pulse Width High for Reading Status Register	5	15		ns

#### Notes:

1. Sampled, not 100% tested.
2. F- $\overline{\text{OE}}$  may be delayed up to t<sub>ELQV</sub> - t<sub>GLQV</sub> after the falling edge of F<sub>1</sub>- $\overline{\text{CE}}$  without impact to t<sub>ELQV</sub>.
3. Address setup time (t<sub>AVEL</sub>, t<sub>AVGL</sub>) is defined from the falling edge of F<sub>1</sub>- $\overline{\text{CE}}$  or F- $\overline{\text{OE}}$  (whichever goes low last).
4. Address hold time (t<sub>ELAX</sub>, t<sub>GLAX</sub>) is defined from the falling edge of F<sub>1</sub>- $\overline{\text{CE}}$  or F- $\overline{\text{OE}}$  (whichever goes low last).
5. Specifications t<sub>AVEL</sub>, t<sub>AVGL</sub>, t<sub>ELAX</sub>, t<sub>GLAX</sub> and t<sub>EHGL</sub>, t<sub>GHGL</sub> for read operations apply to only status register read operations.

6.6.3 Write Cycle (F- $\overline{WE}$  / F<sub>1</sub>- $\overline{CE}$  Controlled)<sup>(1,2)</sup>(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t <sub>AVAV</sub>	Write Cycle Time		65		ns
t <sub>PHWL</sub> (t <sub>PHL</sub> )	$\overline{RST}$ High Recovery to F- $\overline{WE}$ (F <sub>1</sub> - $\overline{CE}$ ) Going Low	3	150		ns
t <sub>ELWL</sub> (t <sub>WLEL</sub> )	F <sub>1</sub> - $\overline{CE}$ (F- $\overline{WE}$ ) Setup to F- $\overline{WE}$ (F <sub>1</sub> - $\overline{CE}$ ) Going Low		0		ns
t <sub>WLWH</sub> (t <sub>ELEH</sub> )	F- $\overline{WE}$ (F <sub>1</sub> - $\overline{CE}$ ) Pulse Width	4	50		ns
t <sub>DVWH</sub> (t <sub>DVEH</sub> )	Data Setup to F- $\overline{WE}$ (F <sub>1</sub> - $\overline{CE}$ ) Going High	8	40		ns
t <sub>AVWH</sub> (t <sub>AVEH</sub> )	Address Setup to F- $\overline{WE}$ (F <sub>1</sub> - $\overline{CE}$ ) Going High	8	50		ns
t <sub>WHEH</sub> (t <sub>EHWH</sub> )	F <sub>1</sub> - $\overline{CE}$ (F- $\overline{WE}$ ) Hold from F- $\overline{WE}$ (F <sub>1</sub> - $\overline{CE}$ ) High		0		ns
t <sub>WHDX</sub> (t <sub>EHDX</sub> )	Data Hold from F- $\overline{WE}$ (F <sub>1</sub> - $\overline{CE}$ ) High		0		ns
t <sub>WHAX</sub> (t <sub>EHAH</sub> )	Address Hold from F- $\overline{WE}$ (F <sub>1</sub> - $\overline{CE}$ ) High		0		ns
t <sub>WHWL</sub> (t <sub>EHEL</sub> )	F- $\overline{WE}$ (F <sub>1</sub> - $\overline{CE}$ ) Pulse Width High	5	15		ns
t <sub>SHWH</sub> (t <sub>SHEH</sub> )	$\overline{WP}$ High Setup to F- $\overline{WE}$ (F <sub>1</sub> - $\overline{CE}$ ) Going High	3	0		ns
t <sub>VVWH</sub> (t <sub>VVEH</sub> )	V <sub>PP</sub> Setup to F- $\overline{WE}$ (F <sub>1</sub> - $\overline{CE}$ ) Going High	3	200		ns
t <sub>WHGL</sub> (t <sub>EHGL</sub> )	Write Recovery before Read		30		ns
t <sub>QVSL</sub>	$\overline{WP}$ High Hold from Valid SRD, RY/ $\overline{BY}$ High-Z	3, 6	0		ns
t <sub>QVVL</sub>	V <sub>PP</sub> Hold from Valid SRD, RY/ $\overline{BY}$ High-Z	3, 6	0		ns
t <sub>WHR0</sub> (t <sub>EHR0</sub> )	F- $\overline{WE}$ (F <sub>1</sub> - $\overline{CE}$ ) High to SR.7 Going "0"	3, 7		t <sub>AVQV</sub> +50	ns
t <sub>WHRL</sub> (t <sub>EHRL</sub> )	F- $\overline{WE}$ (F <sub>1</sub> - $\overline{CE}$ ) High to RY/ $\overline{BY}$ Going Low	3		100	ns

## Notes:

- The timing characteristics for reading the status register during block erase, full chip erase, (page buffer) program operations are the same as during read-only operations. See the AC Characteristics for read cycle.
- A write operation can be initiated and terminated with either F<sub>1</sub>- $\overline{CE}$  or F- $\overline{WE}$ .
- Sampled, not 100% tested.
- Write pulse width (t<sub>WP</sub>) is defined from the falling edge of F<sub>1</sub>- $\overline{CE}$  or F- $\overline{WE}$  (whichever goes low last) to the rising edge of F<sub>1</sub>- $\overline{CE}$  or F- $\overline{WE}$  (whichever goes high first). Hence, t<sub>WP</sub>=t<sub>WLWH</sub>=t<sub>ELEH</sub>=t<sub>WLEH</sub>=t<sub>ELWH</sub>.
- Write pulse width high (t<sub>WPH</sub>) is defined from the rising edge of F<sub>1</sub>- $\overline{CE}$  or F- $\overline{WE}$  (whichever goes high first) to the falling edge of F<sub>1</sub>- $\overline{CE}$  or F- $\overline{WE}$  (whichever goes low last). Hence, t<sub>WPH</sub>=t<sub>WHWL</sub>=t<sub>EHEL</sub>=t<sub>WHEL</sub>=t<sub>EHWL</sub>.
- V<sub>PP</sub> should be held at V<sub>PP</sub>=V<sub>PPH</sub> until determination of block erase, full chip erase, (page buffer) program success (SR.1/3/4/5=0).
- t<sub>WHR0</sub> (t<sub>EHR0</sub>) after the Read Query or Read Identifier Codes command=t<sub>AVQV</sub>+100ns.
- See 6.2.1 Command Definitions for valid address and data for block erase, full chip erase, (page buffer) program or lock bit configuration.



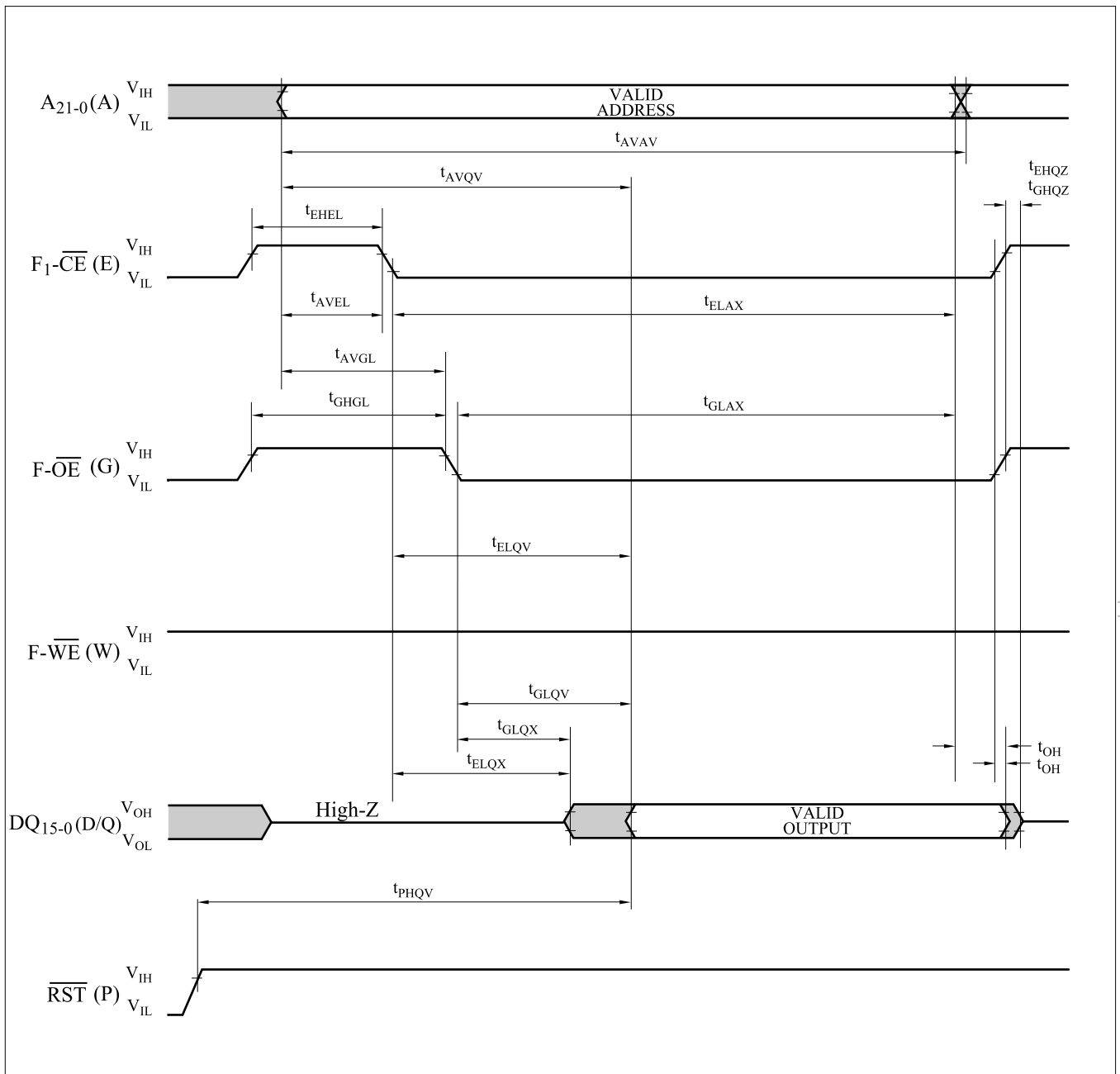
6.6.4 Block Erase, Full Chip Erase, (Page Buffer) Program Performance <sup>(3)</sup>(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

Symbol	Parameter	Notes	Page Buffer Command is Used or not Used	V <sub>PP</sub> =V <sub>PPH</sub>			Unit
				Min.	Typ. <sup>(1)</sup>	Max. <sup>(2)</sup>	
t <sub>WPB</sub>	4K-Word Parameter Block Program Time	2	Not Used		0.05	0.3	s
		2	Used		0.03	0.12	s
t <sub>WMB</sub>	32K-Word Main Block Program Time	2	Not Used		0.38	2.4	s
		2	Used		0.24	1	s
t <sub>WHQV1</sub> / t <sub>EHQV1</sub>	Word Program Time	2	Not Used		11	200	μs
		2	Used		7	100	μs
t <sub>WHQV2</sub> / t <sub>EHQV2</sub>	4K-Word Parameter Block Erase Time	2	-		0.3	4	s
t <sub>WHQV3</sub> / t <sub>EHQV3</sub>	32K-Word Main Block Erase Time	2	-		0.6	5	s
	Full Chip Erase Time	2			80	700	s
t <sub>WHRH1</sub> / t <sub>EHRH1</sub>	(Page Buffer) Program Suspend Latency Time to Read	4	-		5	10	μs
t <sub>WHRH2</sub> / t <sub>EHRH2</sub>	Block Erase Suspend Latency Time to Read	4	-		5	20	μs
t <sub>ERES</sub>	Latency Time from Block Erase Resume Command to Block Erase Suspend Command	5	-	500			μs

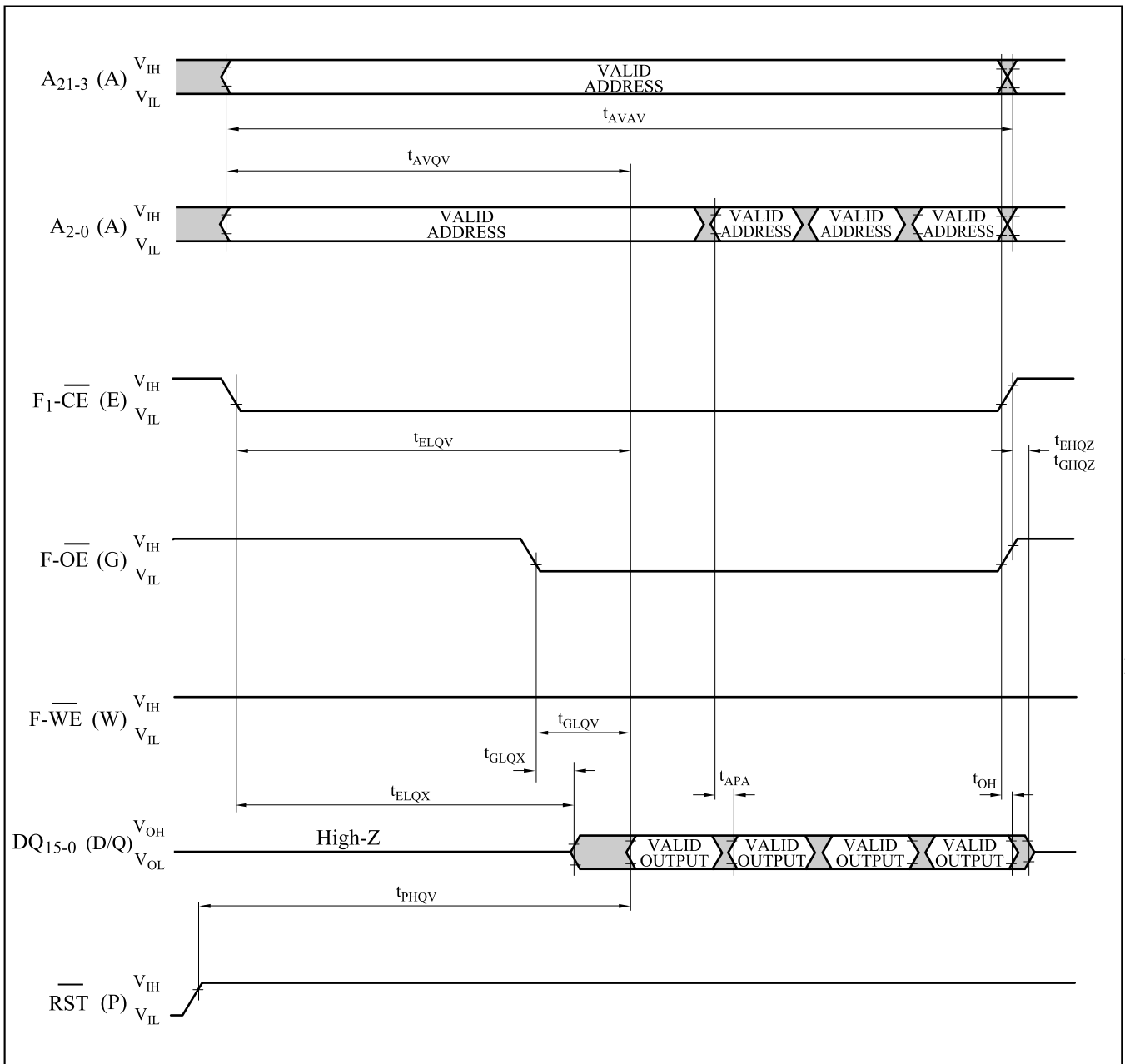
## Notes:

1. Typical values measured at V<sub>CC</sub>=3.0V, V<sub>PP</sub>=3.0V, and T<sub>A</sub>=+25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.
4. A latency time is required from writing suspend command (F<sub>1</sub> $\overline{WE}$  or F<sub>1</sub> $\overline{CE}$  going high) until SR.7 going "1" or RY/ $\overline{BY}$  going High-Z.
5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t<sub>ERES</sub> and its sequence is repeated, the block erase operation may not be finished.

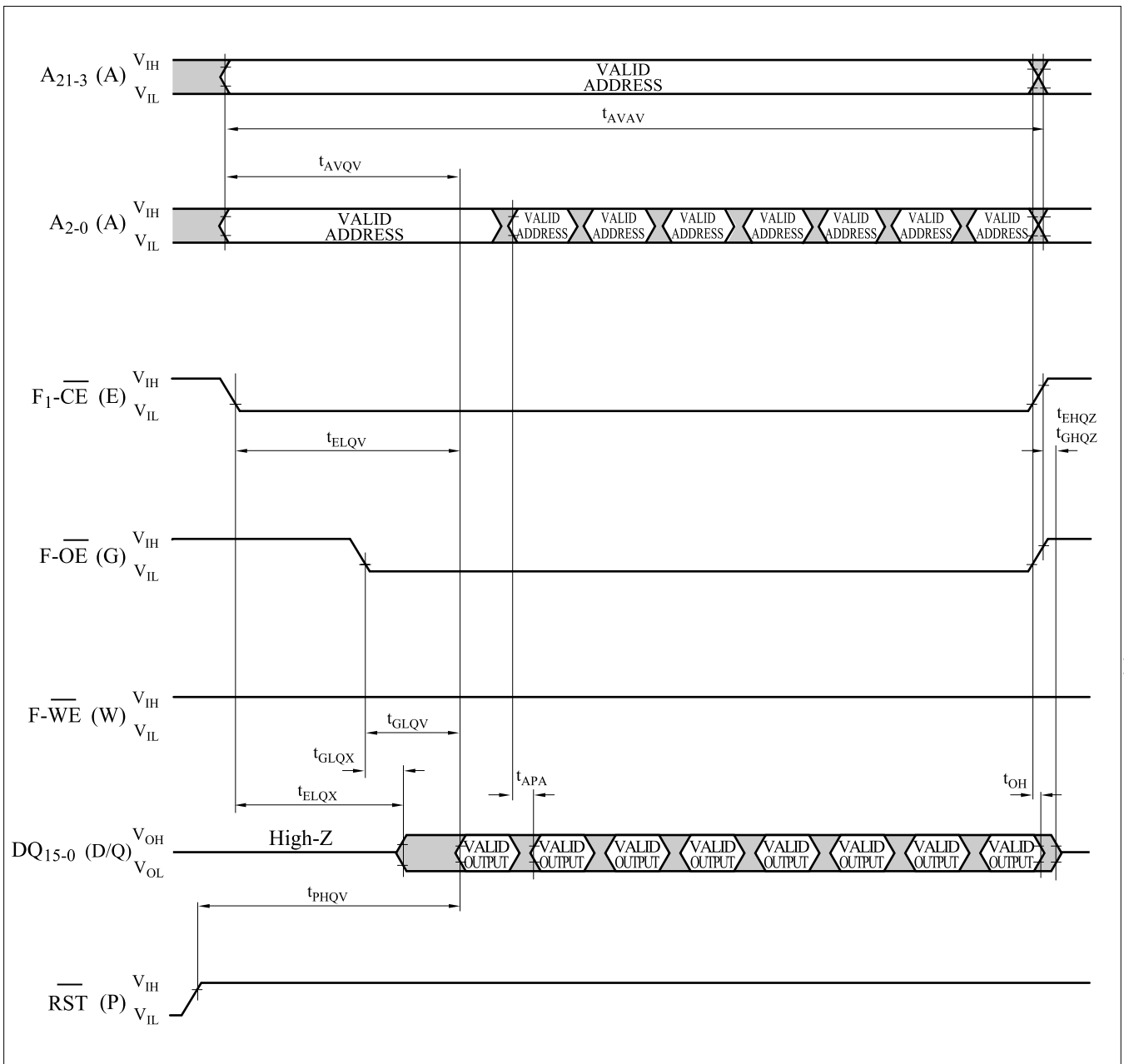
## 6.6.5 Flash Memory AC Characteristics Timing Chart

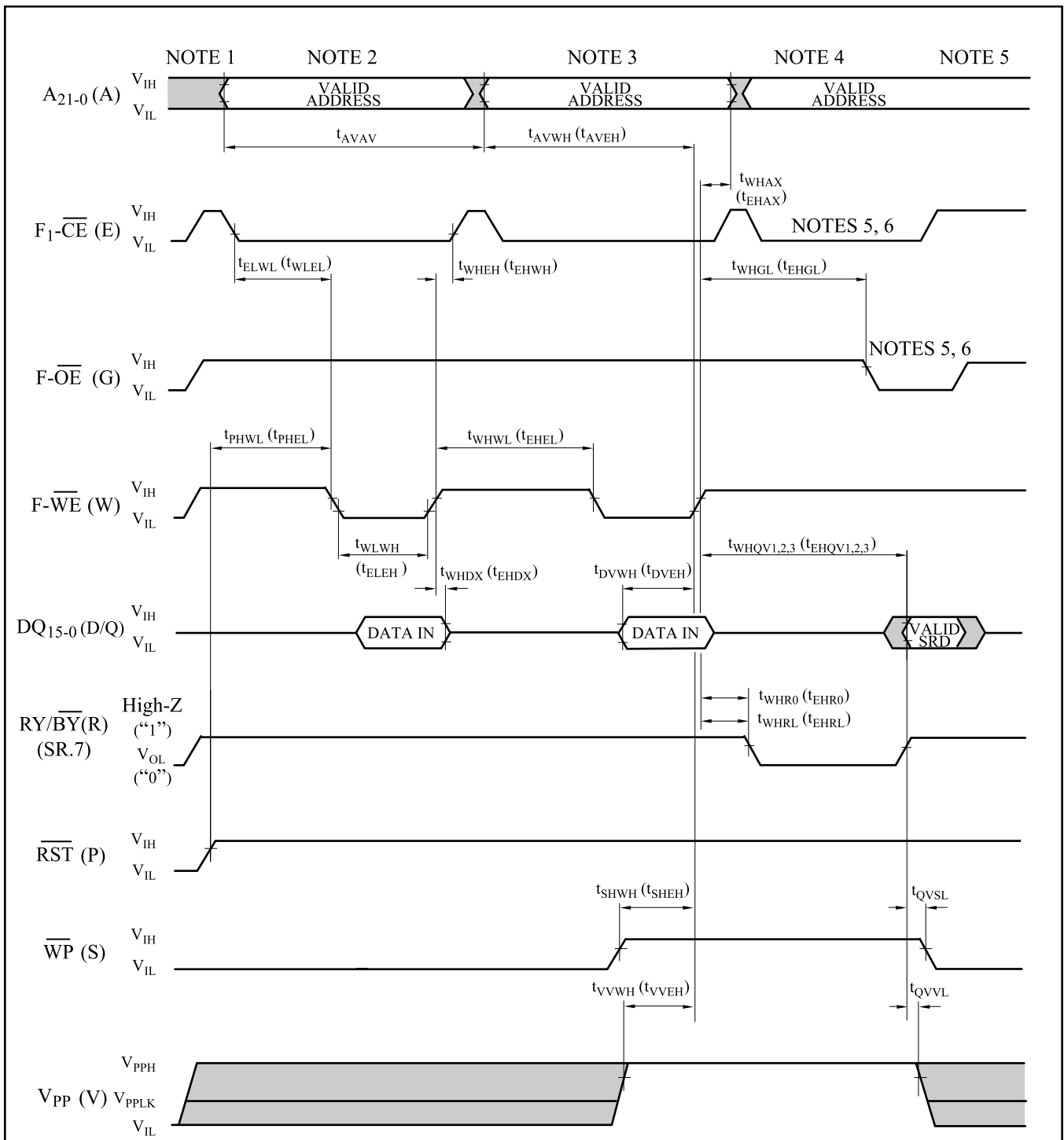
AC Waveform for Single Asynchronous Read Operations from Status Register, Identifier Codes or Query Code

AC Waveform for Asynchronous 4-Word Page Mode Read Operations from Main Blocks or Parameter Blocks



### AC Waveform for Asynchronous 8-Word Page Mode Read Operations from Main Blocks or Parameter Blocks



AC Waveform for Write Operations (F- $\overline{\text{WE}}$  / F1- $\overline{\text{CE}}$  Controlled)

DataSheet4U.com

DataSheet4U.com

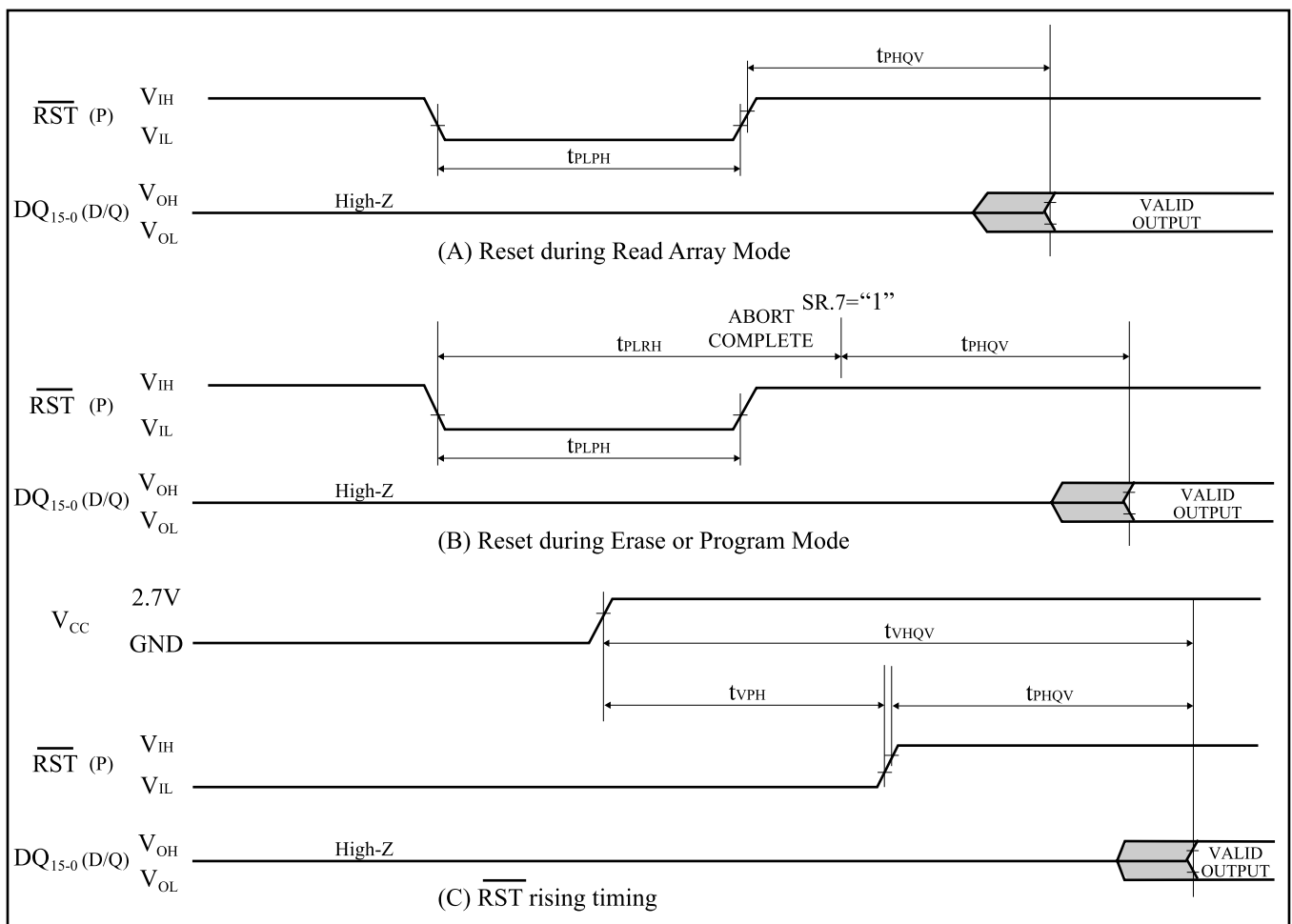
## 6.6.6 Reset Operations

(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t <sub>PLPH</sub>	$\overline{\text{RST}}$ Low to Reset during Read ( $\overline{\text{RST}}$ should be low during power-up.)	1, 2, 3	100		ns
t <sub>PLRH</sub>	$\overline{\text{RST}}$ Low to Reset during Erase or Program	1, 3, 4		22	μs
t <sub>VPH</sub>	V <sub>CC</sub> = 2.7V to $\overline{\text{RST}}$ High	1, 3, 5	100		ns
t <sub>VHQV</sub>	V <sub>CC</sub> = 2.7V to Output Delay	3		1	ms

## Notes:

1. A reset time, t<sub>PHQV</sub>, is required from the later of SR.7 (RY/ $\overline{\text{BY}}$ ) going "1" (High-Z) or  $\overline{\text{RST}}$  going high until outputs are valid. See the AC Characteristics - read cycle for t<sub>PHQV</sub>.
2. t<sub>PLPH</sub> is <100ns the device may still reset but this is not guaranteed.
3. Sampled, not 100% tested.
4. If  $\overline{\text{RST}}$  asserted while a block erase, full chip erase or (page buffer) program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding  $\overline{\text{RST}}$  low minimum 100ns is required after V<sub>CC</sub> has been in predefined range and also has been in stable there.

AC Waveform for Reset Operation

## 7. Flash Memory 2

## 7.1 Truth Table

7.1.1 Bus Operation <sup>(1)</sup>

Flash	Notes	F <sub>2</sub> - $\overline{\text{CE}}$	$\overline{\text{RST}}$	F- $\overline{\text{OE}}$	F- $\overline{\text{WE}}$	DQ <sub>0</sub> to DQ <sub>15</sub>
Read	3,5	L	H	L	H	(7)
Output Disable	5			H		High - Z
Write	2,3,4,5			L	D <sub>IN</sub>	
Standby	5	H	H	X	X	High - Z
Reset Power Down	5,6	X	L			

## Notes:

1. L = V<sub>IL</sub>, H = V<sub>IH</sub>, X = H or L, High-Z = High impedance. Refer to the DC Characteristics.
2. Command writes involving block erase, full chip erase, (page buffer) program are reliably executed when V<sub>PP</sub> = V<sub>PPH</sub> and V<sub>CC</sub> = 2.7V to 3.1V.  
Block erase, full chip erase, (page buffer) program with V<sub>PP</sub> < V<sub>PPH</sub> (Min.) produce spurious results and should not be attempted.
3. Never hold F- $\overline{\text{OE}}$  low and F- $\overline{\text{WE}}$  low at the same timing.
4. Refer to Section 7.2 Command Definitions for Flash Memory valid D<sub>IN</sub> during a write operation.
5.  $\overline{\text{WP}}$  set to V<sub>IL</sub> or V<sub>IH</sub>.
6. Electricity consumption of Flash Memory is lowest when  $\overline{\text{RST}}$  = GND ±0.2V.

## 7. Flash Read Mode

Mode	Address	DQ <sub>0</sub> to DQ <sub>15</sub>
Read Array	X	D <sub>OUT</sub>
Read Identifier Codes	See 7.2.2	See 7.2.2
Read Query	Refer to the Appendix	Refer to the Appendix

7.1.2 Simultaneous Operation Modes Allowed with Four Planes <sup>(1,2)</sup>

IF ONE PARTITION IS:	THEN THE MODES ALLOWED IN THE OTHER PARTITION IS:									
	Read Array	Read ID	Read Status	Read Query	Word Program	Page Buffer Program	Block Erase	Full Chip Erase	Program Suspend	Block Erase Suspend
Read Array	X	X	X	X	X	X	X		X	X
Read ID	X	X	X	X	X	X	X		X	X
Read Status	X	X	X	X	X	X	X	X	X	X
Read Query	X	X	X	X	X	X	X		X	X
Word Program	X	X	X	X						X
Page Buffer Program	X	X	X	X						X
Block Erase	X	X	X	X						
Full Chip Erase			X							
Program Suspend	X	X	X	X						X
Block Erase Suspend	X	X	X	X	X	X			X	

## Notes:

1. "X" denotes the operation available.
2. Configurative Partition Dual Work Restrictions:  
 Status register reflects partition state, not WSM (Write State Machine) state - this allows a status register for each partition.  
 Only one partition can be erased or programmed at a time - no command queuing.  
 Commands must be written to an address within the block targeted by that command.



7.2 Command Definitions for Flash Memory <sup>(11)</sup>

## 7.2.1 Command Definitions

Command	Bus Cycles Req'd	Notes	First Bus Cycle			Second Bus Cycle		
			Oper <sup>(1)</sup>	Address <sup>(2)</sup>	Data	Oper <sup>(1)</sup>	Address <sup>(2)</sup>	Data <sup>(3)</sup>
Read Array	1		Write	PA	FFH			
Read Identifier Codes	≥ 2	4	Write	PA	90H	Read	IA	ID
Read Query	≥ 2	4	Write	PA	98H	Read	QA	QD
Read Status Register	2		Write	PA	70H	Read	PA	SRD
Clear Status Register	1		Write	PA	50H			
Block Erase	2	5	Write	BA	20H	Write	BA	D0H
Full Chip Erase	2	5, 9	Write	X	30H	Write	X	D0H
Program	2	5, 6	Write	WA	40H or 10H	Write	WA	WD
Page Buffer Program	≥ 4	5, 7	Write	WA	E8H	Write	WA	N-1
Block Erase and (Page Buffer) Program Suspend	1	8, 9	Write	PA	B0H			
Block Erase and (Page Buffer) Program Resume	1	8, 9	Write	PA	D0H			
Set Block Lock Bit	2		Write	BA	60H	Write	BA	01H
Clear Block Lock Bit	2	10	Write	BA	60H	Write	BA	D0H
Set Block Lock-down Bit	2		Write	BA	60H	Write	BA	2FH
Set Partition Configuration Register	2		Write	PCRC	60H	Write	PCRC	04H

## Notes:

- Bus operations are defined in 7.1.1 Bus Operation.
- All addresses which are written at the first bus cycle should be the same as the addresses which are written at the second bus cycle.  
X=Any valid address within the device.  
PA=Address within the selected partition.  
IA=Identifier codes address (See 7.2.2 Identifier Codes for Read Operation).  
QA=Query codes address. Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.  
BA=Address within the block being erased, set/cleared block lock bit or set block lock-down bit.  
WA=Address of memory location for the Program command or the first address for the Page Buffer Program command.  
PCRC=Partition configuration register code presented on the address A<sub>0</sub>-A<sub>15</sub>.
- ID=Data read from identifier codes (See 7.2.2 Identifier Codes for Read Operation).  
QD=Data read from query database. Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.  
SRD=Data read from status register. See 7.3 Register Definition for a description of the status register bits.  
WD=Data to be programmed at location WA. Data is latched on the rising edge of F- $\overline{WE}$  or F<sub>2</sub>- $\overline{CE}$  (whichever goes high first) during command write cycles.  
N-1=N is the number of the words to be loaded into a page buffer.
- Following the Read Identifier Codes command, read operations access manufacturer code, device code, block lock configuration code, partition configuration register code (See 7.2.2 Identifier Codes for Read Operation).  
The Read Query command is available for reading CFI (Common Flash Interface) information.
- Block erase, full chip erase or (page buffer) program cannot be executed when the selected block is locked. Unlocked block can be erased or programmed when  $\overline{RST}$  is V<sub>IH</sub>.
- Either 40H or 10H are recognized by the CUI (Command User Interface) as the program setup.
- Following the third bus cycle, input the program sequential address and write data of "N" times. Finally, input the any valid address within the target block to be programmed and the confirm command (D0H). Refer to the LH28F320BF, LH28F640BF, LH28F128BF series Appendix for details.

8. If the program operation in one partition is suspended and the erase operation in other partition is also suspended, the suspended program operation should be resumed first, and then the suspended erase operation should be resumed next.
9. Full chip erase operation can not be suspended.
10. Following the Clear Block Lock Bit command, block which is not locked-down is unlocked when  $\overline{WP}$  is  $V_{IL}$ .  
When  $\overline{WP}$  is  $V_{IH}$ , lock-down bit is disabled and the selected block is unlocked regardless of lock-down configuration.
11. Commands other than those shown above are reserved by SHARP for future device implementations and should not be used.

## 7.2.2 Identifier Codes for Read Operation

	Code	Address [A <sub>15</sub> -A <sub>0</sub> ]	Data [DQ <sub>15</sub> -DQ <sub>0</sub> ]	Notes
Manufacturer Code	Manufacturer Code	0000H	00B0H	4
Device Code	64M (x16) Bottom Parameter Device Code	0001H	00B1H	1, 4
Block Lock Configuration Code	Block is Unlocked	Block Address + 2	DQ <sub>0</sub> = 0	2
	Block is Locked		DQ <sub>0</sub> = 1	2
	Block is not Locked-Down		DQ <sub>1</sub> = 0	2
	Block is Locked-Down		DQ <sub>1</sub> = 1	2
Device Configuration Code	Partition Configuration Register	0006H	PCRC	3, 4

## Notes:

1. Bottom parameter device has its parameter blocks in the plane 0 (The lowest address).
2. Block Address = The beginning location of a block address within the partition to which the Read Identifier Codes command (90H) has been written.  
DQ<sub>15</sub>-DQ<sub>2</sub> is reserved for future implementation.
3. PCRC = Partition Configuration Register Code.
4. The address A<sub>21</sub>-A<sub>16</sub> are shown in below table for reading the manufacturer, device, device configuration code.  
The address to read the identifier codes is dependent on the partition which is selected when writing the Read Identifier Codes command (90H).  
See Section 7.3 Partition Configuration Register Definition (P.38) for the partition configuration register.

## Identifier Codes for Read Operation on Partition Configuration (64M (x16)-bit device)

Partition Configuration Register			Address (64M (x16)-bit device)
PCR.10	PCR.9	PCR.8	[A <sub>21</sub> -A <sub>16</sub> ]
0	0	0	00H
0	0	1	00H or 10H
0	1	0	00H or 20H
1	0	0	00H or 30H
0	1	1	00H or 10H or 20H
1	1	0	00H or 20H or 30H
1	0	1	00H or 10H or 30H
1	1	1	00H or 10H or 20H or 30H

## 7.2.3 Functions of Block Lock and Block Lock-Down

Current State					Erase/Program Allowed <sup>(2)</sup>
State	$\overline{WP}$	DQ <sub>1</sub> <sup>(1)</sup>	DQ <sub>0</sub> <sup>(1)</sup>	State Name	
[000]	0	0	0	Unlocked	Yes
[001] <sup>(3)</sup>	0	0	1	Locked	No
[011]	0	1	1	Locked-down	No
[100]	1	0	0	Unlocked	Yes
[101] <sup>(3)</sup>	1	0	1	Locked	No
[110] <sup>(4)</sup>	1	1	0	Lock-down Disable	Yes
[111]	1	1	1	Lock-down Disable	No

Notes:

- DQ<sub>0</sub> = 1: a block is locked; DQ<sub>0</sub> = 0: a block is unlocked.  
DQ<sub>1</sub> = 1: a block is locked-down; DQ<sub>1</sub> = 0: a block is not locked-down.
- Erase and program are general terms, respectively, to express: block erase, full chip erase and (page buffer) program operations.
- At power-up or device reset, all blocks default to locked state and are not locked-down, that is, [001] ( $\overline{WP} = 0$ ) or [101] ( $\overline{WP} = 1$ ), regardless of the states before power-off or reset operation.
- When  $\overline{WP}$  is driven to V<sub>IL</sub> in [110] state, the state changes to [011] and the blocks are automatically locked.

7.2.4 Block Locking State Transitions upon Command Write <sup>(4)</sup>

Current State				Result after Lock Command Written (Next State)		
State	$\overline{WP}$	DQ <sub>1</sub>	DQ <sub>0</sub>	Set Lock <sup>(1)</sup>	Clear Lock <sup>(1)</sup>	Set Lock-down <sup>(1)</sup>
[000]	0	0	0	[001]	No Change	[011] <sup>(2)</sup>
[001]	0	0	1	No Change <sup>(3)</sup>	[000]	[011]
[011]	0	1	1	No Change	No Change	No Change
[100]	1	0	0	[101]	No Change	[111] <sup>(2)</sup>
[101]	1	0	1	No Change	[100]	[111]
[110]	1	1	0	[111]	No Change	[111] <sup>(2)</sup>
[111]	1	1	1	No Change	[110]	No Change

Notes:

- “Set Lock” means Set Block Lock Bit command, “Clear Lock” means Clear Block Lock Bit command and “Set Lock-down” means Set Block Lock-Down Bit command.
- When the Set Block Lock-Down Bit command is written to the unlocked block (DQ<sub>0</sub> = 0), the corresponding block is locked-down and automatically locked at the same time.
- “No Change” means that the state remains unchanged after the command written.
- In this state transitions table, assumes that  $\overline{WP}$  is not changed and fixed V<sub>IL</sub> or V<sub>IH</sub>.

7.2.5 Block Locking State Transitions upon  $\overline{WP}$  Transition <sup>(4)</sup>

Previous State	Current State				Result after $\overline{WP}$ Transition (Next State)	
	State	$\overline{WP}$	DQ <sub>1</sub>	DQ <sub>0</sub>	$\overline{WP} = 0 \rightarrow 1$ <sup>(1)</sup>	$\overline{WP} = 1 \rightarrow 0$ <sup>(1)</sup>
-	[000]	0	0	0	[100]	-
-	[001]	0	0	1	[101]	-
[110] <sup>(2)</sup>	[011]	0	1	1	[110]	-
Other than [110] <sup>(2)</sup>					[111]	-
-	[100]	1	0	0	-	[000]
-	[101]	1	0	1	-	[001]
-	[110]	1	1	0	-	[011] <sup>(3)</sup>
-	[111]	1	1	1	-	[011]

Notes:

1. " $\overline{WP} = 0 \rightarrow 1$ " means that  $\overline{WP}$  is driven to  $V_{IH}$  and " $\overline{WP} = 1 \rightarrow 0$ " means that  $\overline{WP}$  is driven to  $V_{IL}$ .
2. State transition from the current state [011] to the next state depends on the previous state.
3. When  $\overline{WP}$  is driven to  $V_{IL}$  in [110] state, the state changes to [011] and the blocks are automatically locked.
4. In this state transitions table, assumes that lock configuration commands are not written in previous, current and next state.

## 7.3 Register Definition

## Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
WSMS	BESS	BEFCES	PBPS	VPPS	PBPSS	DPS	R
7	6	5	4	3	2	1	0

SR.15 - SR.8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

SR.7 = WRITE STATE MACHINE STATUS (WSMS)

- 1 = Ready
- 0 = Busy

SR.6 = BLOCK ERASE SUSPEND STATUS (BESS)

- 1 = Block Erase Suspended
- 0 = Block Erase in Progress/Completed

SR.5 = BLOCK ERASE AND FULL CHIP ERASE STATUS (BEFCES)

- 1 = Error in Block Erase or Full Chip Erase
- 0 = Successful Block Erase or Full Chip Erase

SR.4 = (PAGE BUFFER) PROGRAM STATUS (PBPS)

- 1 = Error in (Page Buffer) Program
- 0 = Successful (Page Buffer) Program

SR.3 = V<sub>PP</sub> STATUS (VPPS)

- 1 = V<sub>PP</sub> LOW Detect, Operation Abort
- 0 = V<sub>PP</sub> OK

SR.2 = (PAGE BUFFER) PROGRAM SUSPEND STATUS (PBPSS)

- 1 = (Page Buffer) Program Suspended
- 0 = (Page Buffer) Program in Progress/Completed

SR.1 = DEVICE PROTECT STATUS (DPS)

- 1 = Erase or Program Attempted on a Locked Block, Operation Abort
- 0 = Unlocked

SR.0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

Notes:

Status Register indicates the status of the partition, not WSM (Write State Machine). Even if the SR.7 is "1", the WSM may be occupied by the other partition when the device is set to 2, 3 or 4 partitions configuration.

Check SR.7 or RY/ $\overline{\text{BY}}$  to determine block erase, full chip erase, (page buffer) program completion. SR.6 - SR.1 are invalid while SR.7 = "0".

If both SR.5 and SR.4 are "1"s after a block erase, full chip erase, (page buffer) program, set/clear block lock bit, set block lock-down bit or set partition configuration register attempt, an improper command sequence was entered.

SR.3 does not provide a continuous indication of V<sub>PP</sub> level. The WSM interrogates and indicates the V<sub>PP</sub> level only after Block Erase, Full Chip Erase, (Page Buffer) Program command sequences. SR.3 is not guaranteed to report accurate feedback when V<sub>PP</sub> ≠ V<sub>PPH</sub> or V<sub>PPLK</sub>.

SR.1 does not provide a continuous indication of block lock bit. The WSM interrogates the block lock bit only after Block Erase, Full Chip Erase, (Page Buffer) Program command sequences. It informs the system, depending on the attempted operation, if the block lock bit is set. Reading the block lock configuration codes after writing the Read Identifier Codes command indicates block lock bit status.

SR.15 - SR.8 and SR.0 are reserved for future use and should be masked out when polling the status register.

## Extended Status Register Definition

R	R	R	R	R	R	R	R
15	14	13	12	11	10	9	8
SMS	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

XSR.15-8 = RESERVED FOR FUTURE ENHANCEMENTS (R)

XSR.7 = STATE MACHINE STATUS (SMS)  
 1 = Page Buffer Program available  
 0 = Page Buffer Program not available

XSR.6-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

## Notes:

After issue a Page Buffer Program command (E8H), XSR.7="1" indicates that the entered command is accepted. If XSR.7 is "0", the command is not accepted and a next Page Buffer Program command (E8H) should be issued again to check if page buffer is available or not.

XSR.15-8 and XSR.6-0 are reserved for future use and should be masked out when polling the extended status register.

Partition Configuration Register Definition

R	R	R	R	R	PC2	PC1	PC0
15	14	13	12	11	10	9	8
R	R	R	R	R	R	R	R
7	6	5	4	3	2	1	0

PCR.15-11 = RESERVED FOR FUTURE ENHANCEMENTS (R)  
 PCR.10-8 = PARTITION CONFIGURATION (PC2-0)  
 000 = No partitioning. Dual Work is not allowed.  
 001 = Plane1-3 are merged into one partition.  
 (default in a bottom parameter device)  
 010 = Plane 0-1 and Plane 2-3 are merged into one partition respectively.  
 100 = Plane 0-2 are merged into one partition.  
 (default in a top parameter device)  
 011 = Plane 2-3 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.  
 110 = Plane 0-1 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.  
 101 = Plane 1-2 are merged into one partition. There are three partitions in this configuration. Dual work operation is available between any two partitions.

111 = There are four partitions in this configuration. Each plane corresponds to each partition respectively. Dual work operation is available between any two partitions.

PCR.7-0 = RESERVED FOR FUTURE ENHANCEMENTS (R)

Notes:  
 After power-up or device reset, PCR 10-8 (PC2-0) is set to "001" in a bottom parameter device and "100" in a top parameter device.

See the table below for more details.

PCR.15-11 and PCR.7-0 are reserved for future use and should be masked out when checking the partition configuration register.

Partition Configuration

PC2 PC1 PC0	PARTITIONING FOR DUAL WORK	PC2 PC1 PC0	PARTITIONING FOR DUAL WORK
0 0 0	PARTITION0 	0 1 1	PARTITION2 PARTITION1 PARTITION0 
0 0 1	PARTITION1 PARTITION0 	1 1 0	PARTITION2 PARTITION1 PARTITION0 
0 1 0	PARTITION1 PARTITION0 	1 0 1	PARTITION2 PARTITION1 PARTITION0 
1 0 0	PARTITION1 PARTITION0 	1 1 1	PARTITION3 PARTITION2 PARTITION1 PARTITION0 



## 7.4 Memory Map for Flash Memory

## Bottom Parameter

Bottom Parameter			
	BLOCK NUMBER	ADDRESS RANGE	
PLANE3 (UNIFORM PLANE)	134	32K-WORD	3F8000H - 3FFFFFFH
	133	32K-WORD	3F0000H - 3F7FFFH
	132	32K-WORD	3E8000H - 3EFFFFH
	131	32K-WORD	3E0000H - 3E7FFFH
	130	32K-WORD	3D8000H - 3DFFFFH
	129	32K-WORD	3D0000H - 3D7FFFH
	128	32K-WORD	3C8000H - 3CFFFFH
	127	32K-WORD	3C0000H - 3C7FFFH
	126	32K-WORD	3B8000H - 3BFFFFH
	125	32K-WORD	3B0000H - 3B7FFFH
	124	32K-WORD	3A8000H - 3AFFFFH
	123	32K-WORD	3A0000H - 3A7FFFH
	122	32K-WORD	398000H - 39FFFFH
	121	32K-WORD	390000H - 397FFFH
	120	32K-WORD	388000H - 38FFFFH
	119	32K-WORD	380000H - 387FFFH
	118	32K-WORD	378000H - 37FFFFH
	117	32K-WORD	370000H - 377FFFH
	116	32K-WORD	368000H - 36FFFFH
	115	32K-WORD	360000H - 367FFFH
	114	32K-WORD	358000H - 35FFFFH
	113	32K-WORD	350000H - 357FFFH
	112	32K-WORD	348000H - 34FFFFH
	111	32K-WORD	340000H - 347FFFH
	110	32K-WORD	338000H - 33FFFFH
	109	32K-WORD	330000H - 337FFFH
	108	32K-WORD	328000H - 32FFFFH
	107	32K-WORD	320000H - 327FFFH
	106	32K-WORD	318000H - 31FFFFH
	105	32K-WORD	310000H - 317FFFH
	104	32K-WORD	308000H - 30FFFFH
103	32K-WORD	300000H - 307FFFH	

PLANE2 (UNIFORM PLANE)	102	32K-WORD	2F8000H - 2FFFFFFH
	101	32K-WORD	2F0000H - 2F7FFFH
	100	32K-WORD	2E8000H - 2EFFFFH
	99	32K-WORD	2E0000H - 2E7FFFH
	98	32K-WORD	2D8000H - 2DFFFFH
	97	32K-WORD	2D0000H - 2D7FFFH
	96	32K-WORD	2C8000H - 2CFFFFH
	95	32K-WORD	2C0000H - 2C7FFFH
	94	32K-WORD	2B8000H - 2BFFFFH
	93	32K-WORD	2B0000H - 2B7FFFH
	92	32K-WORD	2A8000H - 2AFFFFH
	91	32K-WORD	2A0000H - 2A7FFFH
	90	32K-WORD	298000H - 29FFFFH
	89	32K-WORD	290000H - 297FFFH
	88	32K-WORD	288000H - 28FFFFH
	87	32K-WORD	280000H - 287FFFH
	86	32K-WORD	278000H - 27FFFFH
	85	32K-WORD	270000H - 277FFFH
	84	32K-WORD	268000H - 26FFFFH
	83	32K-WORD	260000H - 267FFFH
	82	32K-WORD	258000H - 25FFFFH
	81	32K-WORD	250000H - 257FFFH
	80	32K-WORD	248000H - 24FFFFH
	79	32K-WORD	240000H - 247FFFH
	78	32K-WORD	238000H - 23FFFFH
	77	32K-WORD	230000H - 237FFFH
	76	32K-WORD	228000H - 22FFFFH
	75	32K-WORD	220000H - 227FFFH
	74	32K-WORD	218000H - 21FFFFH
	73	32K-WORD	210000H - 217FFFH
	72	32K-WORD	208000H - 20FFFFH
71	32K-WORD	200000H - 207FFFH	

	BLOCK NUMBER	ADDRESS RANGE	
PLANE1 (UNIFORM PLANE)	70	32K-WORD	1F8000H - 1FFFFFFH
	69	32K-WORD	1F0000H - 1F7FFFH
	68	32K-WORD	1E8000H - 1EFFFFH
	67	32K-WORD	1E0000H - 1E7FFFH
	66	32K-WORD	1D8000H - 1DFFFFH
	65	32K-WORD	1D0000H - 1D7FFFH
	64	32K-WORD	1C8000H - 1CFFFFH
	63	32K-WORD	1C0000H - 1C7FFFH
	62	32K-WORD	1B8000H - 1BFFFFH
	61	32K-WORD	1B0000H - 1B7FFFH
	60	32K-WORD	1A8000H - 1AFFFFH
	59	32K-WORD	1A0000H - 1A7FFFH
	58	32K-WORD	198000H - 19FFFFH
	57	32K-WORD	190000H - 197FFFH
	56	32K-WORD	188000H - 18FFFFH
	55	32K-WORD	180000H - 187FFFH
	54	32K-WORD	178000H - 17FFFFH
	53	32K-WORD	170000H - 177FFFH
	52	32K-WORD	168000H - 16FFFFH
	51	32K-WORD	160000H - 167FFFH
	50	32K-WORD	158000H - 15FFFFH
	49	32K-WORD	150000H - 157FFFH
	48	32K-WORD	148000H - 14FFFFH
	47	32K-WORD	140000H - 147FFFH
	46	32K-WORD	138000H - 13FFFFH
	45	32K-WORD	130000H - 137FFFH
	44	32K-WORD	128000H - 12FFFFH
	43	32K-WORD	120000H - 127FFFH
	42	32K-WORD	118000H - 11FFFFH
	41	32K-WORD	110000H - 117FFFH
	40	32K-WORD	108000H - 10FFFFH
39	32K-WORD	100000H - 107FFFH	

PLANE0 (PARAMETER PLANE)	38	32K-WORD	0F8000H - 0FFFFFFH
	37	32K-WORD	0F0000H - 0F7FFFH
	36	32K-WORD	0E8000H - 0EFFFFH
	35	32K-WORD	0E0000H - 0E7FFFH
	34	32K-WORD	0D8000H - 0DFFFFH
	33	32K-WORD	0D0000H - 0D7FFFH
	32	32K-WORD	0C8000H - 0CFFFFH
	31	32K-WORD	0C0000H - 0C7FFFH
	30	32K-WORD	0B8000H - 0BFFFFH
	29	32K-WORD	0B0000H - 0B7FFFH
	28	32K-WORD	0A8000H - 0AFFFFH
	27	32K-WORD	0A0000H - 0A7FFFH
	26	32K-WORD	098000H - 09FFFFH
	25	32K-WORD	090000H - 097FFFH
	24	32K-WORD	088000H - 08FFFFH
	23	32K-WORD	080000H - 087FFFH
	22	32K-WORD	078000H - 07FFFFH
	21	32K-WORD	070000H - 077FFFH
	20	32K-WORD	068000H - 06FFFFH
	19	32K-WORD	060000H - 067FFFH
	18	32K-WORD	058000H - 05FFFFH
	17	32K-WORD	050000H - 057FFFH
	16	32K-WORD	048000H - 04FFFFH
	15	32K-WORD	040000H - 047FFFH
	14	32K-WORD	038000H - 03FFFFH
	13	32K-WORD	030000H - 037FFFH
	12	32K-WORD	028000H - 02FFFFH
	11	32K-WORD	020000H - 027FFFH
	10	32K-WORD	018000H - 01FFFFH
	9	32K-WORD	010000H - 017FFFH
	8	32K-WORD	008000H - 00FFFFH
7	4K-WORD	007000H - 007FFFH	
6	4K-WORD	006000H - 006FFFH	
5	4K-WORD	005000H - 005FFFH	
4	4K-WORD	004000H - 004FFFH	
3	4K-WORD	003000H - 003FFFH	
2	4K-WORD	002000H - 002FFFH	
1	4K-WORD	001000H - 001FFFH	
0	4K-WORD	000000H - 000FFFH	

## 7.5 DC Electrical Characteristics for Flash Memory

## DC Electrical Characteristics

(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

Symbol	Parameter		Notes	Min.	Typ.	Max.	Unit	Test Conditions
C <sub>IN</sub>	Input Capacitance		5			7	pF	V <sub>IN</sub> = 0V, f = 1MHz, T <sub>A</sub> = 25°C
C <sub>IO</sub>	I/O Capacitance		5			10	pF	V <sub>I/O</sub> = 0V, f = 1MHz, T <sub>A</sub> = 25°C
I <sub>LI</sub>	Input Leakage Current					±1	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>LO</sub>	Output Leakage Current					±1	μA	V <sub>OUT</sub> = V <sub>CC</sub> or GND
I <sub>CCS</sub>	V <sub>CC</sub> Standby Current		1, 8		4	20	μA	V <sub>CC</sub> = V <sub>CC</sub> Max., F <sub>2-CE</sub> = $\overline{\text{RST}}$ = V <sub>CC</sub> ±0.2V, $\overline{\text{WP}}$ = V <sub>CC</sub> or GND
I <sub>CCAS</sub>	V <sub>CC</sub> Automatic Power Savings Current		1, 4		4	20	μA	V <sub>CC</sub> = V <sub>CC</sub> Max., F <sub>2-CE</sub> = GND ±0.2V, $\overline{\text{WP}}$ = V <sub>CC</sub> or GND
I <sub>CCD</sub>	V <sub>CC</sub> Reset Power-Down Current		1		4	20	μA	$\overline{\text{RST}}$ = GND ±0.2V I <sub>OUT</sub> (RY/BY) = 0mA
I <sub>CCR</sub>	Average V <sub>CC</sub> Read Current Normal Mode		1, 7		15	25	mA	V <sub>CC</sub> = V <sub>CC</sub> Max., F <sub>2-CE</sub> = V <sub>IL</sub> , F- $\overline{\text{OE}}$ = V <sub>IH</sub> , f = 5MHz I <sub>OUT</sub> = 0mA
	Average V <sub>CC</sub> Read Current Page Mode	8 Word Read	1, 7		5	10	mA	
I <sub>CCW</sub>	V <sub>CC</sub> (Page Buffer) Program Current		1, 5, 7		20	60	mA	V <sub>PP</sub> = V <sub>PPH</sub>
I <sub>CCE</sub>	V <sub>CC</sub> Block Erase, Full Chip Erase Current		1, 5, 7		10	30	mA	V <sub>PP</sub> = V <sub>PPH</sub>
I <sub>CCWS</sub> I <sub>CCES</sub>	V <sub>CC</sub> (Page Buffer) Program or Block Erase Suspend Current		1, 2, 7		10	200	μA	F <sub>2-CE</sub> = V <sub>IH</sub>
I <sub>PPS</sub> I <sub>PPR</sub>	V <sub>PP</sub> Standby or Read Current		1, 6, 7		2	5	μA	V <sub>PP</sub> ≤ V <sub>CC</sub>
I <sub>PPW</sub>	V <sub>PP</sub> (Page Buffer) Program Current		1,5,6,7		2	5	μA	V <sub>PP</sub> = V <sub>PPH</sub>
I <sub>PPE</sub>	V <sub>PP</sub> Block Erase, Full Chip Erase Current		1,5,6,7		2	5	μA	V <sub>PP</sub> = V <sub>PPH</sub>
I <sub>PPWS</sub>	V <sub>PP</sub> (Page Buffer) Program Suspend Current		1, 6, 7		2	5	μA	V <sub>PP</sub> = V <sub>PPH</sub>
I <sub>PPES</sub>	V <sub>PP</sub> Block Erase Suspend Current		1, 6, 7		2	5	μA	V <sub>PP</sub> = V <sub>PPH</sub>

## DC Electrical Characteristics (Continue)

(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
V <sub>IL</sub>	Input Low Voltage	5	-0.3		0.4	V	
V <sub>IH</sub>	Input High Voltage	5	V <sub>CC</sub> -0.4		V <sub>CC</sub> +0.3	V	
V <sub>OL</sub>	Output Low Voltage	5, 8			0.2V <sub>CC</sub>	V	I <sub>OL</sub> = 0.5mA
V <sub>OH</sub>	Output High Voltage	5	2.2			V	I <sub>OH</sub> = -0.5mA
V <sub>PPLK</sub>	V <sub>PP</sub> Lockout during Normal Operations	3,5,6			0.4	V	
V <sub>PPH</sub>	V <sub>PP</sub> during Block Erase, Full Chip Erase, (Page Buffer) Program Operations	6	1.65	3	3.1	V	
V <sub>LKO</sub>	V <sub>CC</sub> Lockout Voltage		1.5			V	

## Notes:

- All currents are in RMS unless otherwise noted. Typical values are the reference values at V<sub>CC</sub> = 3.0V and T<sub>A</sub> = +25°C unless V<sub>CC</sub> is specified.
- I<sub>CCWS</sub> and I<sub>CCES</sub> are specified with the device de-selected. If read or (page buffer) program is executed while in block erase suspend mode, the device's current draw is the sum of I<sub>CCES</sub> and I<sub>CCR</sub> or I<sub>CCW</sub>. If read is executed while in (page buffer) program suspend mode, the device's current draw is the sum of I<sub>CCWS</sub> and I<sub>CCR</sub>.
- Block erase, full chip erase, (page buffer) program are inhibited when V<sub>PP</sub> ≤ V<sub>PPLK</sub>, and not guaranteed outside the specified voltage.
- The Automatic Power Savings (APS) feature automatically places the device in power save mode after read cycle completion. Standard address access timings (t<sub>AVQV</sub>) provide new data when addresses are changed.
- Sampled, not 100% tested.
- V<sub>PP</sub> is not used for power supply pin. With V<sub>PP</sub> ≤ V<sub>PPLK</sub>, block erase, full chip erase, (page buffer) program cannot be executed and should not be attempted.
- The operating current in dual work is the sum of the operating current (read, erase, program) in each plane.
- Includes RY/BY

## 7.6 AC Electrical Characteristics for Flash Memory

## 7.6.1 AC Test Conditions

Input Pulse Level	0 V to 2.7 V
Input Rise and Fall Time	5 ns
Input and Output Timing Ref. level	1.35 V
Output Load	1TTL +C <sub>L</sub> (50pF)

## 7.6.2 Read Cycle

(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t <sub>AVAV</sub>	Read Cycle Time		65		ns
t <sub>AVQV</sub>	Address to Output Delay			65	ns
t <sub>ELQV</sub>	F <sub>2</sub> - $\overline{\text{CE}}$ to Output Delay	2		65	ns
t <sub>APA</sub>	Page Address Access Time			25	ns
t <sub>GLQV</sub>	F- $\overline{\text{OE}}$ to Output Delay	2		20	ns
t <sub>PHQV</sub>	$\overline{\text{RST}}$ High to Output Delay			150	ns
t <sub>EHQZ</sub> , t <sub>GHQZ</sub>	F <sub>2</sub> - $\overline{\text{CE}}$ or F- $\overline{\text{OE}}$ to Output in High-Z, Whichever Occurs First	1		20	ns
t <sub>ELQX</sub>	F <sub>2</sub> - $\overline{\text{CE}}$ to Output in Low-Z	1	0		ns
t <sub>GLQX</sub>	F- $\overline{\text{OE}}$ to Output in Low-Z	1	0		ns
t <sub>OH</sub>	Output Hold from First Occurring Address, F <sub>2</sub> - $\overline{\text{CE}}$ or F- $\overline{\text{OE}}$ Change	1	0		ns
t <sub>AVEL</sub> , t <sub>AVGL</sub>	Address Setup to F <sub>2</sub> - $\overline{\text{CE}}$ and F- $\overline{\text{OE}}$ Going Low for Reading Status Register	3,5	10		ns
t <sub>ELAX</sub> , t <sub>GLAX</sub>	Address Hold from F <sub>2</sub> - $\overline{\text{CE}}$ and F- $\overline{\text{OE}}$ Going Low for Reading Status Register	4,5	30		ns
t <sub>EHGL</sub> , t <sub>GHGL</sub>	F <sub>2</sub> - $\overline{\text{CE}}$ and F- $\overline{\text{OE}}$ Pulse Width High for Reading Status Register	5	15		ns

## Notes:

1. Sampled, not 100% tested.
2. F- $\overline{\text{OE}}$  may be delayed up to t<sub>ELQV</sub> - t<sub>GLQV</sub> after the falling edge of F<sub>2</sub>- $\overline{\text{CE}}$  without impact to t<sub>ELQV</sub>.
3. Address setup time (t<sub>AVEL</sub>, t<sub>AVGL</sub>) is defined from the falling edge of F<sub>2</sub>- $\overline{\text{CE}}$  or F- $\overline{\text{OE}}$  (whichever goes low last).
4. Address hold time (t<sub>ELAX</sub>, t<sub>GLAX</sub>) is defined from the falling edge of F<sub>2</sub>- $\overline{\text{CE}}$  or F- $\overline{\text{OE}}$  (whichever goes low last).
5. Specifications t<sub>AVEL</sub>, t<sub>AVGL</sub>, t<sub>ELAX</sub>, t<sub>GLAX</sub> and t<sub>EHGL</sub>, t<sub>GHGL</sub> for read operations apply to only status register read operations.

7.6.3 Write Cycle (F- $\overline{\text{WE}}$  / F<sub>2</sub>- $\overline{\text{CE}}$  Controlled)<sup>(1,2)</sup>(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t <sub>AVAV</sub>	Write Cycle Time		65		ns
t <sub>PHWL</sub> (t <sub>PHL</sub> )	$\overline{\text{RST}}$ High Recovery to F- $\overline{\text{WE}}$ (F <sub>2</sub> - $\overline{\text{CE}}$ ) Going Low	3	150		ns
t <sub>ELWL</sub> (t <sub>LEL</sub> )	F <sub>2</sub> - $\overline{\text{CE}}$ (F- $\overline{\text{WE}}$ ) Setup to F- $\overline{\text{WE}}$ (F <sub>2</sub> - $\overline{\text{CE}}$ ) Going Low		0		ns
t <sub>WLWH</sub> (t <sub>LEH</sub> )	F- $\overline{\text{WE}}$ (F <sub>2</sub> - $\overline{\text{CE}}$ ) Pulse Width	4	50		ns
t <sub>DVWH</sub> (t <sub>DVEH</sub> )	Data Setup to F- $\overline{\text{WE}}$ (F <sub>2</sub> - $\overline{\text{CE}}$ ) Going High	8	40		ns
t <sub>AVWH</sub> (t <sub>AVEH</sub> )	Address Setup to F- $\overline{\text{WE}}$ (F <sub>2</sub> - $\overline{\text{CE}}$ ) Going High	8	50		ns
t <sub>WHEH</sub> (t <sub>EHWH</sub> )	F <sub>2</sub> - $\overline{\text{CE}}$ (F- $\overline{\text{WE}}$ ) Hold from F- $\overline{\text{WE}}$ (F <sub>2</sub> - $\overline{\text{CE}}$ ) High		0		ns
t <sub>WHDX</sub> (t <sub>EHDX</sub> )	Data Hold from F- $\overline{\text{WE}}$ (F <sub>2</sub> - $\overline{\text{CE}}$ ) High		0		ns
t <sub>WHAX</sub> (t <sub>EHAX</sub> )	Address Hold from F- $\overline{\text{WE}}$ (F <sub>2</sub> - $\overline{\text{CE}}$ ) High		0		ns
t <sub>WHWL</sub> (t <sub>EHHL</sub> )	F- $\overline{\text{WE}}$ (F <sub>2</sub> - $\overline{\text{CE}}$ ) Pulse Width High	5	15		ns
t <sub>SHWH</sub> (t <sub>SEH</sub> )	$\overline{\text{WP}}$ High Setup to F- $\overline{\text{WE}}$ (F <sub>2</sub> - $\overline{\text{CE}}$ ) Going High	3	0		ns
t <sub>VVWH</sub> (t <sub>VVEH</sub> )	V <sub>PP</sub> Setup to F- $\overline{\text{WE}}$ (F <sub>2</sub> - $\overline{\text{CE}}$ ) Going High	3	200		ns
t <sub>WHGL</sub> (t <sub>EHGL</sub> )	Write Recovery before Read		30		ns
t <sub>QVSL</sub>	$\overline{\text{WP}}$ High Hold from Valid SRD, RY/ $\overline{\text{BY}}$ High-Z	3, 6	0		ns
t <sub>QVVL</sub>	V <sub>PP</sub> Hold from Valid SRD, RY/ $\overline{\text{BY}}$ High-Z	3, 6	0		ns
t <sub>WHR0</sub> (t <sub>EHR0</sub> )	F- $\overline{\text{WE}}$ (F <sub>2</sub> - $\overline{\text{CE}}$ ) High to SR.7 Going "0"	3, 7		t <sub>AVQV</sub> +50	ns
t <sub>WHRL</sub> (t <sub>EHRL</sub> )	F- $\overline{\text{WE}}$ (F <sub>2</sub> - $\overline{\text{CE}}$ ) High to RY/ $\overline{\text{BY}}$ Going Low	3		100	ns

## Notes:

- The timing characteristics for reading the status register during block erase, full chip erase, (page buffer) program operations are the same as during read-only operations. See the AC Characteristics for read cycle.
- A write operation can be initiated and terminated with either F<sub>2</sub>- $\overline{\text{CE}}$  or F- $\overline{\text{WE}}$ .
- Sampled, not 100% tested.
- Write pulse width (t<sub>WP</sub>) is defined from the falling edge of F<sub>2</sub>- $\overline{\text{CE}}$  or F- $\overline{\text{WE}}$  (whichever goes low last) to the rising edge of F<sub>2</sub>- $\overline{\text{CE}}$  or F- $\overline{\text{WE}}$  (whichever goes high first). Hence, t<sub>WP</sub>=t<sub>WLWH</sub>=t<sub>ELEH</sub>=t<sub>WLEH</sub>=t<sub>ELWH</sub>.
- Write pulse width high (t<sub>WPH</sub>) is defined from the rising edge of F<sub>2</sub>- $\overline{\text{CE}}$  or F- $\overline{\text{WE}}$  (whichever goes high first) to the falling edge of F<sub>2</sub>- $\overline{\text{CE}}$  or F- $\overline{\text{WE}}$  (whichever goes low last). Hence, t<sub>WPH</sub>=t<sub>WHWL</sub>=t<sub>EHEL</sub>=t<sub>WHEL</sub>=t<sub>EHWL</sub>.
- V<sub>PP</sub> should be held at V<sub>PP</sub>=V<sub>PPH</sub> until determination of block erase, full chip erase, (page buffer) program success (SR.1/3/4/5=0).
- t<sub>WHR0</sub> (t<sub>EHR0</sub>) after the Read Query or Read Identifier Codes command=t<sub>AVQV</sub>+100ns.
- See 7.2.1 Command Definitions for valid address and data for block erase, full chip erase, (page buffer) program or lock bit configuration.

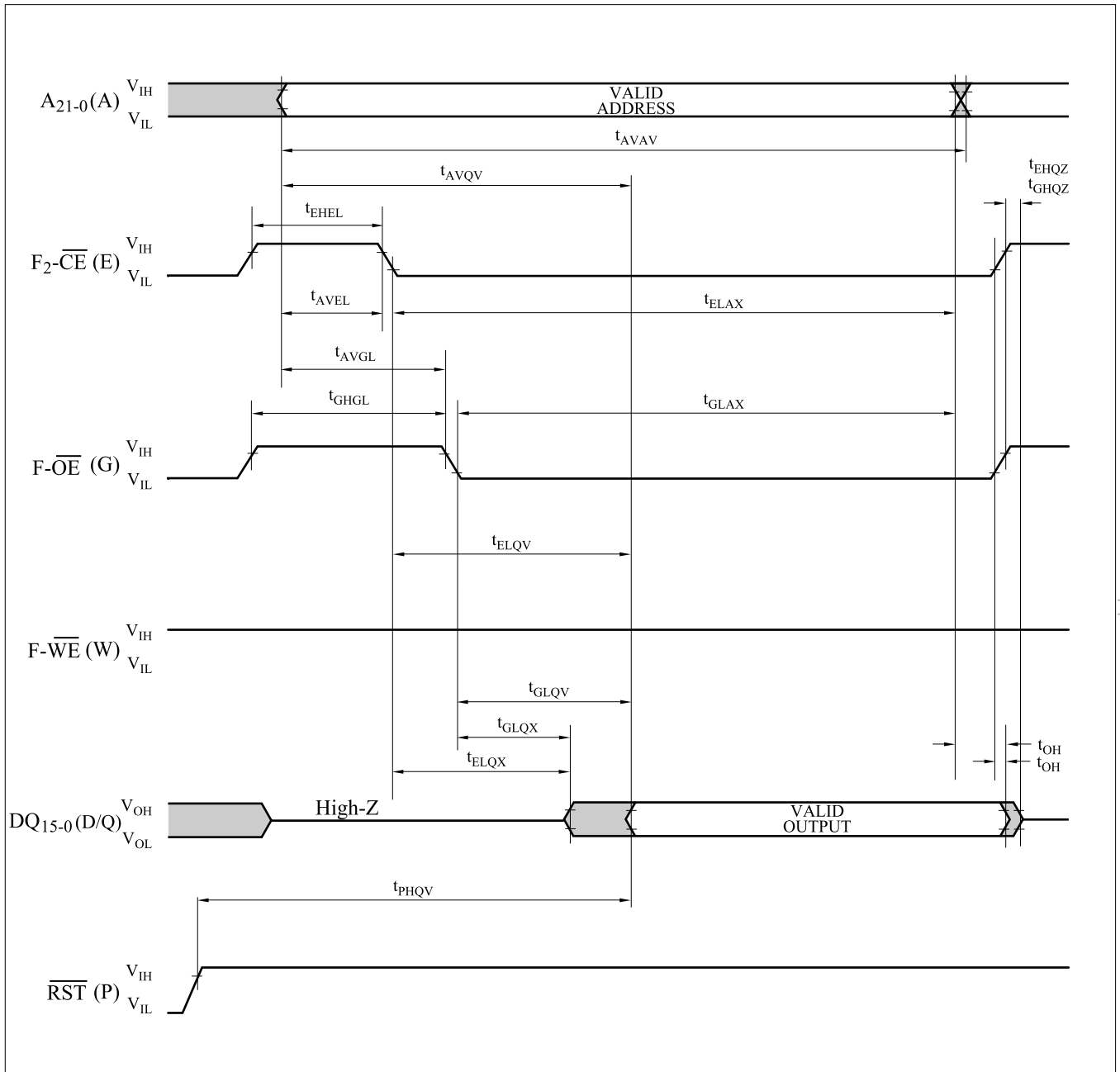
7.6.4 Block Erase, Full Chip Erase, (Page Buffer) Program Performance <sup>(3)</sup>(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

Symbol	Parameter	Notes	Page Buffer Command is Used or not Used	V <sub>PP</sub> =V <sub>PPH</sub>			Unit
				Min.	Typ. <sup>(1)</sup>	Max. <sup>(2)</sup>	
t <sub>WPB</sub>	4K-Word Parameter Block Program Time	2	Not Used		0.05	0.3	s
		2	Used		0.03	0.12	s
t <sub>WMB</sub>	32K-Word Main Block Program Time	2	Not Used		0.38	2.4	s
		2	Used		0.24	1	s
t <sub>WHQV1</sub> / t <sub>EHQV1</sub>	Word Program Time	2	Not Used		11	200	μs
		2	Used		7	100	μs
t <sub>WHQV2</sub> / t <sub>EHQV2</sub>	4K-Word Parameter Block Erase Time	2	-		0.3	4	s
t <sub>WHQV3</sub> / t <sub>EHQV3</sub>	32K-Word Main Block Erase Time	2	-		0.6	5	s
	Full Chip Erase Time	2			80	700	s
t <sub>WHRH1</sub> / t <sub>EHRH1</sub>	(Page Buffer) Program Suspend Latency Time to Read	4	-		5	10	μs
t <sub>WHRH2</sub> / t <sub>EHRH2</sub>	Block Erase Suspend Latency Time to Read	4	-		5	20	μs
t <sub>ERES</sub>	Latency Time from Block Erase Resume Command to Block Erase Suspend Command	5	-	500			μs

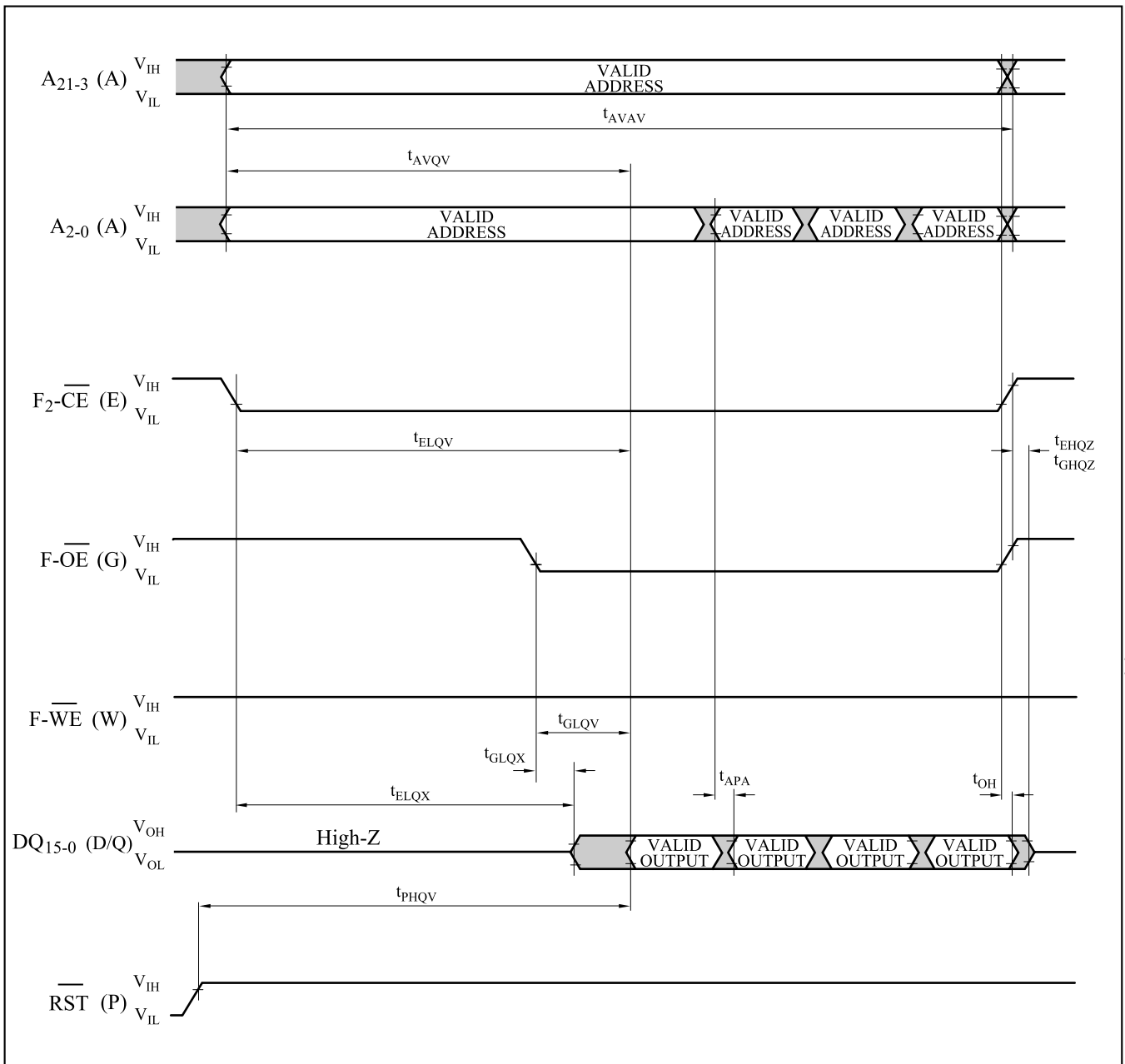
## Notes:

1. Typical values measured at V<sub>CC</sub> = 3.0V, V<sub>PP</sub> = 3.0V, and T<sub>A</sub> = +25°C. Assumes corresponding lock bits are not set. Subject to change based on device characterization.
2. Excludes external system-level overhead.
3. Sampled, but not 100% tested.
4. A latency time is required from writing suspend command (F<sub>2</sub> $\overline{\text{WE}}$  or F<sub>2</sub> $\overline{\text{CE}}$  going high) until SR.7 going "1" or RY/ $\overline{\text{BY}}$  going High-Z.
5. If the interval time from a Block Erase Resume command to a subsequent Block Erase Suspend command is shorter than t<sub>ERES</sub> and its sequence is repeated, the block erase operation may not be finished.

## 7.6.5 Flash Memory AC Characteristics Timing Chart

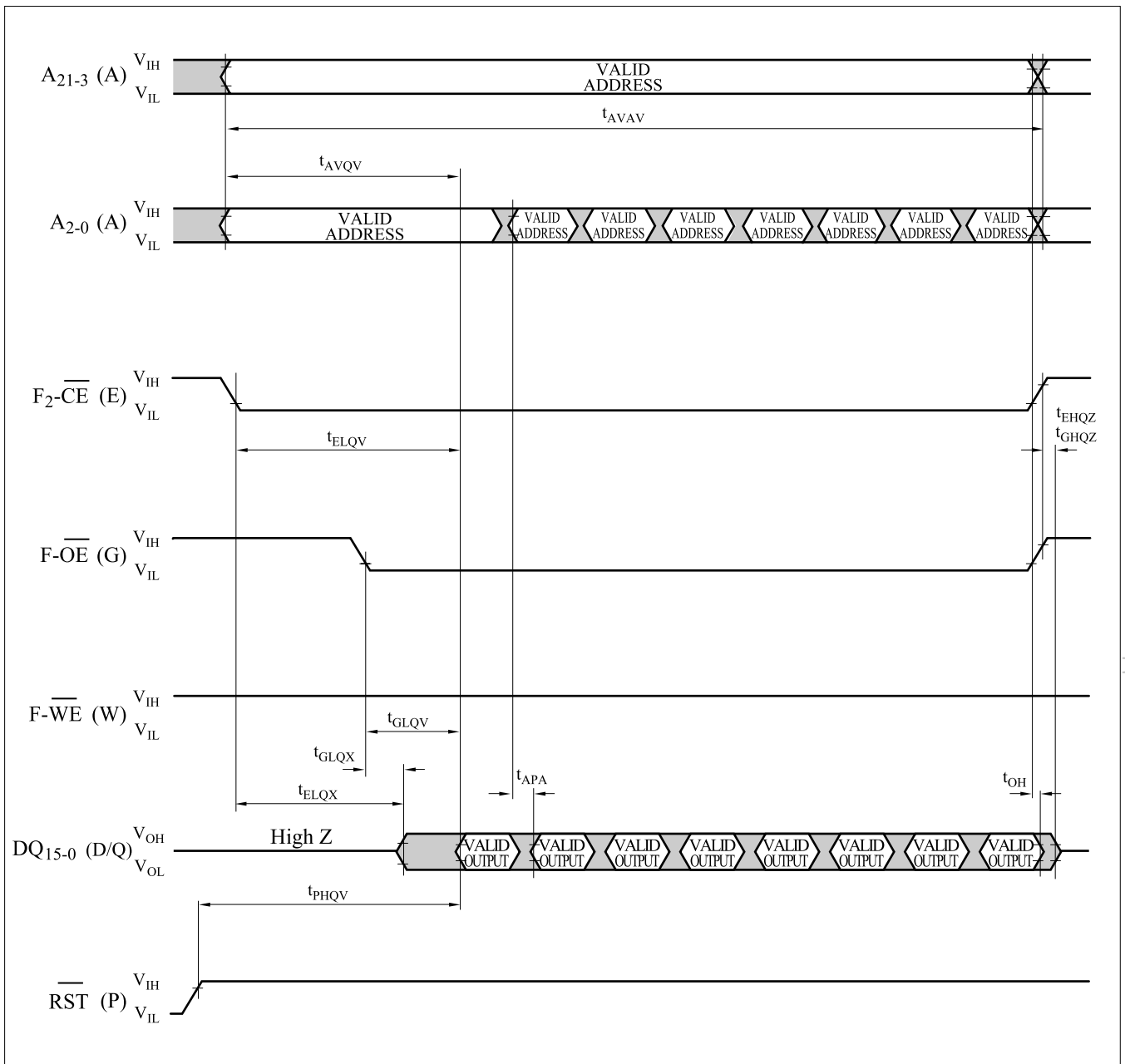
AC Waveform for Single Asynchronous Read Operations from Status Register, Identifier Codes or Query Code

### AC Waveform for Asynchronous 4-Word Page Mode Read Operations from Main Blocks or Parameter Blocks



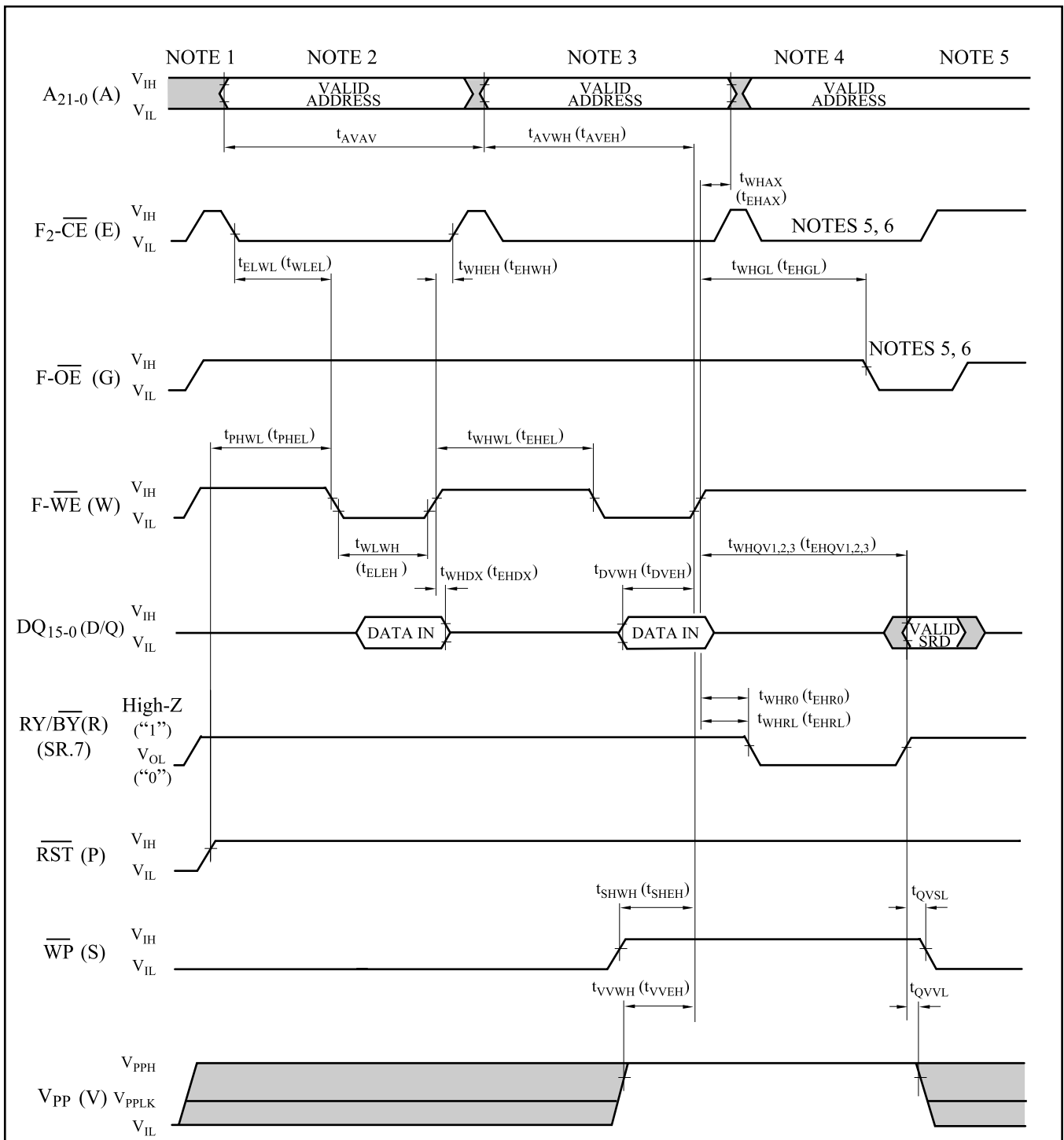


**AC Waveform for Asynchronous 8-Word Page Mode Read Operations from Main Blocks or Parameter Blocks**



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AC Waveform for Write Operations (F- $\overline{WE}$  / F2- $\overline{CE}$  Controlled)

## Notes:

1. VCC power-up and standby.
2. Write each first cycle command.
3. Write each second cycle command or valid address and data.
4. Automated erase or program delay.
5. Read status register data.
6. For read operation, F- $\overline{OE}$  and F2- $\overline{CE}$  must be driven active, and F- $\overline{WE}$  de-asserted.

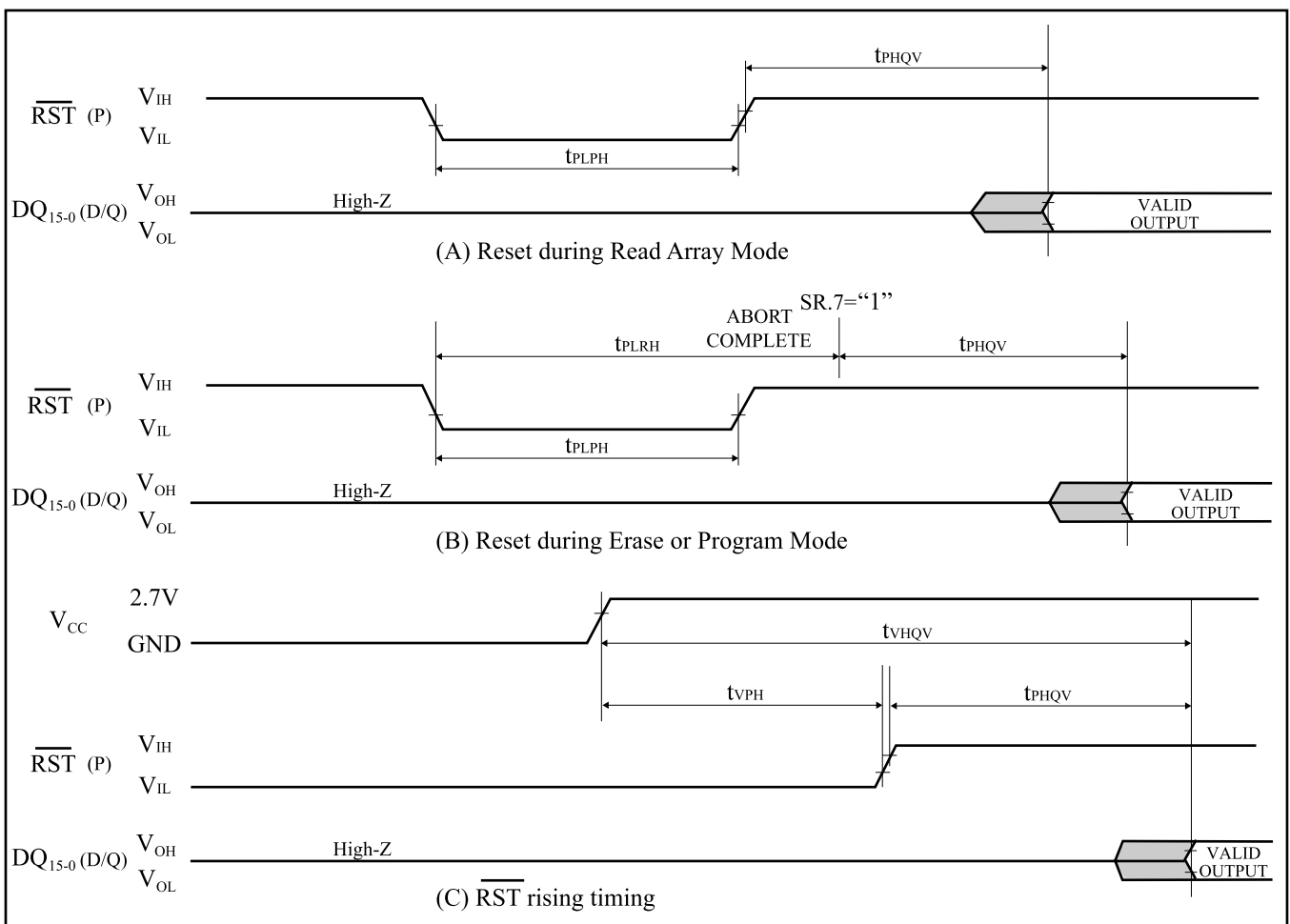
## 7.6.6 Reset Operations

 $(T_A = -25^\circ\text{C to } +85^\circ\text{C}, V_{CC} = 2.7\text{V to } 3.1\text{V})$ 

Symbol	Parameter	Notes	Min.	Max.	Unit
$t_{PLPH}$	$\overline{\text{RST}}$ Low to Reset during Read ( $\overline{\text{RST}}$ should be low during power-up.)	1, 2, 3	100		ns
$t_{PLRH}$	$\overline{\text{RST}}$ Low to Reset during Erase or Program	1, 3, 4		22	$\mu\text{s}$
$t_{VPH}$	$V_{CC} = 2.7\text{V to } \overline{\text{RST}}$ High	1, 3, 5	100		ns
$t_{VHQV}$	$V_{CC} = 2.7\text{V to Output Delay}$	3		1	ms

## Notes:

1. A reset time,  $t_{PHQV}$ , is required from the later of SR.7 (RY/ $\overline{\text{BY}}$ ) going "1" (High-Z) or  $\overline{\text{RST}}$  going high until outputs are valid. See the AC Characteristics - read cycle for  $t_{PHQV}$ .
2.  $t_{PLPH}$  is  $<100\text{ns}$  the device may still reset but this is not guaranteed.
3. Sampled, not 100% tested.
4. If  $\overline{\text{RST}}$  asserted while a block erase, full chip erase or (page buffer) program operation is not executing, the reset will complete within 100ns.
5. When the device power-up, holding  $\overline{\text{RST}}$  low minimum 100ns is required after  $V_{CC}$  has been in predefined range and also has been in stable there.

AC Waveform for Reset Operation

## 8. Smartcombo RAM

## 8.1 Truth Table

8.1.1 Bus Operation <sup>(1)</sup>

Smartcombo RAM	Notes	SC- $\overline{CE}_1$	CE <sub>2</sub>	S- $\overline{OE}$	S- $\overline{WE}$	$\overline{LB}$	$\overline{UB}$	DQ <sub>0</sub> to Q <sub>15</sub>
Read		L	H	L	H	(3)		(3)
Output Disable				H	H	X	X	High - Z
Write				H	L	(3)		(3)
Standby		H	L	X	X	X	X	High - Z
		X				H	H	
Sleep	2	X				X	X	

Notes:

1. L = V<sub>IL</sub>, H = V<sub>IH</sub>, X = H or L, High-Z = High impedance. Refer to the DC Characteristics.
2. CE<sub>2</sub> pin must be fixed to high level except sleep mode.
3.  $\overline{LB}$ ,  $\overline{UB}$  Control Mode

$\overline{LB}$	$\overline{UB}$	DQ <sub>0</sub> to DQ <sub>7</sub>	DQ <sub>8</sub> to DQ <sub>15</sub>
L	L	D <sub>OUT</sub> /D <sub>IN</sub>	D <sub>OUT</sub> /D <sub>IN</sub>
L	H	D <sub>OUT</sub> /D <sub>IN</sub>	High - Z
H	L	High - Z	D <sub>OUT</sub> /D <sub>IN</sub>

## 8.2 DC Electrical Characteristics for Smartcombo RAM

## DC Electrical Characteristics

(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
C <sub>IN</sub>	Input Capacitance	1			8	pF	V <sub>IN</sub> = 0V
C <sub>IO</sub>	I/O Capacitance	1			10	pF	V <sub>I/O</sub> = 0V
I <sub>LI</sub>	Input Leakage Current				±1	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>LO</sub>	Output Leakage Current				±1	μA	V <sub>OUT</sub> = V <sub>CC</sub> or GND
I <sub>SB</sub>	V <sub>CC</sub> Standby Current	2			100	μA	SC- $\overline{CE}_1 \geq V_{CC} - 0.2V$ , CE <sub>2</sub> ≥ V <sub>CC</sub> - 0.2V
I <sub>SLP</sub>	V <sub>CC</sub> Sleep Mode Current	3			30	μA	SC- $\overline{CE}_1 \geq V_{CC} - 0.2V$ , CE <sub>2</sub> ≤ 0.2V
I <sub>CC1</sub>	V <sub>CC</sub> Operation Current				50	mA	t <sub>CYCLE</sub> = Min., I <sub>I/O</sub> = 0mA, SC- $\overline{CE}_1 = V_{IL}$
V <sub>IL</sub>	Input Low Voltage	1	-0.3		0.4	V	
V <sub>IH</sub>	Input High Voltage	1	V <sub>CC</sub> -0.4		V <sub>CC</sub> +0.3	V	
V <sub>OL</sub>	Output Low Voltage	1			0.2V <sub>CC</sub>	V	I <sub>OL</sub> = 0.5mA
V <sub>OH</sub>	Output High Voltage	1	2.2			V	I <sub>OH</sub> = -0.5mA

Notes:

1. Sampled, not 100% tested.
2. Memory cell data is held. (CE<sub>2</sub> = "V<sub>IH</sub>")
3. Memory cell data is not held. (CE<sub>2</sub> = "V<sub>IL</sub>")

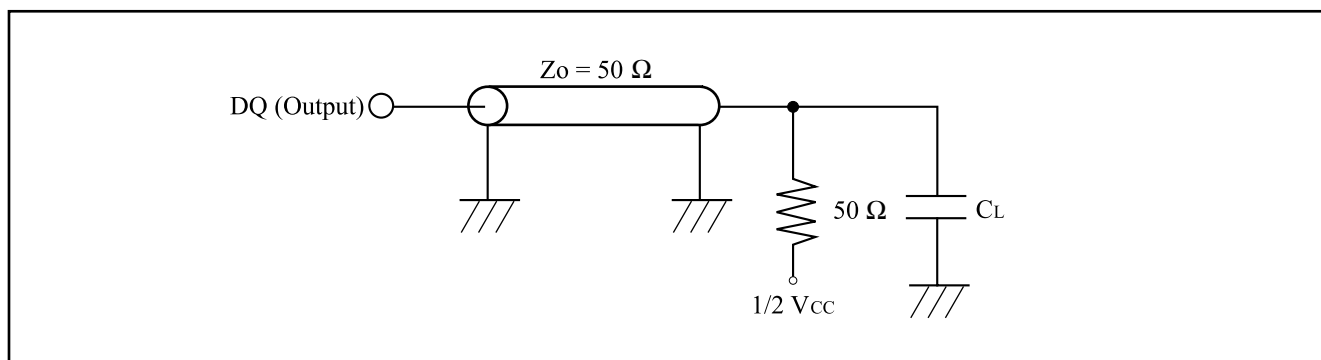
### 8.3 AC Electrical Characteristics for Smartcombo RAM

#### 8.3.1 AC Test Conditions

Input Pulse Level	$0.2V_{CC}$ to $0.8V_{CC}$
Input Rise and Fall Time	5 ns
Input and Output Timing Ref. Level	$1/2 V_{CC}$
Output Load	1TTL + $C_L$ (30pF) <sup>(1, 2)</sup>

Notes:

1. Including scope and socket capacitance.
2. AC characteristics directed with the note should be measured with the output load shown in below.



## 8.3.2 Read Cycle

(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t <sub>RC</sub>	Read Cycle Time		65		ns
t <sub>AA</sub>	Address Access Time			65	ns
t <sub>ACE</sub>	Chip Enable Access Time			65	ns
t <sub>OE</sub>	Output Enable to Output Valid			45	ns
t <sub>BE</sub>	Byte Enable Access Time			65	ns
t <sub>PAA</sub>	Page Access Time			20	ns
t <sub>OH</sub>	Output Hold from Address Change		5		ns
t <sub>PRC</sub>	Page Read Cycle Time		20		ns
t <sub>CLZ</sub>	SC- $\overline{CE}_1$ Low to Output Active		10		ns
t <sub>OLZ</sub>	S- $\overline{OE}$ Low to Output Active		5		ns
t <sub>BLZ</sub>	$\overline{UB}$ or $\overline{LB}$ Low to Output Active		5		ns
t <sub>CHZ</sub>	SC- $\overline{CE}_1$ High to Output in High-Z			25	ns
t <sub>OHZ</sub>	S- $\overline{OE}$ High to Output in High-Z			25	ns
t <sub>BHZ</sub>	$\overline{UB}$ or $\overline{LB}$ High to Output in High-Z			25	ns
t <sub>ASO</sub>	Address Setup to S- $\overline{OE}$ Low		0		ns
t <sub>OHAH</sub>	S- $\overline{OE}$ High Level to Address Hold		-5		ns
t <sub>CHAH</sub>	SC- $\overline{CE}_1$ High Level to Address Hold		0		ns
t <sub>BHAH</sub>	$\overline{LB}$ , $\overline{UB}$ High Level to Address Hold	2	0		ns
t <sub>CLOL</sub>	SC- $\overline{CE}_1$ Low Level to S- $\overline{OE}$ Low Level	1	0	10,000	ns
t <sub>OLCH</sub>	S- $\overline{OE}$ Low Level to SC- $\overline{CE}_1$ High Level		45		ns
t <sub>CP</sub>	SC- $\overline{CE}_1$ High Level Pulse Width		10		ns
t <sub>BP</sub>	$\overline{LB}$ , $\overline{UB}$ High Level Pulse Width		10		ns
t <sub>OP</sub>	S- $\overline{OE}$ High Level Pulse Width	1	2	10,000	ns

## Notes:

- t<sub>CLOL</sub> and t<sub>OP</sub> (Max.) are applied while SC- $\overline{CE}_1$  is being hold at low level.
- t<sub>BHAH</sub> is specified after both  $\overline{LB}$  and  $\overline{UB}$  are High.

## 8.3.3 Write Cycle

(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t <sub>WC</sub>	Write Cycle Time		65		ns
t <sub>CW</sub>	Chip Enable to End of Write		55		ns
t <sub>AW</sub>	Address Valid to End of Write		55		ns
t <sub>BW</sub>	Byte Select Time		55		ns
t <sub>WP</sub>	Write Pulse Width		50		ns
t <sub>WR</sub>	Write Recovery Time		0		ns
t <sub>CP</sub>	SC- $\overline{\text{CE}}_1$ High Level Pulse Width		10		ns
t <sub>BP</sub>	$\overline{\text{LB}}$ , $\overline{\text{UB}}$ High Level Pulse Width		10		ns
t <sub>WHP</sub>	S- $\overline{\text{WE}}$ High Pulse Width		10		ns
t <sub>WHZ</sub>	S- $\overline{\text{WE}}$ Low to Output in High-Z			25	ns
t <sub>OW</sub>	S- $\overline{\text{WE}}$ High to Output Active		15		ns
t <sub>AS</sub>	Address Setup Time		0		ns
t <sub>DW</sub>	Input Data Setup Time		30		ns
t <sub>DH</sub>	Input Data Hold Time		0		ns
t <sub>OHAH</sub>	S- $\overline{\text{OE}}$ High Level to Address Hold		-5		ns
t <sub>CHAH</sub>	SC- $\overline{\text{CE}}_1$ High Level to Address Hold		0		ns
t <sub>BHAH</sub>	$\overline{\text{LB}}$ , $\overline{\text{UB}}$ High Level to Address Hold	2	0		ns
t <sub>OES</sub>	S- $\overline{\text{OE}}$ High Level to S- $\overline{\text{WE}}$ Set	1	0	10,000	ns
t <sub>OEH</sub>	S- $\overline{\text{WE}}$ High Level to S- $\overline{\text{OE}}$ Set	1	10	10,000	ns

## Notes:

1. t<sub>OES</sub> and t<sub>OEH</sub> (Max.) are applied while SC- $\overline{\text{CE}}_1$  is being hold at low level.
2. t<sub>BHAH</sub> is specified after both  $\overline{\text{LB}}$  and  $\overline{\text{UB}}$  are High.



## 8.3.4 Initialization

(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t <sub>VHMH</sub>	Power Application to CE <sub>2</sub> Low Level Hold		50		μs
t <sub>CHMH</sub>	SC- $\overline{\text{CE}}_1$ High Level to CE <sub>2</sub> High Level		10		ns
t <sub>MHCL</sub>	Following Power Application CE <sub>2</sub> High Level Hold to SC- $\overline{\text{CE}}_1$ Low Level		300		μs

## 8.3.5 Sleep Mode Entry / Exit

(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

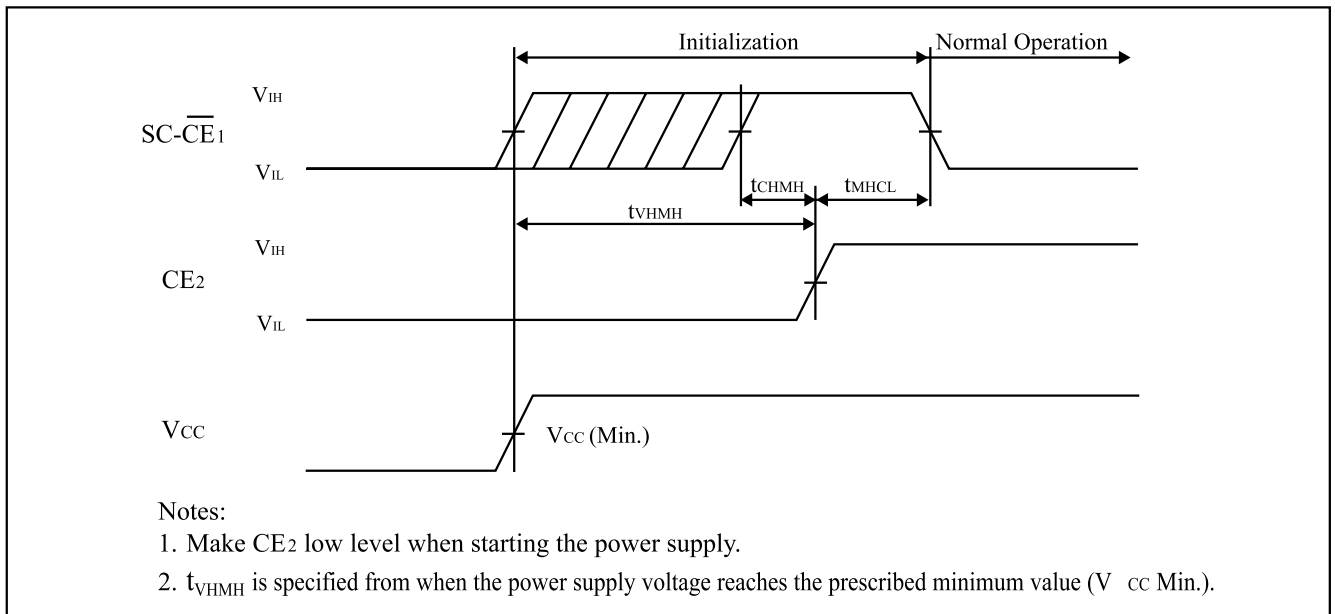
Symbol	Parameter	Notes	Min.	Max.	Unit
t <sub>CHML</sub>	Sleep Mode Entry SC- $\overline{\text{CE}}_1$ High Level to CE <sub>2</sub> Low Level		0		ns
t <sub>MHCL</sub>	Sleep Mode Exit to Normal Operation CE <sub>2</sub> High Level to SC- $\overline{\text{CE}}_1$ Low Level		300		μs

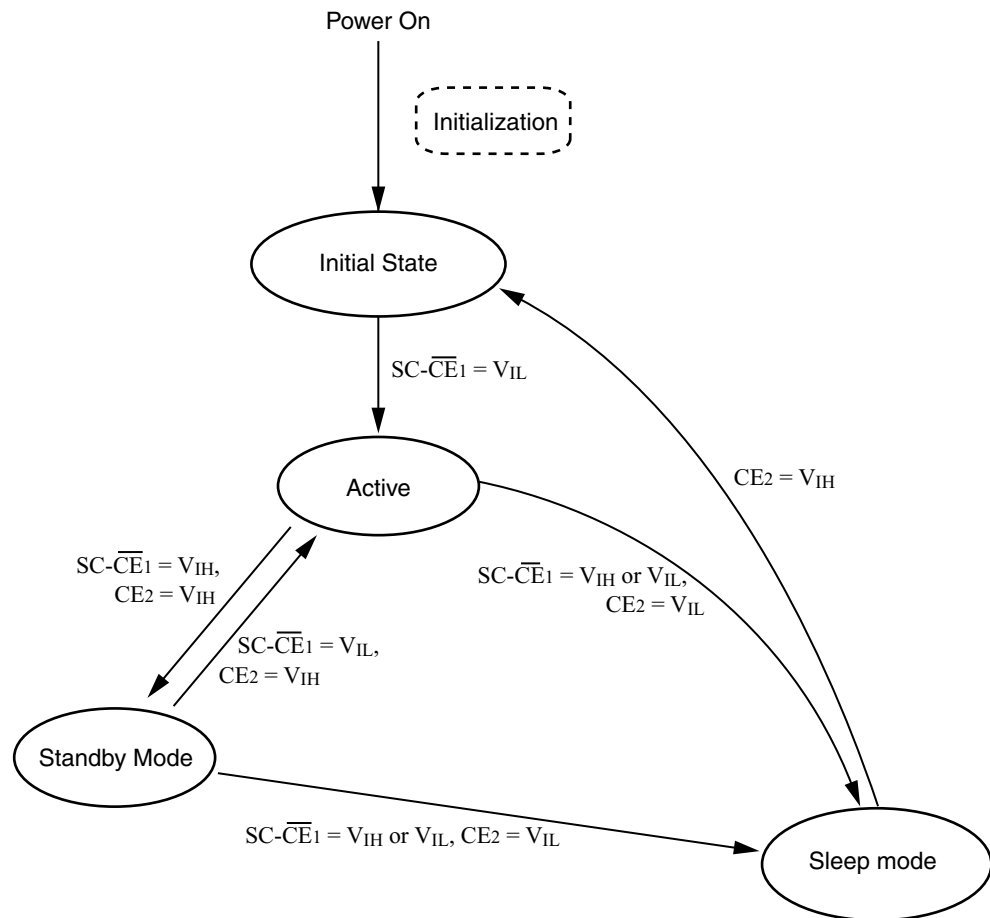
#### 8.4 Initialization

Initialize the power application using the following sequence to stabilize internal circuits.

- (1) Following power application, make  $CE_2$  high level after fixing  $CE_2$  to low level for the period of  $t_{VHMH}$ . Make  $SC-\overline{CE}_1$  high level before making  $CE_2$  high level.
- (2)  $SC-\overline{CE}_1$  and  $CE_2$  are fixed to high level for the period of  $t_{MHCL}$ .

Normal operation is possible after the completion of initialization.



Standby Mode State Machine

## 8.5 Page Read Operation

### 8.5.1 Features of Page Read Operation <sup>(2)</sup>

Features	Notes	8 Words Mode
Page Length		8 words
Page Read-corresponding Addresses		$A_2, A_1, A_0$
Page Read Start Address		Don't care
Page Direction		Don't care
Interrupt during page read operation	1	Enabled

Notes:

1. An interrupt is output when  $SC-\overline{CE}_1 = \text{High}$  or in case  $A_3$  or a higher address changes.
2. Page Length:  
8 words is supported as the page lengths.

Page-Corresponding Addresses:

The page read-enabled addresses are  $A_2, A_1,$  and  $A_0$ . Fix addresses other than  $A_2, A_1,$  and  $A_0$  during page read operation.

Page Start Address:

Since random page read is supported, any address ( $A_2, A_1, A_0$ ) can be used as the page read start address.

Page Direction:

Since random page read is possible, there is not restriction on the page direction.

Interrupt during Page Read Operation:

When generating an interrupt during page read, either make  $SC-\overline{CE}_1$  high level or change  $A_3$  and higher addresses.

When page read is not used:

Since random page read is supported, even when not using page read, random access is possible as usual.

## 8.6 Mode Register Settings

The sleep mode can be set using the mode register. Since the initial value of the mode register at power application is undefined, be sure to set the mode register after initialization at power application. However, since sleep mode is not entered unless  $CE_2 = \text{Low}$  when sleep mode is not used, it is not necessary to set the mode register. Moreover, when using page read without using sleep mode, it is not necessary to set the mode register.

### 8.6.1 Mode Register Setting Method

The mode register setting mode can be entered by successively writing two specific data after two continuous reads of the highest address (1FFFFFFH). The mode register setting is a continuous four-cycle operation (two read cycles and two write cycles).

Commands are written to the command register. The command register is used to latch the addresses and data required for executing commands, and it does not have an exclusive memory area.

For the timing chart and flow chart, refer to Mode Register Setting Timing Chart (P.72), Mode Register Setting Flow Chart (P.73).

Following table shows the commands and command sequences.

#### Command Sequence

Command Sequence	1st Bus Cycle (Read Cycle)		2nd Bus Cycle (Read Cycle)		3rd Bus Cycle (Write Cycle)		4th Bus Cycle (Write Cycle)	
	Address	Data	Address	Data	Address	Data	Address	Data
Sleep Mode	1FFFFFFH	-	1FFFFFFH	-	1FFFFFFH	00H	1FFFFFFH	07H

#### 4th Bus Cycle (Write cycle)

DQ	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Mode Register Setting	0	0	0	0	0	0	0	0	0	0	0	0	0	PL	1	1

Page Length	1	8 words
-------------	---	---------

### 8.6.2 Cautions for Setting Mode Register

Since, for the mode register setting, the internal counter status is judged by toggling  $SC-\overline{CE}_1$  and  $S-\overline{OE}$ , toggle  $SC-\overline{CE}_1$  at every cycle during entry (read cycle twice, write cycle twice), and toggle  $S-\overline{OE}$  like  $SC-\overline{CE}_1$  at the first and second read cycles.

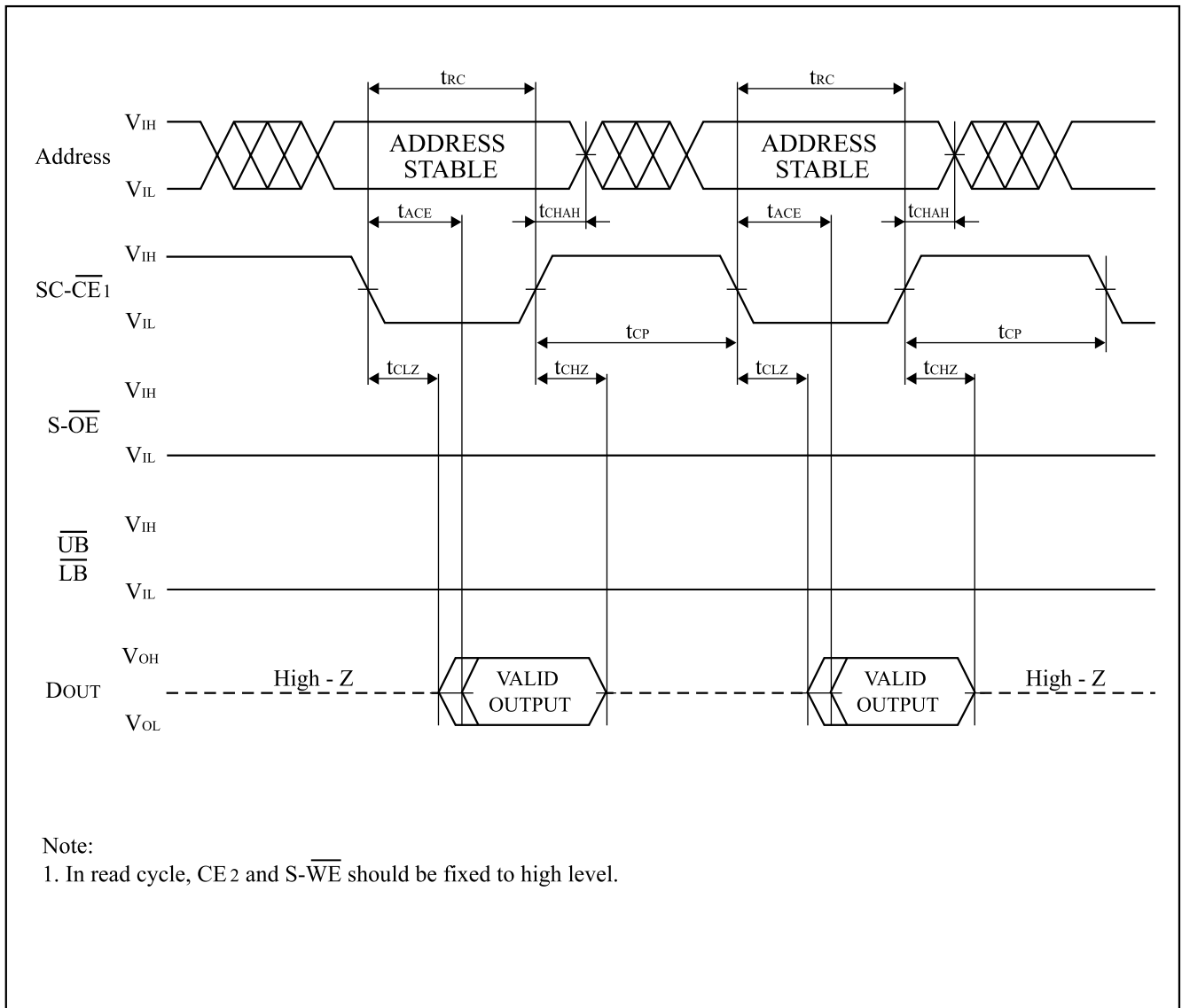
If incorrect addresses or data are written, or if addresses or data are written in the incorrect order, the setting of the mode register are not performed correctly.

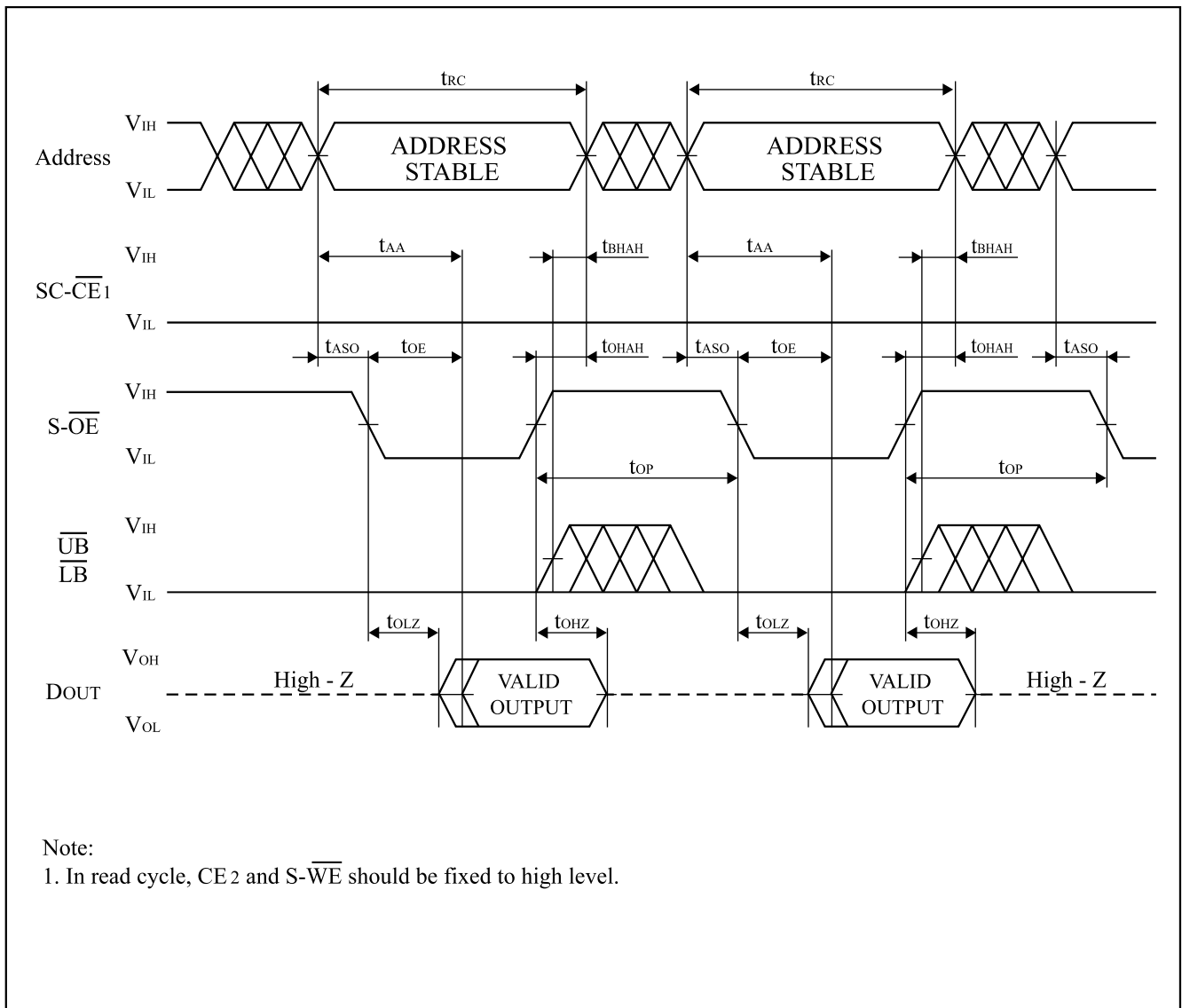
When the highest address (1FFFFFFH) is read consecutively three or more times, the mode register setting entries are cancelled.

Once the sleep mode has been set in the mode register, these settings are retained until they are set again, while applying the power supply. However, the mode register setting will become undefined if the power is turned off, so set the mode register again after power application.

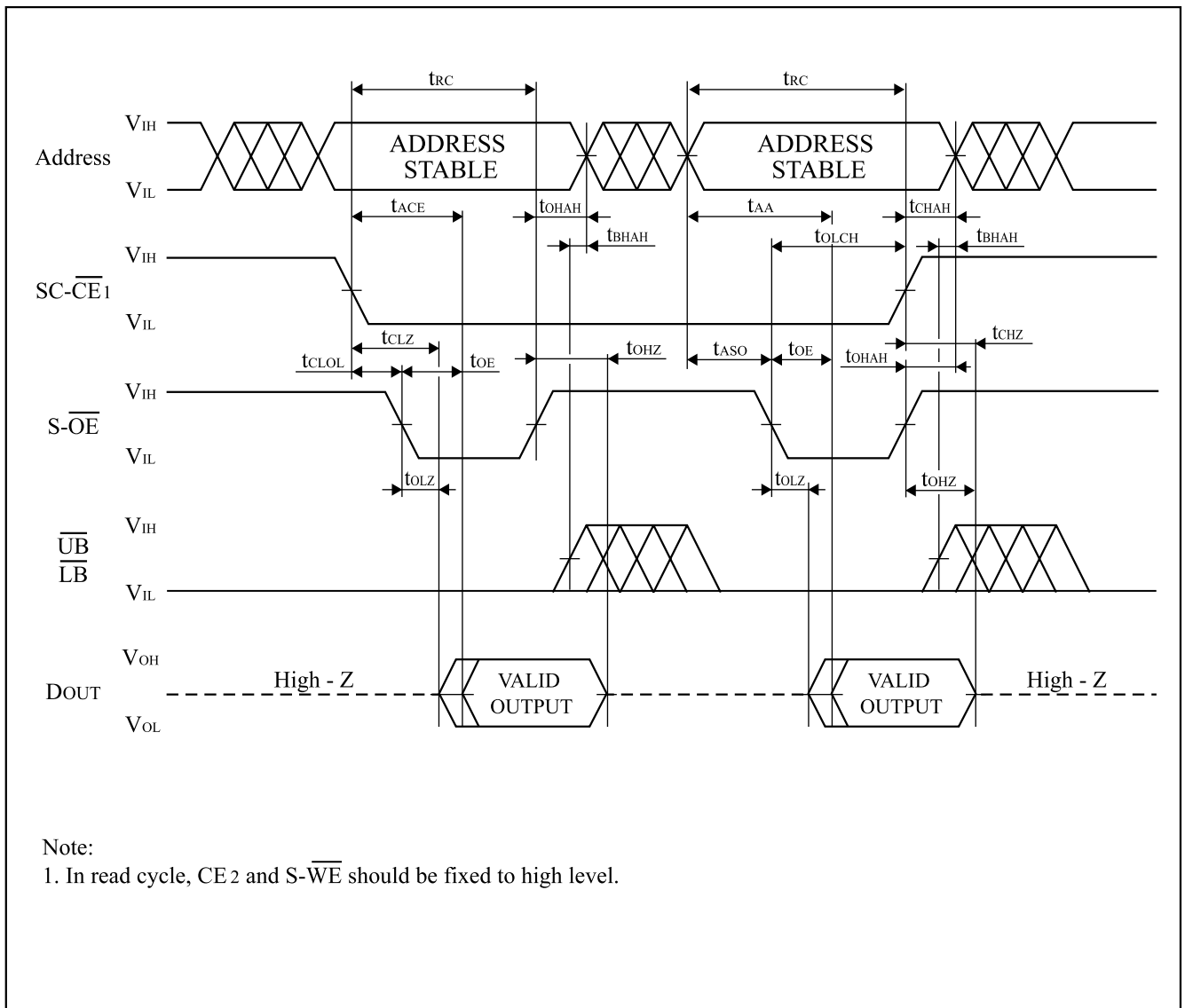
For the timing chart and flow chart, refer to Mode Register Setting Timing Chart (P.72), Mode Register Setting Flow Chart (P.73).

## 8.7 Smartcombo RAM AC Characteristics Timing Chart

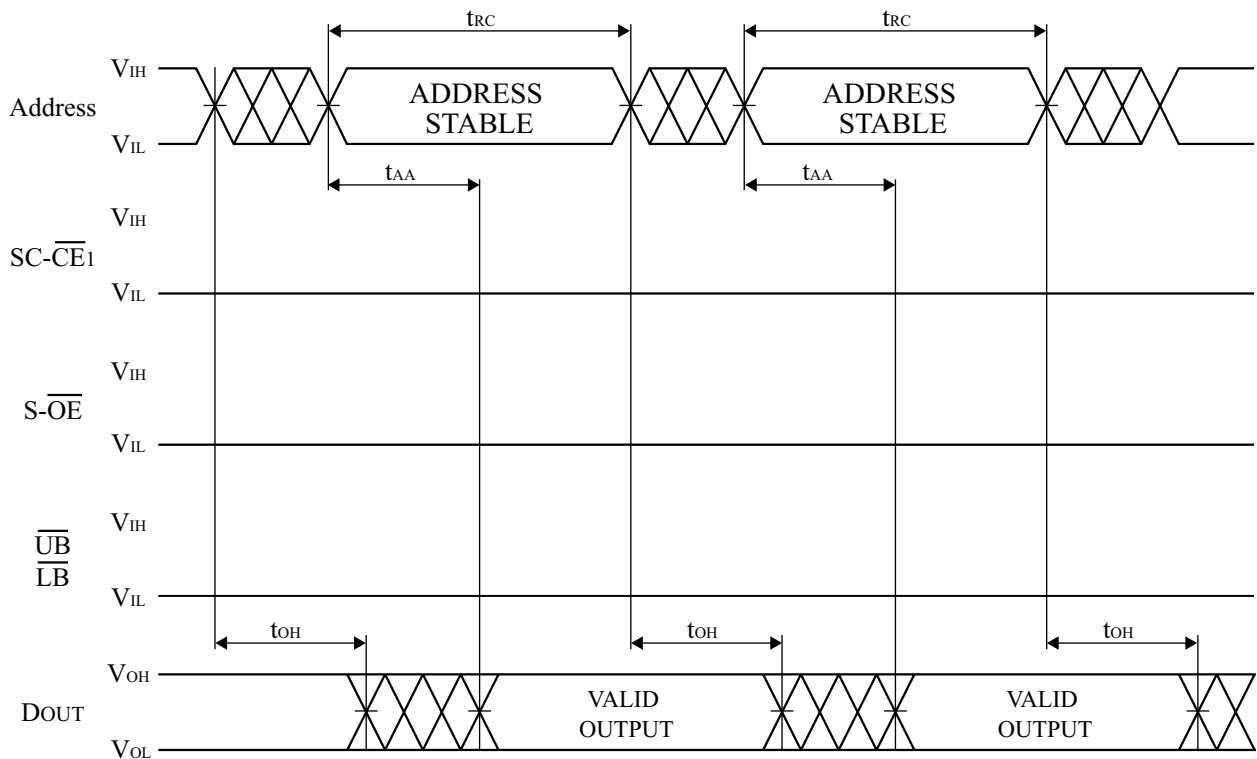
Read Cycle Timing Chart 1 (SC- $\overline{\text{CE}}_1$  Controlled)

Read Cycle Timing Chart 2 (S- $\overline{\text{OE}}$  Controlled)



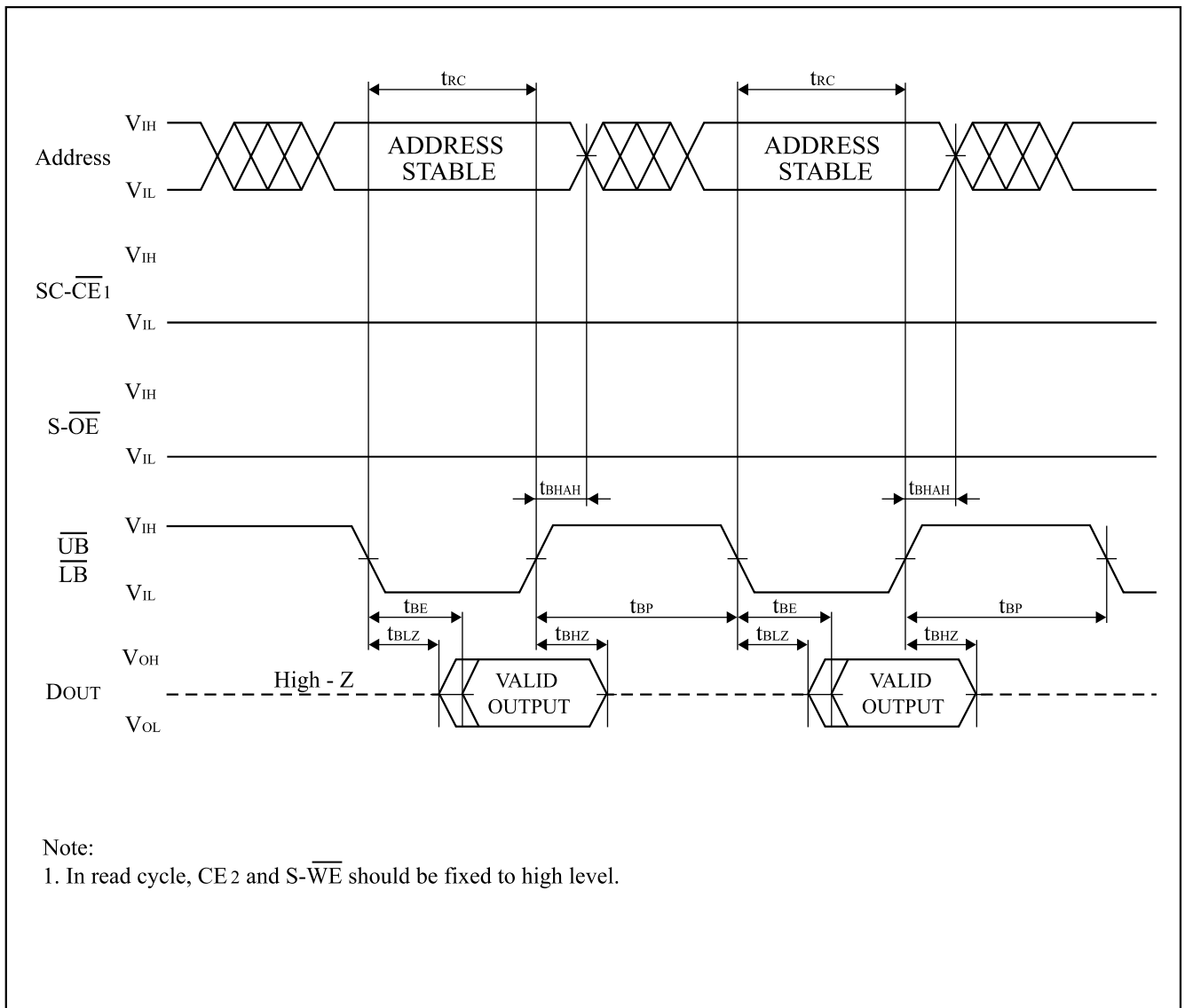
Read Cycle Timing Chart 3 (SC- $\overline{CE1}$  / S- $\overline{OE}$  Controlled)

Read Cycle Timing Chart 4 (Address Controlled)



## Notes:

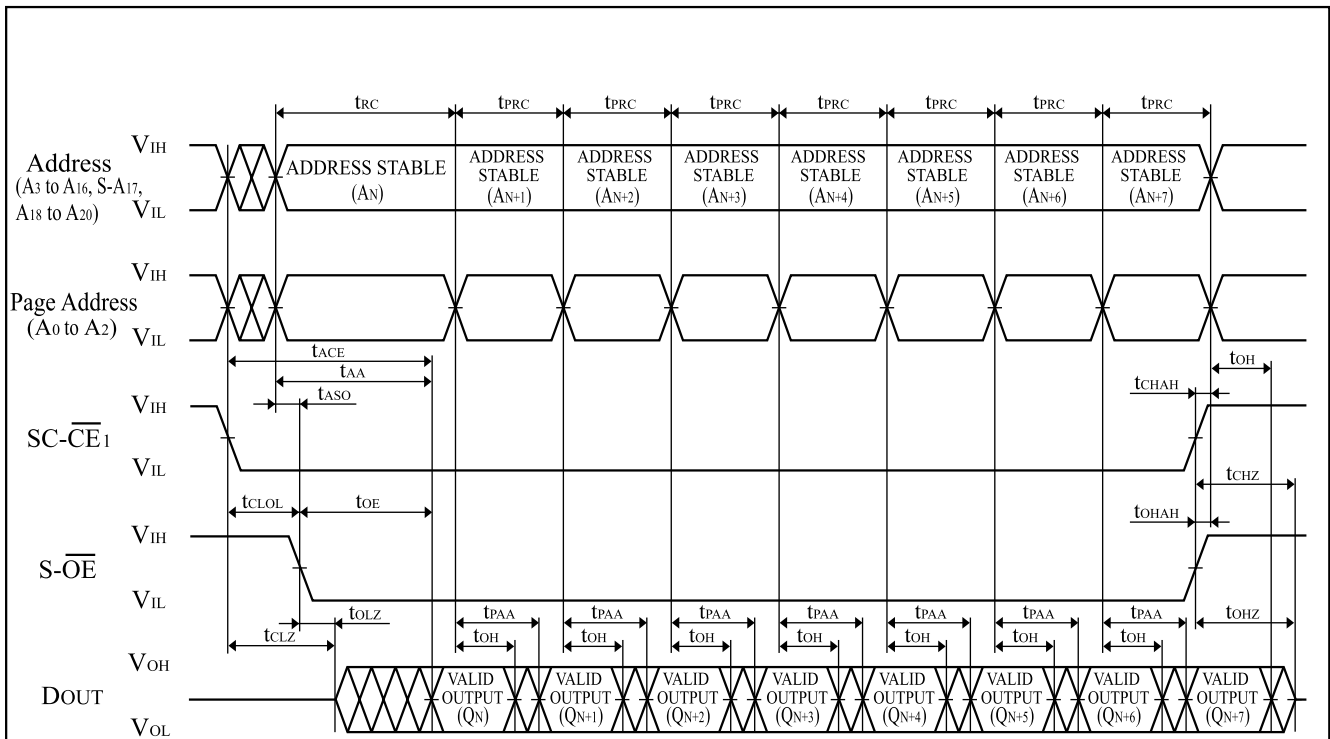
1. In read cycle,  $CE2$  and  $S-\overline{WE}$  should be fixed to high level.
2. When read cycle time is less than  $t_{RC}$  (Min.), the address access time ( $t_{AA}$ ) is not guaranteed.

Read Cycle Timing Chart 5 ( $\overline{\text{LB}}/\overline{\text{UB}}$  Controlled)

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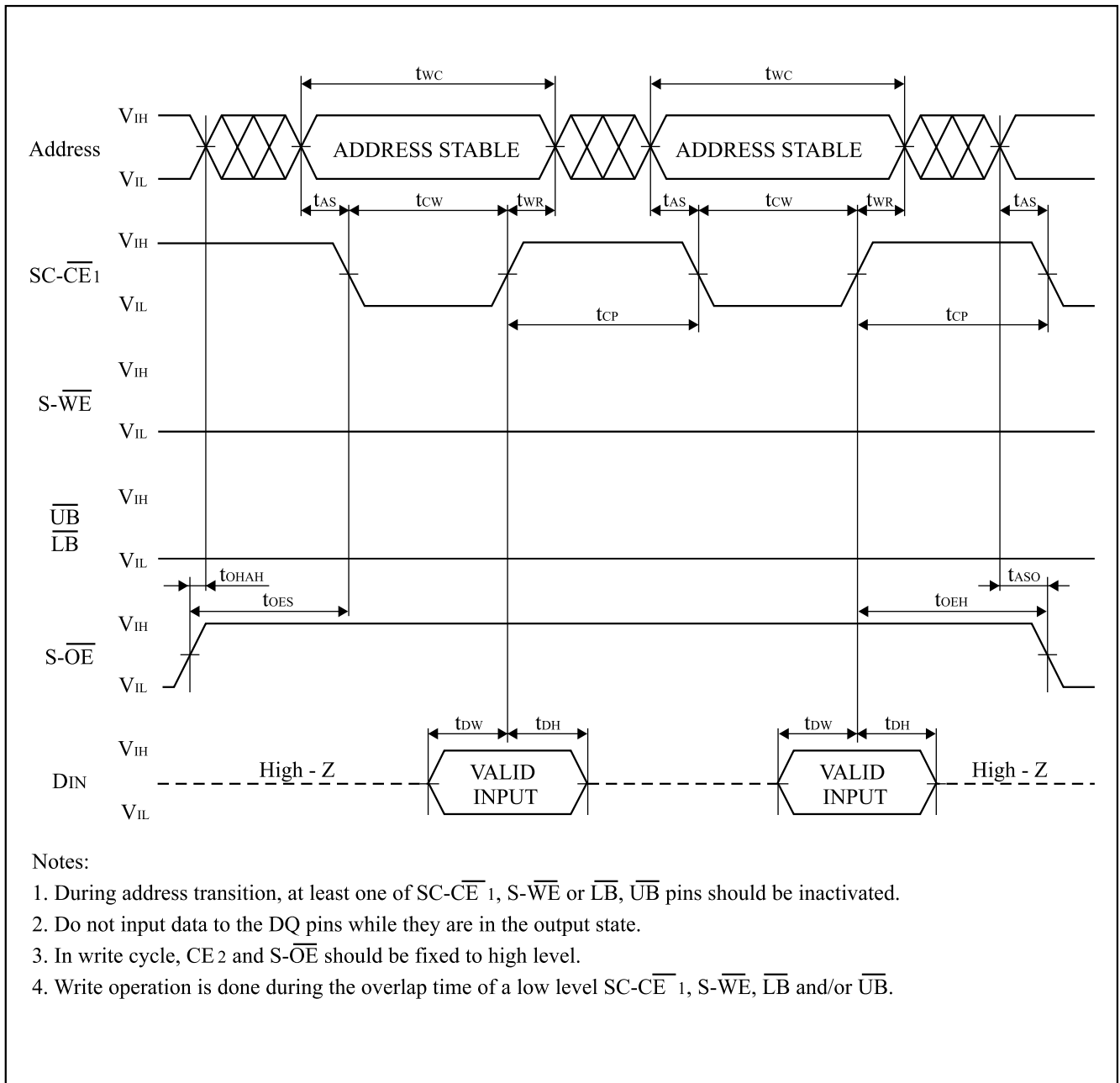
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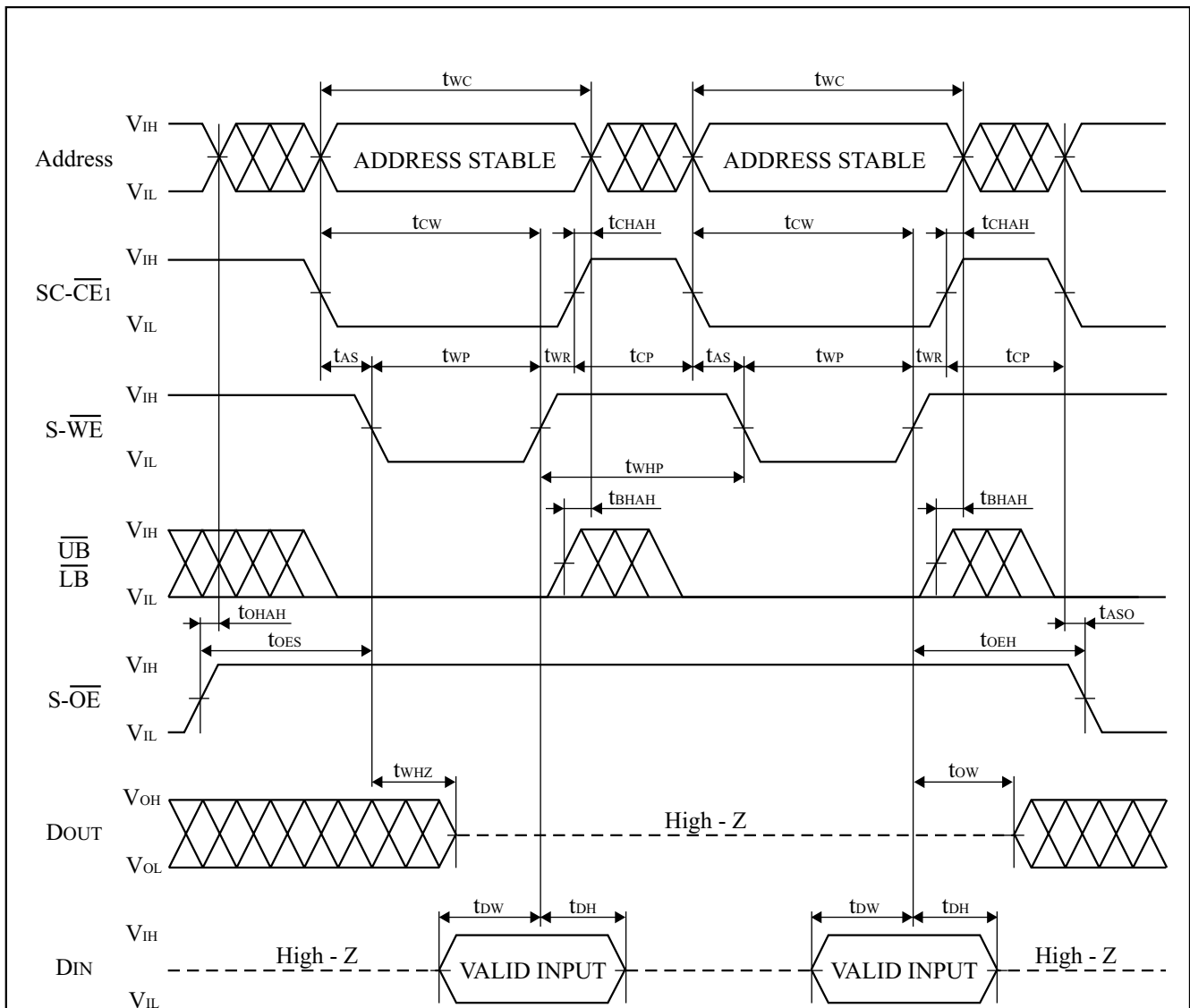
## 8 Word Page Read Cycle Timing Chart



## Notes:

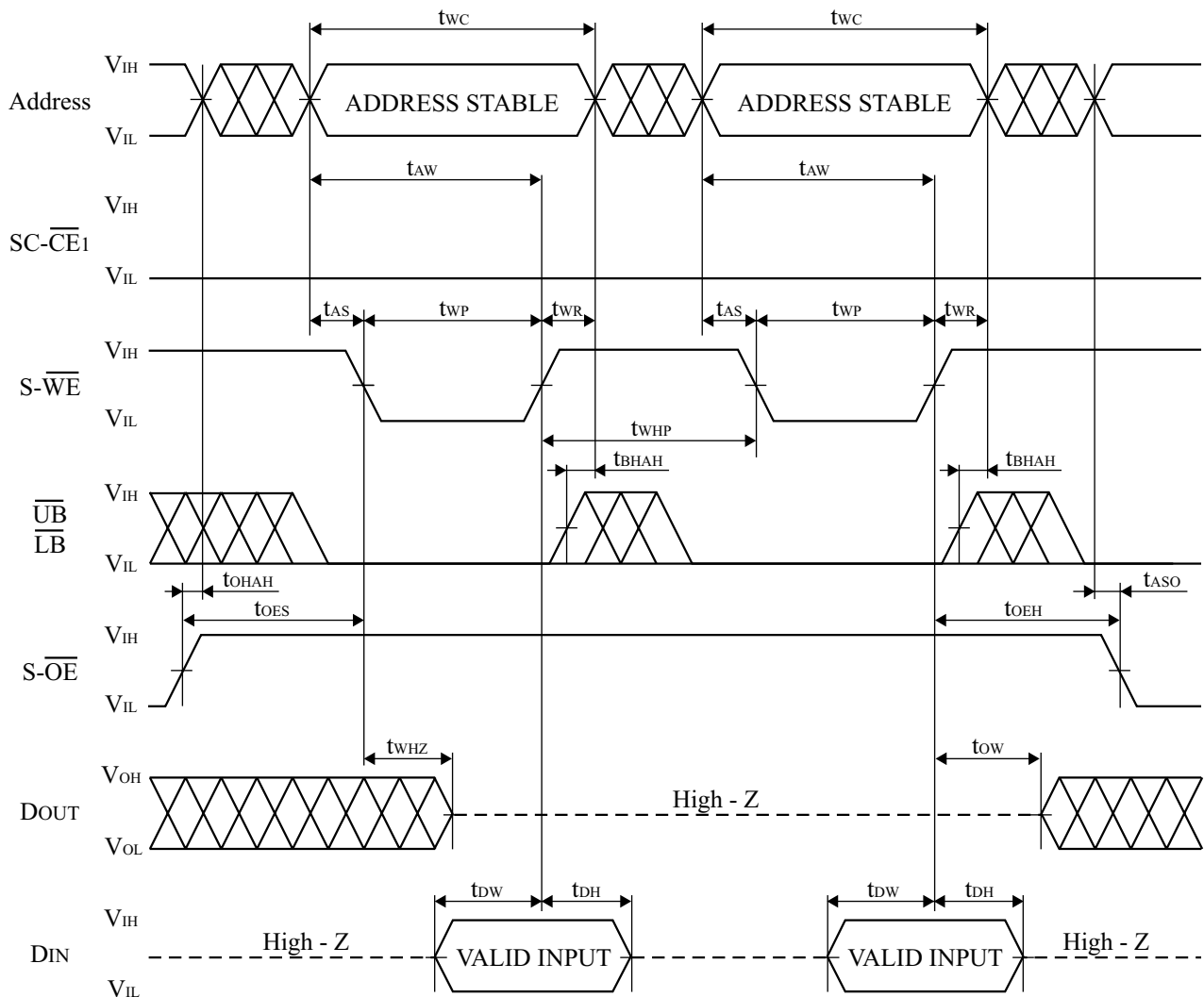
1. In read cycle,  $\overline{CE}_2$  and S- $\overline{WE}$  should be fixed to high level.
2.  $\overline{LB}$  and  $\overline{UB}$  are Low level.

Write Cycle Timing Chart 1 (SC- $\overline{CE1}$  Controlled)

Write Cycle Timing Chart 2 (S- $\overline{\text{WE}}$  Controlled)

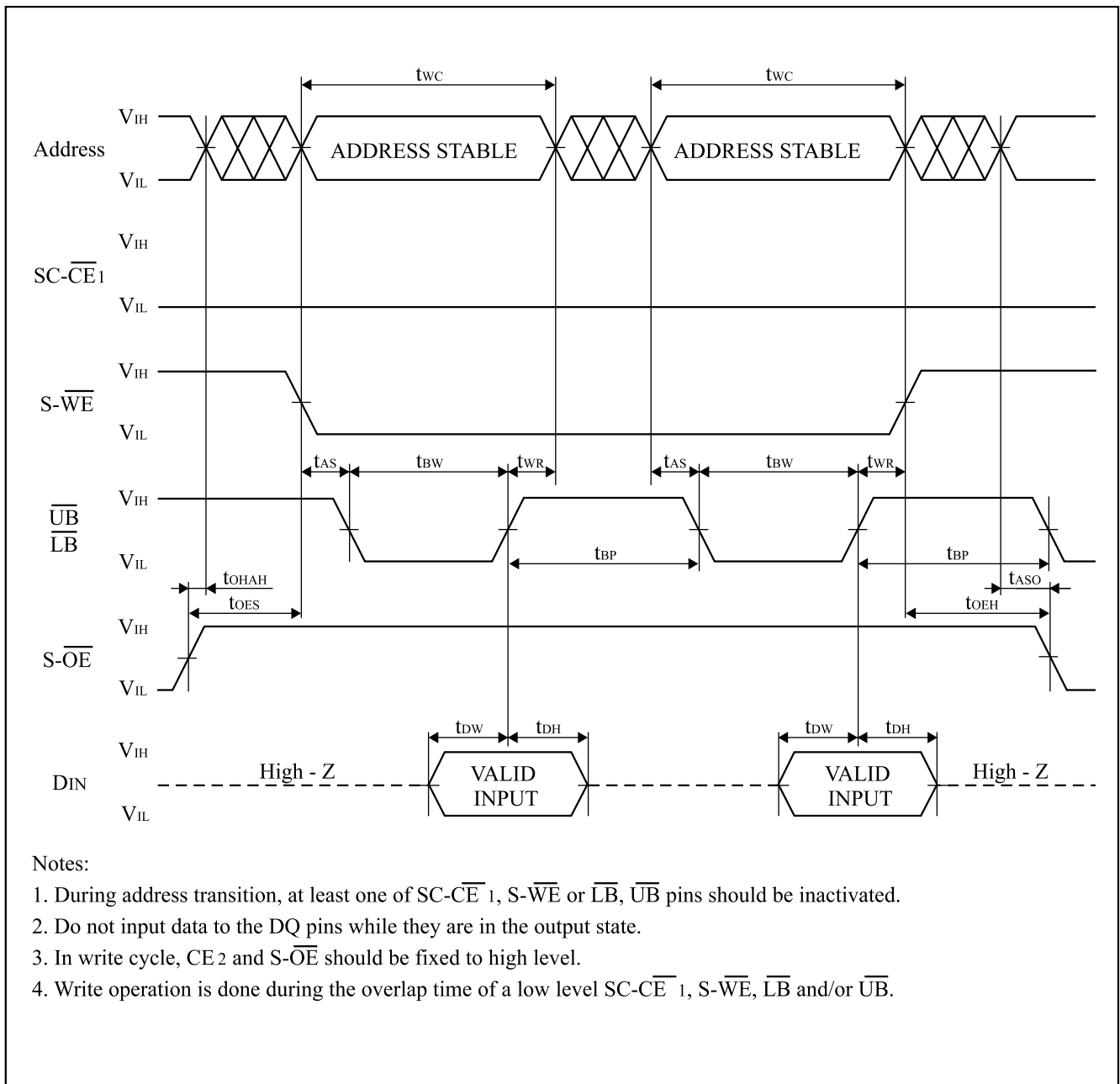
## Notes:

1. During address transition, at least one of SC- $\overline{\text{CE}}1$ , S- $\overline{\text{WE}}$  or  $\overline{\text{LB}}$ ,  $\overline{\text{UB}}$  pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
3. In write cycle, CE2 and S- $\overline{\text{OE}}$  should be fixed to high level.
4. Write operation is done during the overlap time of a low level SC- $\overline{\text{CE}}1$ , S- $\overline{\text{WE}}$ ,  $\overline{\text{LB}}$  and/or  $\overline{\text{UB}}$ .

Write Cycle Timing Chart 3 (S- $\overline{WE}$  Controlled)

## Notes:

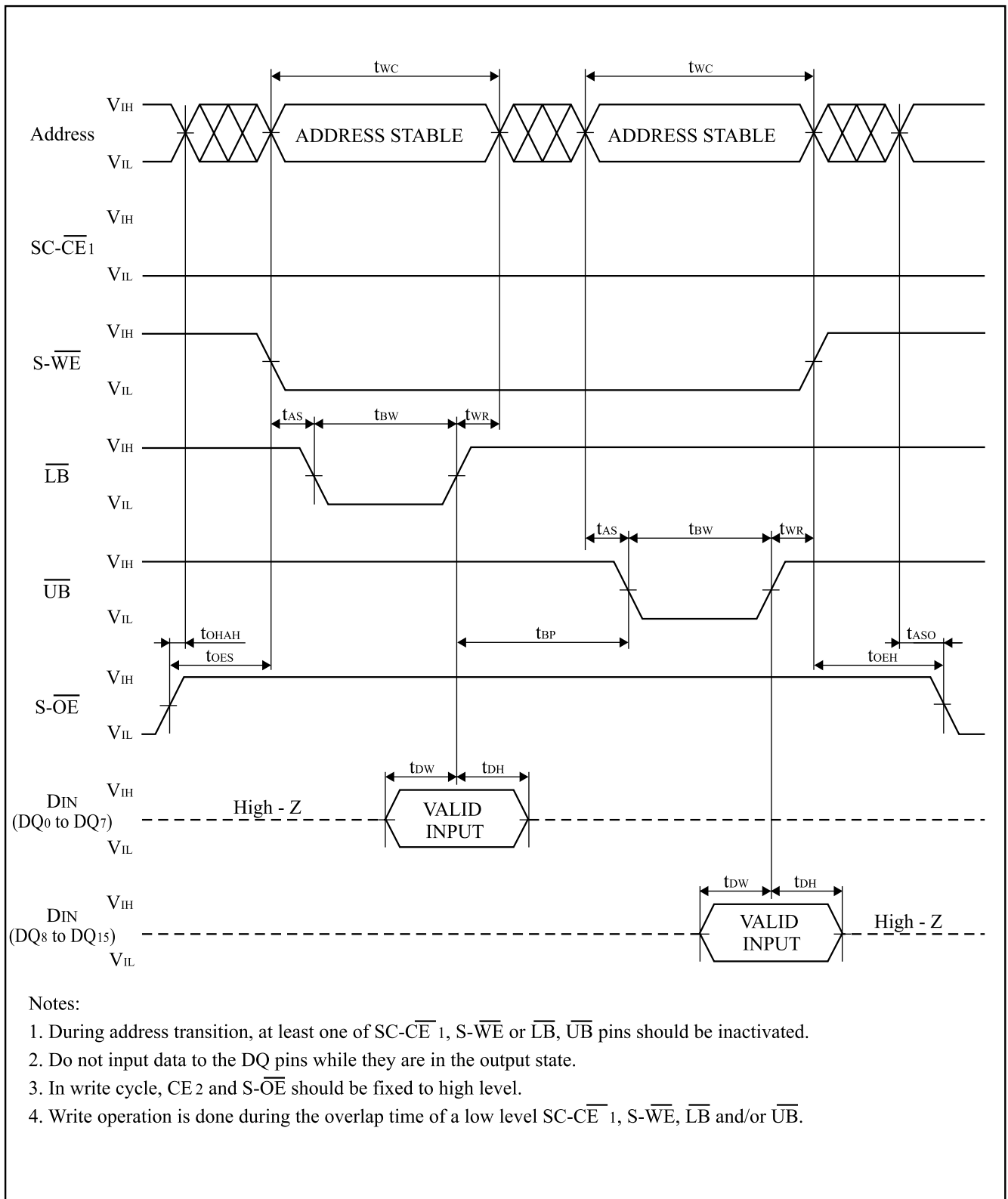
1. During address transition, at least one of SC- $\overline{CE1}$ , S- $\overline{WE}$  or  $\overline{LB}$ ,  $\overline{UB}$  pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
3. In write cycle, CE2 and S- $\overline{OE}$  should be fixed to high level.
4. Write operation is done during the overlap time of a low level SC- $\overline{CE1}$ , S- $\overline{WE}$ ,  $\overline{LB}$  and/or  $\overline{UB}$ .

Write Cycle Timing Chart 4 ( $\overline{\text{LB}} / \overline{\text{UB}}$  Controlled)

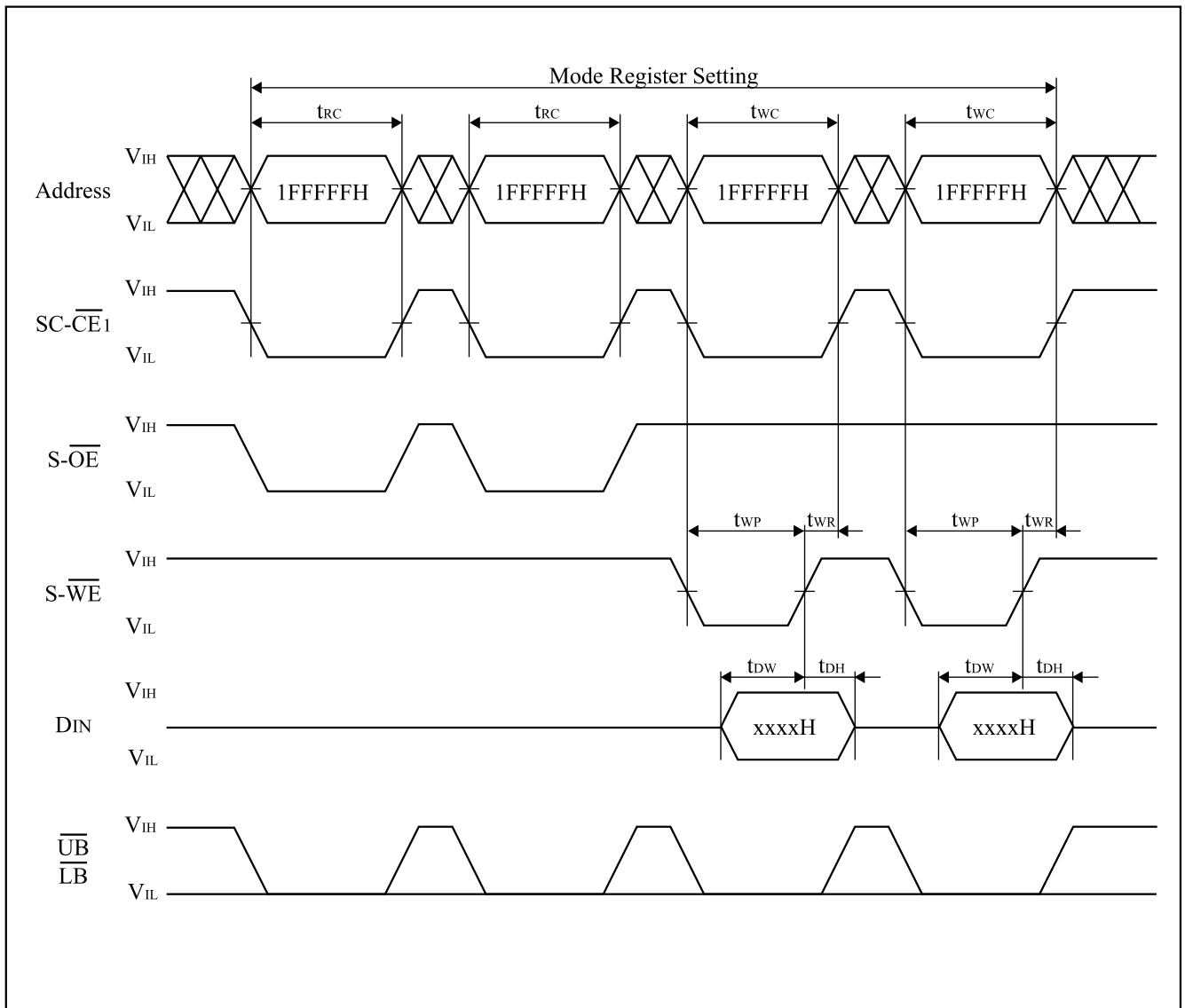
## Notes:

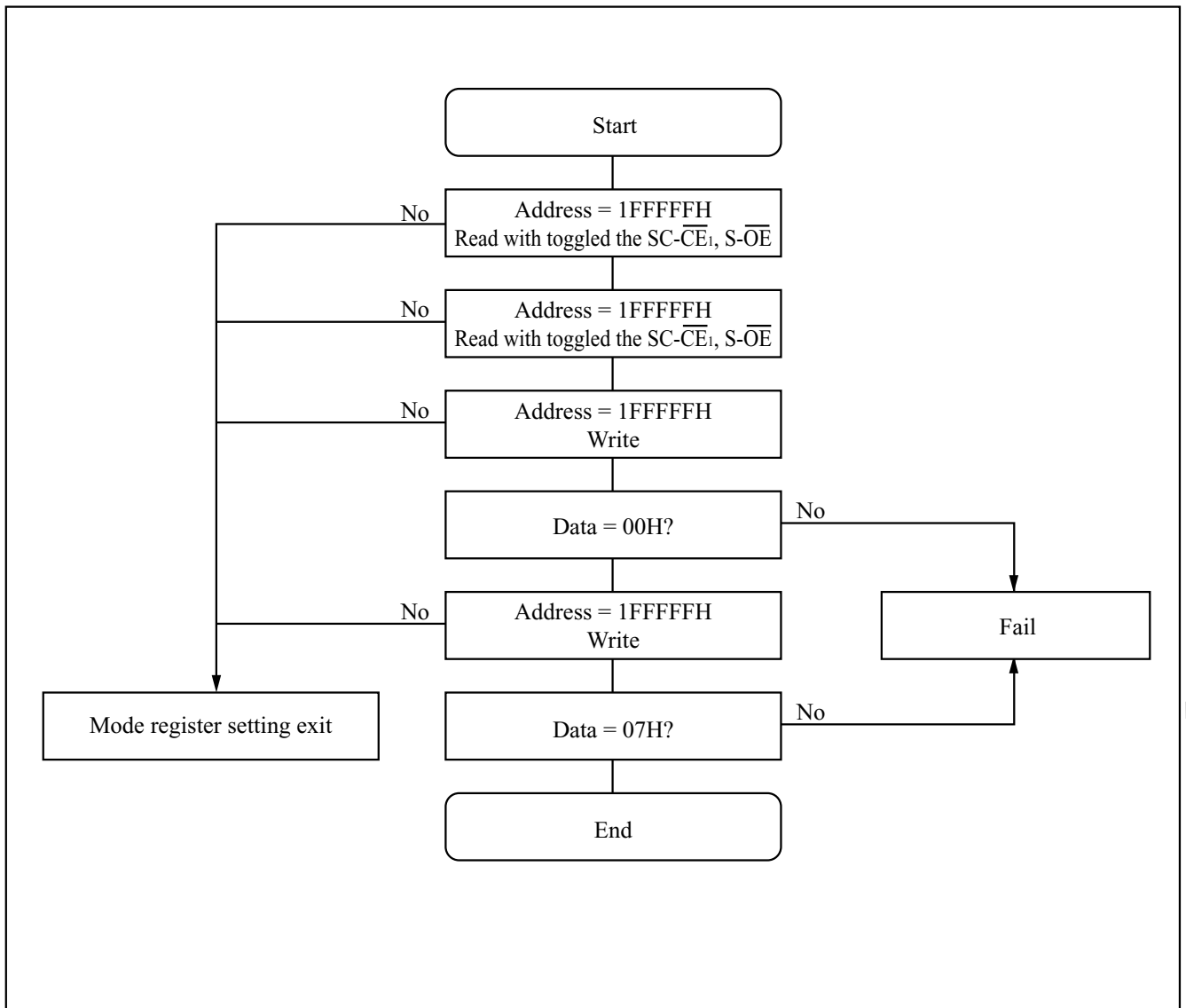
1. During address transition, at least one of  $\overline{\text{SC-CE}}_1$ ,  $\overline{\text{S-WE}}$  or  $\overline{\text{LB}}$ ,  $\overline{\text{UB}}$  pins should be inactivated.
2. Do not input data to the DQ pins while they are in the output state.
3. In write cycle,  $\overline{\text{CE}}_2$  and  $\overline{\text{S-OE}}$  should be fixed to high level.
4. Write operation is done during the overlap time of a low level  $\overline{\text{SC-CE}}_1$ ,  $\overline{\text{S-WE}}$ ,  $\overline{\text{LB}}$  and/or  $\overline{\text{UB}}$ .



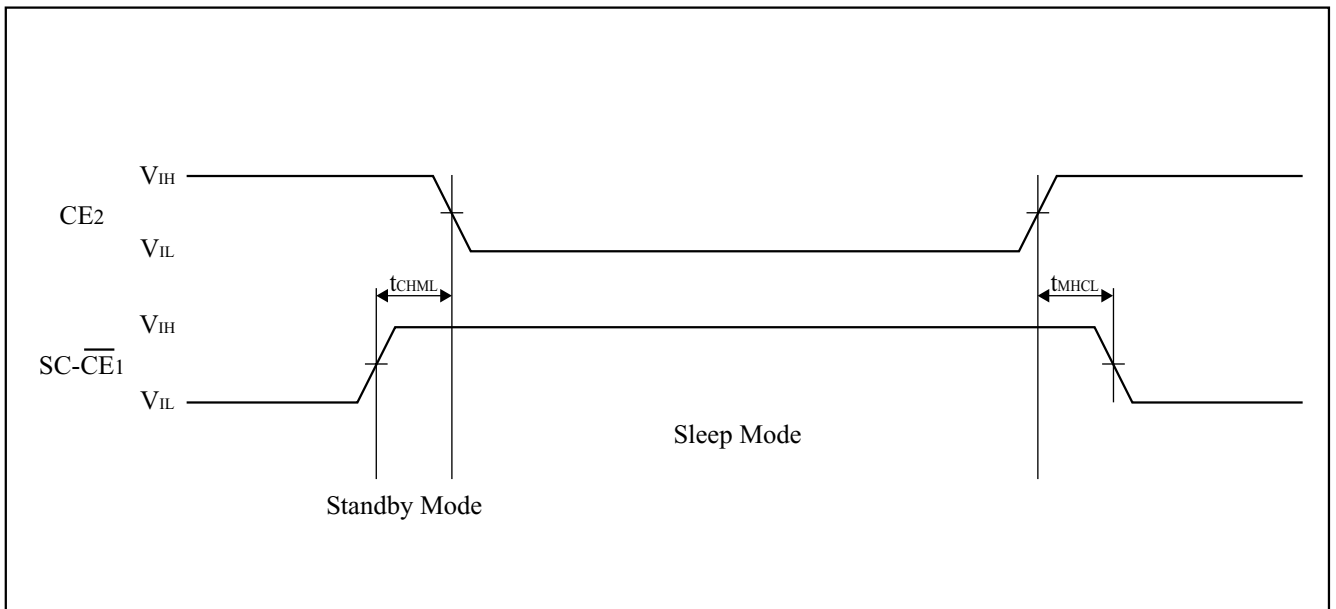
Write Cycle Timing Chart 5 ( $\overline{\text{LB}} / \overline{\text{UB}}$  Independent Controlled)

### Mode Register Setting Timing Chart



Mode Register Setting Flow Chart

Sleep Mode Entry / Exit Timing Chart



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## 9. SRAM

## 9.1 Truth Table

9.1.1 Bus Operation <sup>(1)</sup>

SRAM	Notes	S- $\overline{CE}_1$	CE <sub>2</sub>	S- $\overline{OE}$	S- $\overline{WE}$	$\overline{LB}$	$\overline{UB}$	DQ <sub>0</sub> to DQ <sub>15</sub>
Read		L	H	L	H	(2)		(2)
Output Disable				H	H	X	X	High - Z
Write				X	L	(2)		(2)
Standby		H	X	X	X	X	X	High - Z
		X	L			X	X	
		X	X			H	H	

Notes:

1. L = V<sub>IL</sub>, H = V<sub>IH</sub>, X = H or L, High-Z = High impedance. Refer to the DC Characteristics.2.  $\overline{LB}$ ,  $\overline{UB}$  Control Mode

$\overline{LB}$	$\overline{UB}$	DQ <sub>0</sub> to DQ <sub>7</sub>	DQ <sub>8</sub> to DQ <sub>15</sub>
L	L	D <sub>OUT</sub> /D <sub>IN</sub>	D <sub>OUT</sub> /D <sub>IN</sub>
L	H	D <sub>OUT</sub> /D <sub>IN</sub>	High - Z
H	L	High - Z	D <sub>OUT</sub> /D <sub>IN</sub>

## 9.2 DC Electrical Characteristics for SRAM

## DC Electrical Characteristics

(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Typ.	Max.	Unit	Test Conditions
C <sub>IN</sub>	Input Capacitance	1			8	pF	V <sub>IN</sub> = 0V, f = 1MHz, T <sub>A</sub> = 25°C
C <sub>IO</sub>	I/O Capacitance	1			10	pF	V <sub>I/O</sub> = 0V, f = 1MHz, T <sub>A</sub> = 25°C
I <sub>LI</sub>	Input Leakage Current				±1	μA	V <sub>IN</sub> = V <sub>CC</sub> or GND
I <sub>LO</sub>	Output Leakage Current				±1	μA	V <sub>OUT</sub> = V <sub>CC</sub> or GND
I <sub>SB</sub>	V <sub>CC</sub> Standby Current				25	μA	S- $\overline{\text{CE}}_1$ , CE <sub>2</sub> ≥ V <sub>CC</sub> - 0.2V or CE <sub>2</sub> ≤ 0.2V
I <sub>CC1</sub>	V <sub>CC</sub> Operation Current				45	mA	S- $\overline{\text{CE}}_1$ = V <sub>IL</sub> , CE <sub>2</sub> = V <sub>IH</sub> , V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> t <sub>CYCLE</sub> = Min. I <sub>I/O</sub> = 0mA
I <sub>CC2</sub>	V <sub>CC</sub> Operation Current				8	mA	S- $\overline{\text{CE}}_1$ ≤ 0.2V, CE <sub>2</sub> ≥ V <sub>CC</sub> - 0.2V, V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or ≤ 0.2V t <sub>CYCLE</sub> = 1μs I <sub>I/O</sub> = 0mA
V <sub>IL</sub>	Input Low Voltage	1	-0.3		0.4	V	
V <sub>IH</sub>	Input High Voltage	1	V <sub>CC</sub> -0.4		V <sub>CC</sub> +0.3	V	
V <sub>OL</sub>	Output Low Voltage	1			0.2V <sub>CC</sub>	V	I <sub>OL</sub> = 0.5mA
V <sub>OH</sub>	Output High Voltage	1	2.2			V	I <sub>OH</sub> = -0.5mA

Note:

1. Sampled, not 100% tested.

### 9.3 AC Electrical Characteristics for SRAM

#### 9.3.1 AC Test Conditions

Input Pulse Level	0.4 V to 2.2 V
Input Rise and Fall Time	5 ns
Input and Output Timing Ref. Level	1.5 V
Output Load	1TTL + C <sub>L</sub> (30pF) <sup>(1)</sup>

Note:

- Including scope and socket capacitance.

#### 9.3.2 Read Cycle

(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

Symbol	Parameter	Notes	Min.	Max.	Unit
t <sub>RC</sub>	Read Cycle Time		65		ns
t <sub>AA</sub>	Address Access Time			65	ns
t <sub>ACE1</sub>	Chip Enable Access Time (S- $\overline{\text{CE}}_1$ )			65	ns
t <sub>ACE2</sub>	Chip Enable Access Time (CE <sub>2</sub> )			65	ns
t <sub>BE</sub>	Byte Enable Access Time			65	ns
t <sub>OE</sub>	Output Enable to Output Valid			40	ns
t <sub>OH</sub>	Output Hold from Address Change		10		ns
t <sub>LZ1</sub>	S- $\overline{\text{CE}}_1$ Low to Output Active	1	10		ns
t <sub>LZ2</sub>	CE <sub>2</sub> High to Output Active	1	10		ns
t <sub>OLZ</sub>	S- $\overline{\text{OE}}$ Low to Output Active	1	5		ns
t <sub>BLZ</sub>	$\overline{\text{UB}}$ or $\overline{\text{LB}}$ Low to Output Active	1	10		ns
t <sub>HZ1</sub>	S- $\overline{\text{CE}}_1$ High to Output in High-Z	1, 2	0	25	ns
t <sub>HZ2</sub>	CE <sub>2</sub> Low to Output in High-Z	1, 2	0	25	ns
t <sub>OHZ</sub>	S- $\overline{\text{OE}}$ High to Output in High-Z	1, 2	0	25	ns
t <sub>BHZ</sub>	$\overline{\text{UB}}$ or $\overline{\text{LB}}$ High to Output in High-Z	1, 2	0	25	ns

Notes:

- Active output to High-Z and High-Z to output active tests specified for a  $\pm 200\text{mV}$  transition from steady state levels into the test load.
- The period from S- $\overline{\text{CE}}_1$  Rise,  $\overline{\text{UB}}$  Rise,  $\overline{\text{LB}}$  Rise S- $\overline{\text{OE}}$  Rise (CE<sub>2</sub>: Falling) to output buffer off is logically 10ns.

## 9.3.3 Write Cycle

(T<sub>A</sub> = -25°C to +85°C, V<sub>CC</sub> = 2.7V to 3.1V)

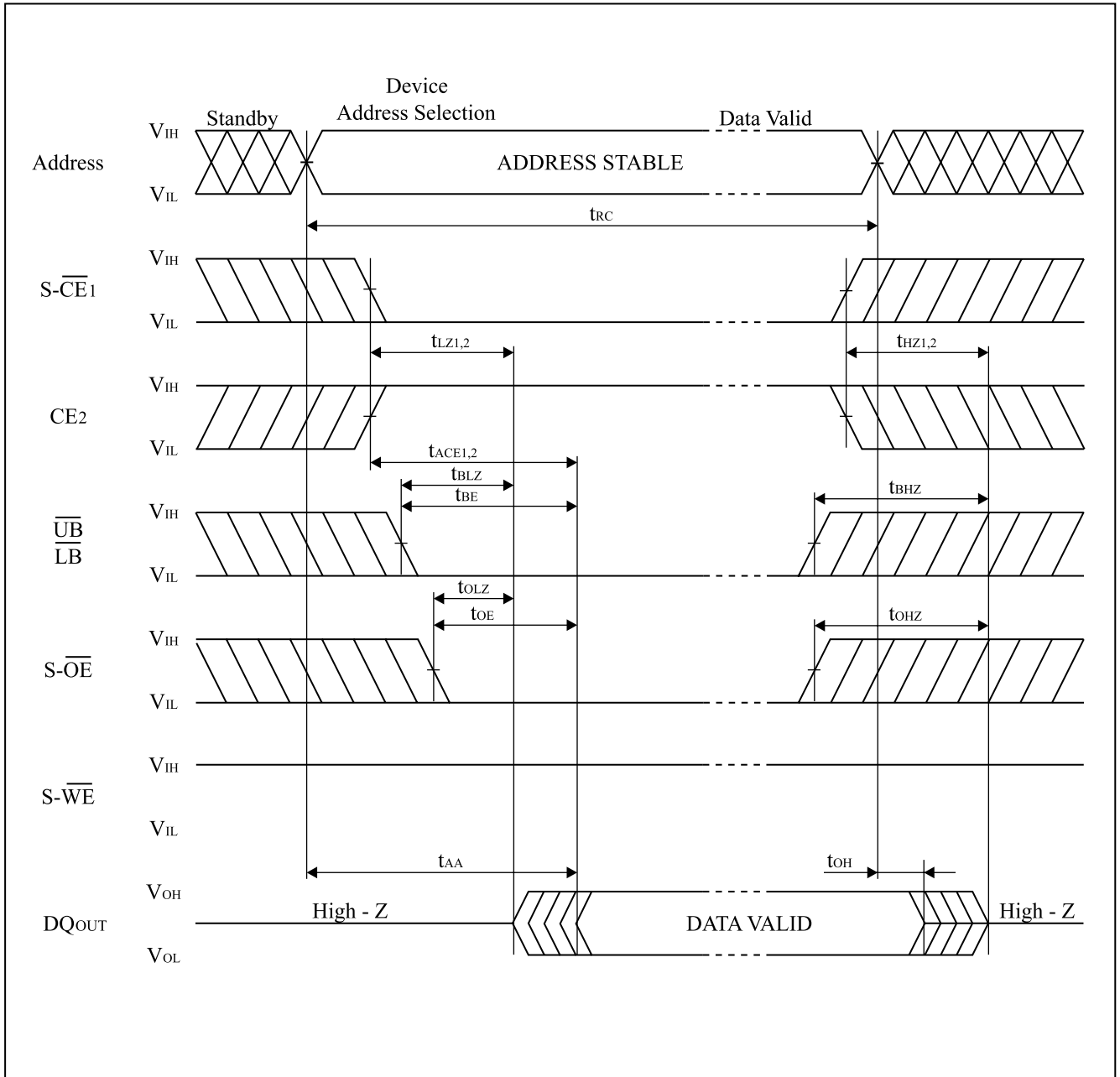
Symbol	Parameter	Notes	Min.	Max.	Unit
t <sub>WC</sub>	Write Cycle Time		65		ns
t <sub>CW</sub>	Chip Enable to End of Write		60		ns
t <sub>AW</sub>	Address Valid to End of Write		60		ns
t <sub>BW</sub>	Byte Select Time		60		ns
t <sub>AS</sub>	Address Setup Time		0		ns
t <sub>WP</sub>	Write Pulse Width		50		ns
t <sub>WR</sub>	Write Recovery Time		0		ns
t <sub>DW</sub>	Input Data Setup Time		30		ns
t <sub>DH</sub>	Input Data Hold Time		0		ns
t <sub>OW</sub>	S- $\overline{\text{WE}}$ High to Output Active	1	5		ns
t <sub>WZ</sub>	S- $\overline{\text{WE}}$ Low to Output in High-Z	1	0	25	ns

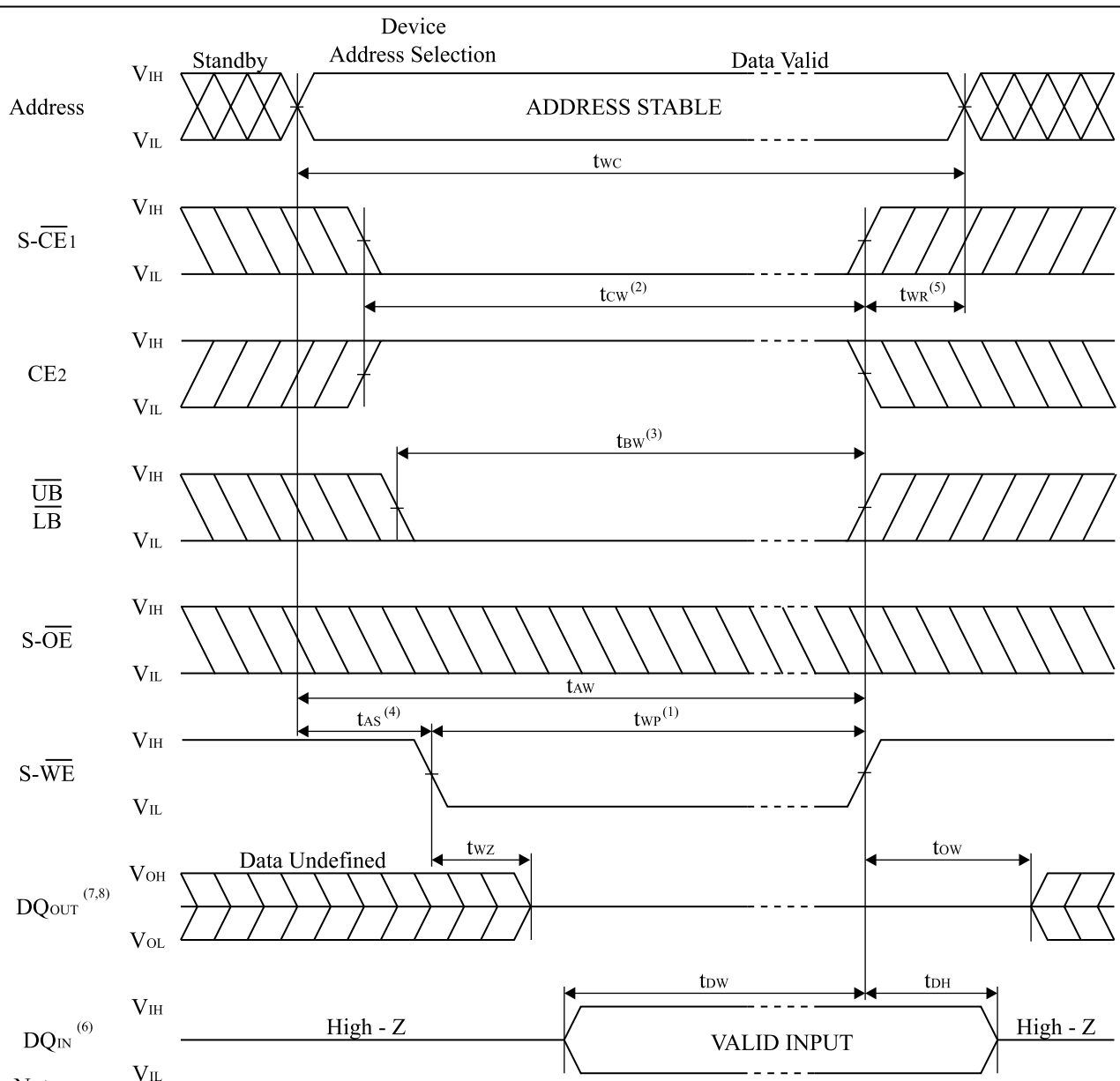
Note:

- Active output to High-Z and High-Z to output active tests specified for a  $\pm 200\text{mV}$  transition from steady state levels into the test load.



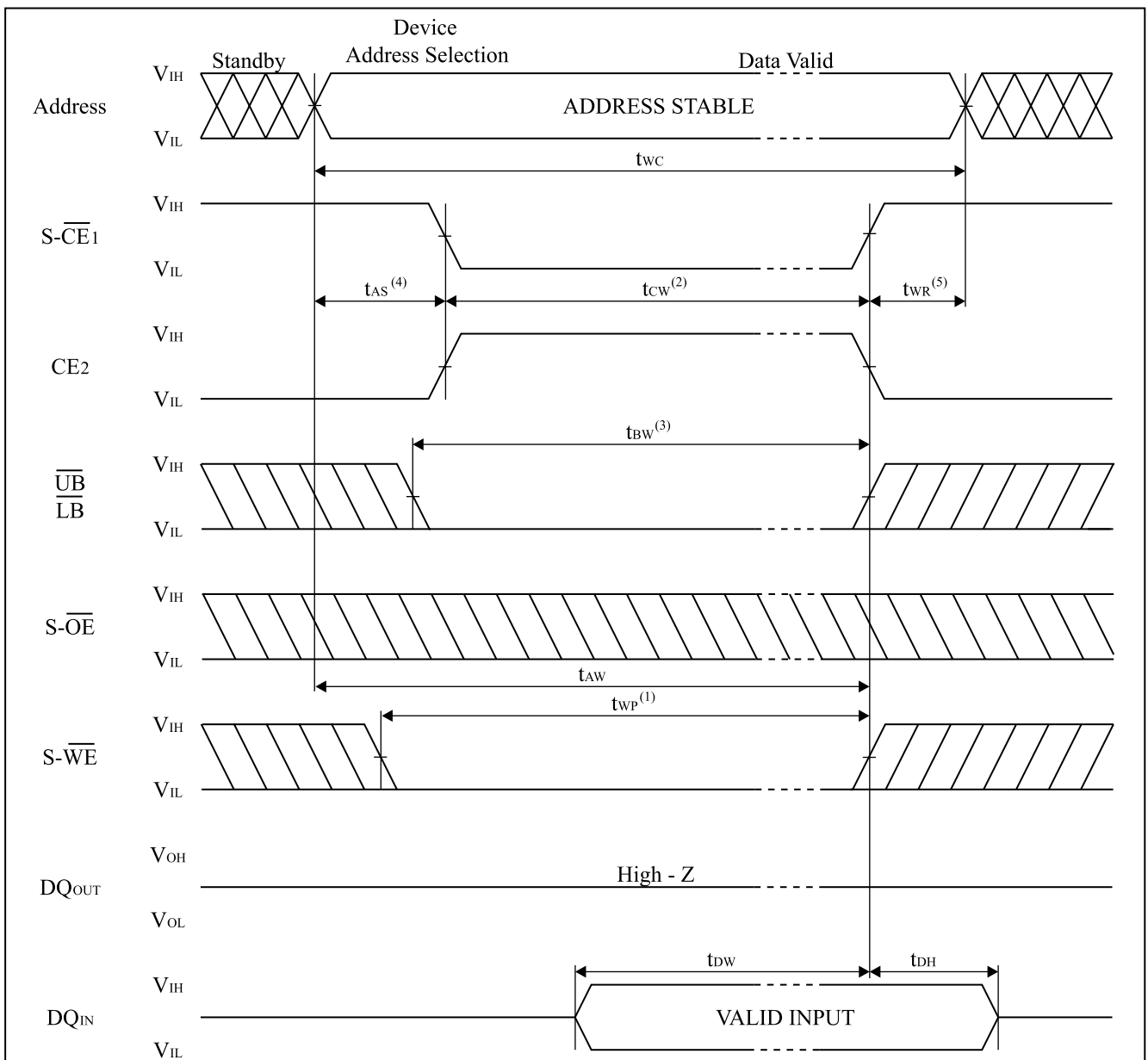
## 9.4 SRAM AC Characteristics Timing Chart

Read Cycle Timing Chart

Write Cycle Timing Chart (S- $\overline{\text{WE}}$  Controlled)

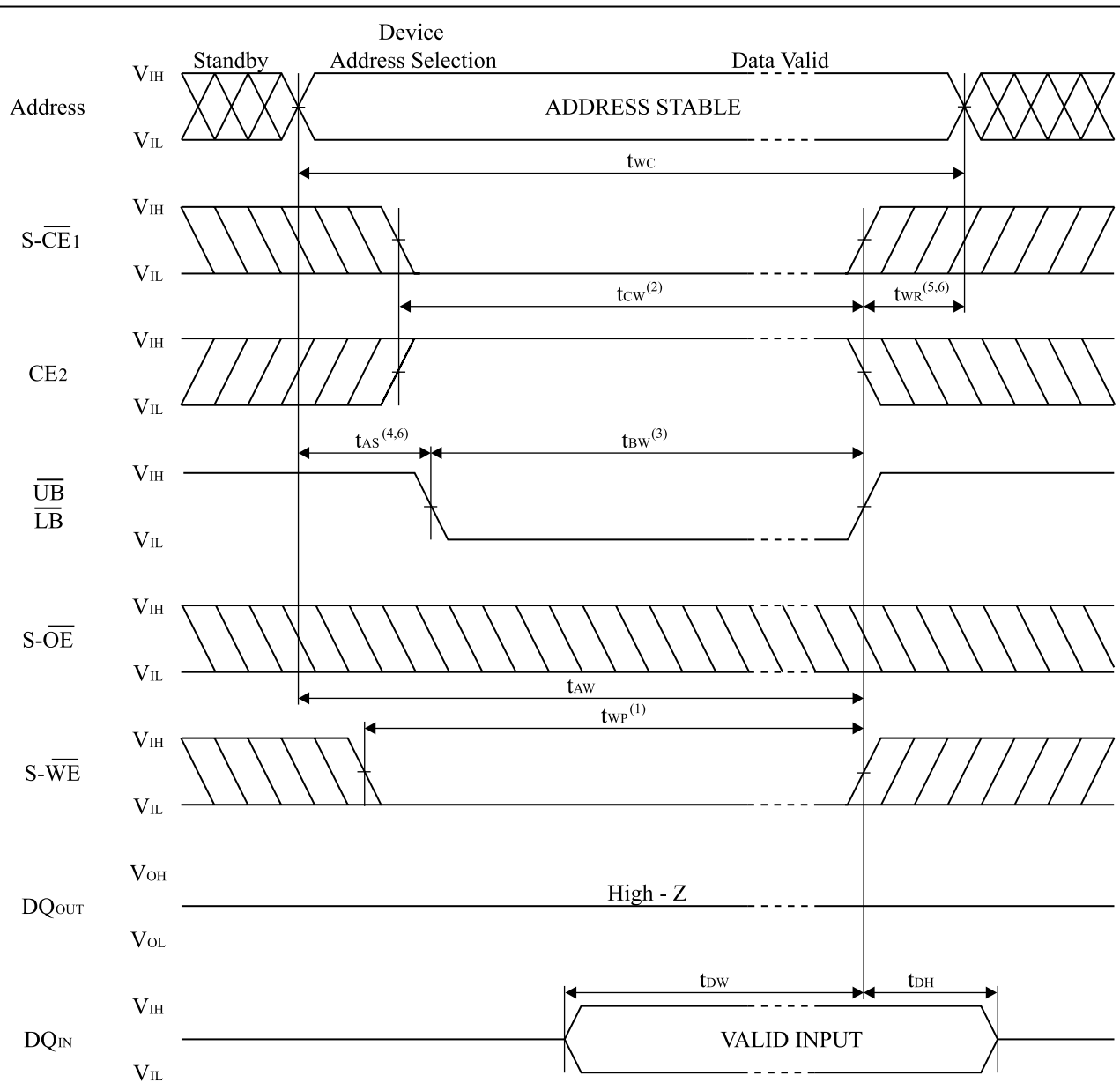
## Notes:

1. A write occurs during the overlap of a low S- $\overline{\text{CE}}$ <sub>1</sub>, a high CE<sub>2</sub> and a low S- $\overline{\text{WE}}$ .  
A write begins at the latest transition among S- $\overline{\text{CE}}$ <sub>1</sub> going low, CE<sub>2</sub> going high and S- $\overline{\text{WE}}$  going low.  
A write ends at the earliest transition among S- $\overline{\text{CE}}$ <sub>1</sub> going high, CE<sub>2</sub> going low and S- $\overline{\text{WE}}$  going high.  
 $t_{wp}^{(1)}$  is measured from the beginning of write to the end of write.
2.  $t_{cw}^{(2)}$  is measured from the later of S- $\overline{\text{CE}}$ <sub>1</sub> going low or CE<sub>2</sub> going high to the end of write.
3.  $t_{bw}^{(3)}$  is measured from the time of going low  $\overline{\text{UB}}$  or low  $\overline{\text{LB}}$  to the end of write.
4.  $t_{as}^{(4)}$  is measured from the address valid to beginning of write.
5.  $t_{wr}^{(5)}$  is measured from the end of write to the address change.  $t_{wr}^{(5)}$  applies in case a write ends at S- $\overline{\text{CE}}$ <sub>1</sub> going high, CE<sub>2</sub> going low or S- $\overline{\text{WE}}$  going high.
6. During this period DQ pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
7. If S- $\overline{\text{CE}}$ <sub>1</sub> goes low or CE<sub>2</sub> goes high simultaneously with S- $\overline{\text{WE}}$  going low or after S- $\overline{\text{WE}}$  going low, the outputs remain in high impedance state.
8. If S- $\overline{\text{CE}}$ <sub>1</sub> goes high or CE<sub>2</sub> goes low simultaneously with S- $\overline{\text{WE}}$  going high or before S- $\overline{\text{WE}}$  going high, the outputs remain in high impedance state.

Write Cycle Timing Chart (S- $\overline{\text{CE}}_1$  Controlled)

## Notes:

1. A write occurs during the overlap of a low S- $\overline{\text{CE}}_1$ , a high CE<sub>2</sub> and a low S- $\overline{\text{WE}}$ .  
A write begins at the latest transition among S- $\overline{\text{CE}}_1$  going low, CE<sub>2</sub> going high and S- $\overline{\text{WE}}$  going low.  
A write ends at the earliest transition among S- $\overline{\text{CE}}_1$  going high, CE<sub>2</sub> going low and S- $\overline{\text{WE}}$  going high.  
 $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the later of S- $\overline{\text{CE}}_1$  going low or CE<sub>2</sub> going high to the end of write.
3.  $t_{BW}$  is measured from the time of going low  $\overline{\text{UB}}$  or low  $\overline{\text{LB}}$  to the end of write.
4.  $t_{AS}$  is measured from the address valid to beginning of write.
5.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applies in case a write ends at S- $\overline{\text{CE}}_1$  going high, CE<sub>2</sub> going low or S- $\overline{\text{WE}}$  going high.

Write Cycle Timing Chart ( $\overline{UB} / \overline{LB}$  Controlled)

## Notes:

1. A write occurs during the overlap of a low S- $\overline{CE}_1$ , a high CE<sub>2</sub> and a low S- $\overline{WE}$ .  
A write begins at the latest transition among S- $\overline{CE}_1$  going low, CE<sub>2</sub> going high and S- $\overline{WE}$  going low.  
A write ends at the earliest transition among S- $\overline{CE}_1$  going high, CE<sub>2</sub> going low and S- $\overline{WE}$  going high.  
 $t_{WP}$  is measured from the beginning of write to the end of write.
2.  $t_{CW}$  is measured from the later of S- $\overline{CE}_1$  going low or CE<sub>2</sub> going high to the end of write.
3.  $t_{BW}$  is measured from the time of going low  $\overline{UB}$  or low  $\overline{LB}$  to the end of write.
4.  $t_{AS}$  is measured from the address valid to beginning of write.
5.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applies in case a write ends at S- $\overline{CE}_1$  going high, CE<sub>2</sub> going low or S- $\overline{WE}$  going high.
6.  $\overline{UB}$  and  $\overline{LB}$  need to make the time of start of a cycle, and an end "high" level for reservation of  $t_{AS}$  and  $t_{WR}$ .

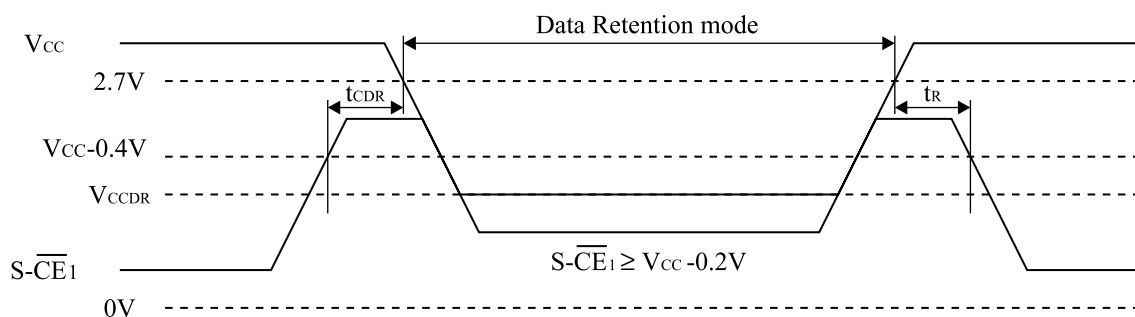
## 9.5 Data Retention Characteristics for SRAM

 $(T_A = -25^\circ\text{C to } +85^\circ\text{C})$ 

Symbol	Parameter	Note	Min.	Typ. <sup>(1)</sup>	Max.	Unit	Conditions
$V_{CCDR}$	Data Retention Supply voltage	2	1.5		3.1	V	$\overline{S-CE_1}, CE_2 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ , $\overline{LB}, \overline{UB} \geq V_{CC} - 0.2V$ , $CE_2 \geq V_{CC} - 0.2V$ or $\overline{S-CE_1} \leq 0.2V$
$I_{CCDR}$	Data Retention Supply current	2		2	25	$\mu\text{A}$	$V_{CC} = 3.0V$ , $\overline{S-CE_1}, CE_2 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ , $\overline{LB}, \overline{UB} \geq V_{CC} - 0.2V$ , $CE_2 \geq V_{CC} - 0.2V$ or $\overline{S-CE_1} \leq 0.2V$
$t_{CDR}$	Chip enable setup time		0			ns	
$t_R$	Chip enable hold time		$t_{RC}$			ns	

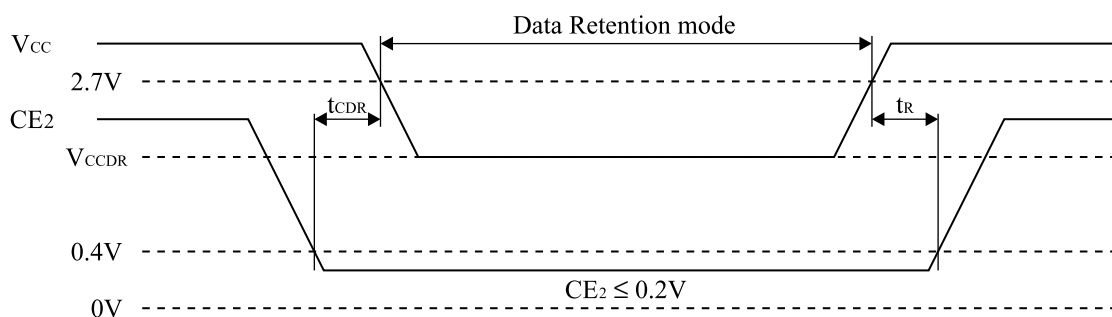
Notes:

- Reference value at  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = 3.0V$ .
- $\overline{S-CE_1} \geq V_{CC} - 0.2V$ ,  $CE_2 \geq V_{CC} - 0.2V$  ( $\overline{S-CE_1}$  controlled) or  $CE_2 \leq 0.2V$  ( $CE_2$  controlled).

Data Retention Timing Chart ( $\overline{S-CE_1}$  Controlled)<sup>(1)</sup>

Note:

- To control the data retention mode at  $\overline{S-CE_1}$ , fix the input level of  $CE_2$  between " $V_{CCDR}$  and  $V_{CCDR} - 0.2V$ " or " $0V$  and  $0.2V$ " during the data retention mode.

Data Retention Timing Chart ( $CE_2$  Controlled)

## 10. Notes

This product is a stacked CSP package that a 64M (x16) bit Flash Memory, a 64M (x16) bit Flash Memory, a 32M (x16) bit Smartcombo RAM and a 8M (x16) bit SRAM are assembled into.

### -Supply Power

Maximum difference (between F/SC- $V_{CC}$  and S- $V_{CC}$ ) of the voltage is less than 0.3V.

### -Power Supply and Chip Enable of Flash Memory, Smartcombo RAM and SRAM

Two or more chips among Flash memory (F<sub>1</sub>, F<sub>2</sub>), Smartcombo RAM and SRAM should not be active simultaneously.

If the two memories are active together, possibly they may not operate normally by interference noises or data collision on DQ bus.

Both F/SC- $V_{CC}$  and S- $V_{CC}$  are needed to be applied by the recommended supply voltage at the same time except Smartcombo RAM sleep mode and/or SRAM data retention mode.

### -Power Up Sequence

When turning on Flash memory power supply, keep  $\overline{RST}$  low. After F/SC- $V_{CC}$  reaches over 2.7V, keep  $\overline{RST}$  low for more than 100 nsec.

### -Device Decoupling

This is a 4 chips stacked CSP package. When one of the chips is active, others are in standby mode. Therefore, these power supplies should be designed very carefully.

Exclusive power supply pins for each Memory and GND pin need careful decoupling of devices. Especially, note Flash Memory, Smartcombo RAM and SRAM peak current caused by transition of control signals.

When one of the Flash Memory is in busy mode, (page buffer) program, block erase and full chip erase command should not be inputted to the other (F<sub>1</sub>-CE, F<sub>2</sub>-CE, SC-CE<sub>1</sub>, S-CE<sub>1</sub>, CE<sub>2</sub>).

## 11. Flash Memory Data Protection

Noises having a level exceeding the limit specified in the specification may be generated under specific operating conditions on some systems. Such noises, when induced onto F- $\overline{\text{WE}}$  signal or power supply, may be interpreted as false commands and causes undesired memory updating. To protect the data stored in the flash memory against unwanted writing, systems operating with the flash memory should have the following write protect designs, as appropriate:

■ The below describes data protection method.

### 1. Protection of data in each block

- Any locked block by setting its block lock bit is protected against the data alternation. When  $\overline{\text{WP}}$  is low, any locked-down block by setting its block lock-down bit is protected from lock status changes. By using this function, areas can be defined, for example, program area (locked blocks), and data area (unlocked blocks).
- For detailed block locking scheme, see Section 6.2, 7.2 Command Definitions for Flash Memory.

### 2. Protection of data with $V_{\text{PP}}$ control

- When the level of  $V_{\text{PP}}$  is lower than  $V_{\text{PPLK}}$  ( $V_{\text{PP}}$  lockout voltage), write functions to all blocks are disabled. All blocks are locked and the data in the blocks are completely protected.

### 3. Protection of data with $\overline{\text{RST}}$

- Especially during power transitions such as power-up and power-down, the flash memory enters reset mode by bringing  $\overline{\text{RST}}$  to low, which inhibits write operation to all blocks.
- For detailed description on  $\overline{\text{RST}}$  control, see Section 6.6.6, 7.6.6 AC Electrical Characteristics for Flash Memory, Reset Operations.

■ Protection against noises on F- $\overline{\text{WE}}$  signal

To prevent the recognition of false commands as write commands, system designer should consider the method for reducing noises on F- $\overline{\text{WE}}$  signal.

## 12. Design Considerations

### 1. Power Supply Decoupling

To avoid a bad effect to the system by flash memory, Smartcombo RAM and SRAM power switching characteristics, each device should have a 0.1 $\mu$ F ceramic capacitor connected between F/SC-V<sub>CC</sub> and GND, between V<sub>PP</sub> and GND and between S-V<sub>CC</sub> and GND.

Low inductance capacitors should be placed as close as possible to package leads.

### 2. V<sub>PP</sub> Trace on Printed Circuit Boards

Updating the memory contents of flash memories that reside in the target system requires that the printed circuit board designer pay attention to the V<sub>PP</sub> Power Supply trace. Use similar trace widths and layout considerations given to the F/SC-V<sub>CC</sub> power bus.

### 3. The Inhibition of Overwrite Operation

Please do not execute reprogramming "0" for the bit which has already been programmed "0". Overwrite operation may generate unerasable bit.

In case of reprogramming "0" to the data which has been programmed "1".

- Program "0" for the bit in which you want to change data from "1" to "0".
- Program "1" for the bit which has already been programmed "0".

For example, changing data from "1011110110111101" to "1010110110111100" requires "111011111111110" programming.

### 4. Power Supply

Block erase, full chip erase, (page buffer) program with an invalid V<sub>PP</sub> (See Chapter 6.5, 7.5 DC Electrical Characteristics for Flash Memory) produce spurious results and should not be attempted.

Device operations at invalid F/SC-V<sub>CC</sub> voltage (See Chapter 6.5, 7.5 DC Electrical Characteristics for Flash Memory, 8.2 DC Electrical Characteristics for Smartcombo RAM) produce spurious results and should not be attempted.



13. Related Document Information<sup>(1)</sup>

Document No.	Document Name
FUM00701	LH28F320BF, LH28F640BF, LH28F128BF Series Appendix

Note:

1. International customers should contact their local SHARP or distribution sales offices.

## LRS1B12 Flash MEMORY ERRATA

**1. AC Characteristics****PROBLEM**

The table below summarizes the AC characteristics.

AC Characteristics - Write Operations

$$V_{CC}=2.7V-3.1V$$

Page	Symbol	Parameter	Min.	Max.	Unit
22, 43	$t_{AVAV}$	Write Cycle Time	75		ns
22, 43	$t_{WHWL}$ ( $t_{EHEL}$ )	F- $\overline{WE}$ (F- $\overline{CE}$ ) Pulse Width High	25		ns

**WORKAROUND**

System designers should consider these specifications.

**STATUS**

This is intended to be fixed in future devices.

## A-1 RECOMMENDED OPERATING CONDITIONS

### A-1.1 At Device Power-Up

AC timing illustrated in Figure A-1 is recommended for the supply voltages and the control signals at device power-up. If the timing in the figure is ignored, the device may not operate correctly.

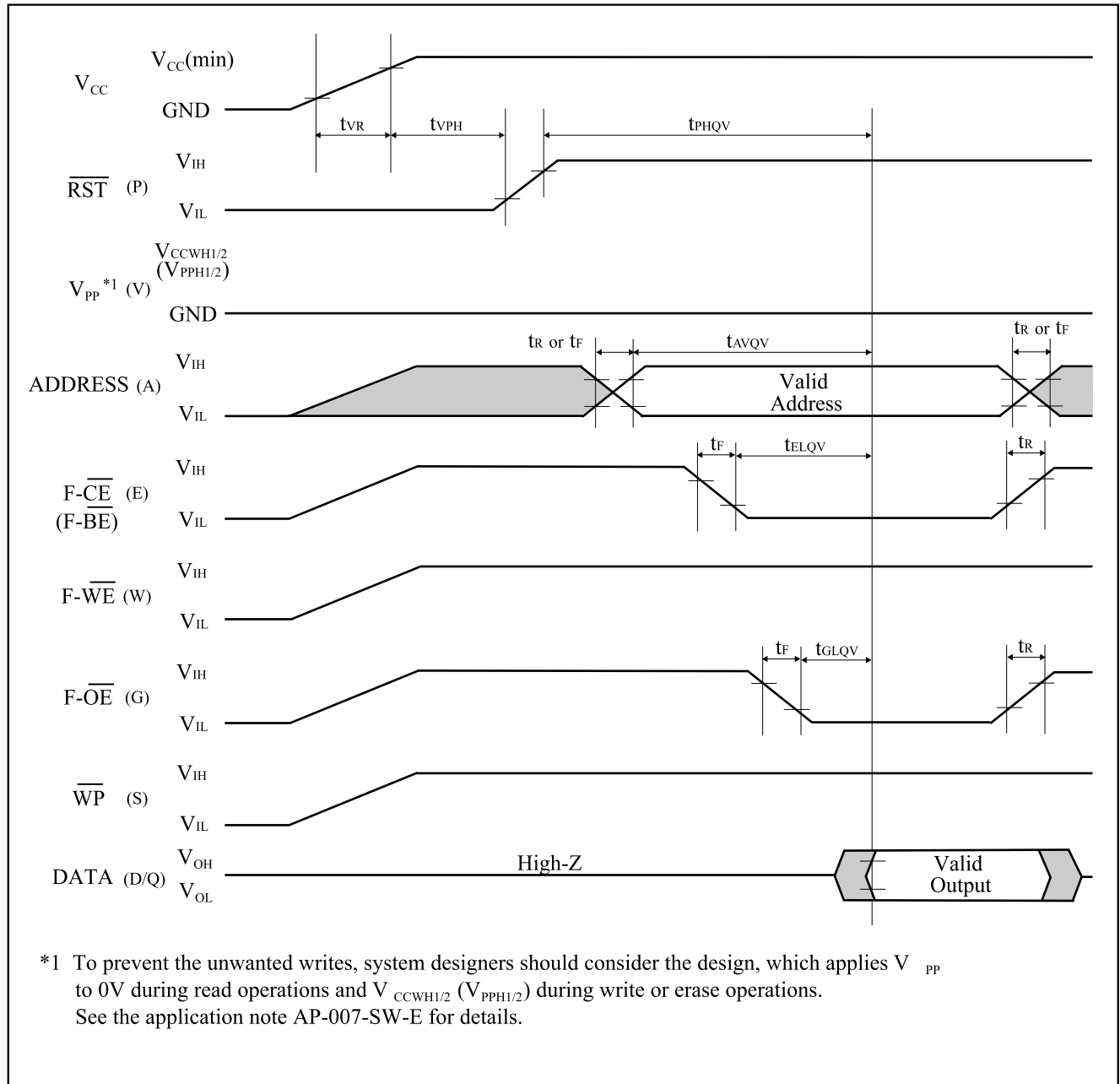


Figure A-1. AC Timing at Device Power-Up

For the AC specifications  $t_{VR}$ ,  $t_R$ ,  $t_f$  in the figure, refer to the next page. See the “AC Electrical Characteristics for Flash Memory” described in specifications for the supply voltage range, the operating temperature and the AC specifications not shown in the next page.

## A-1.1.1 Rise and Fall Time

Symbol	Parameter	Notes	Min.	Max.	Unit
$t_{VR}$	$V_{CC}$ Rise Time	1	0.5	30000	$\mu\text{s/V}$
$t_R$	Input Signal Rise Time	1, 2		1	$\mu\text{s/V}$
$t_F$	Input Signal Fall Time	1, 2		1	$\mu\text{s/V}$

## NOTES:

1. Sampled, not 100% tested.
2. This specification is applied for not only the device power-up but also the normal operations.

## A-1.2 Glitch Noises

Do not input the glitch noises which are below  $V_{IH}$  (Min.) or above  $V_{IL}$  (Max.) on address, data, reset, and control signals, as shown in Figure A-2 (b). The acceptable glitch noises are illustrated in Figure A-2 (a).

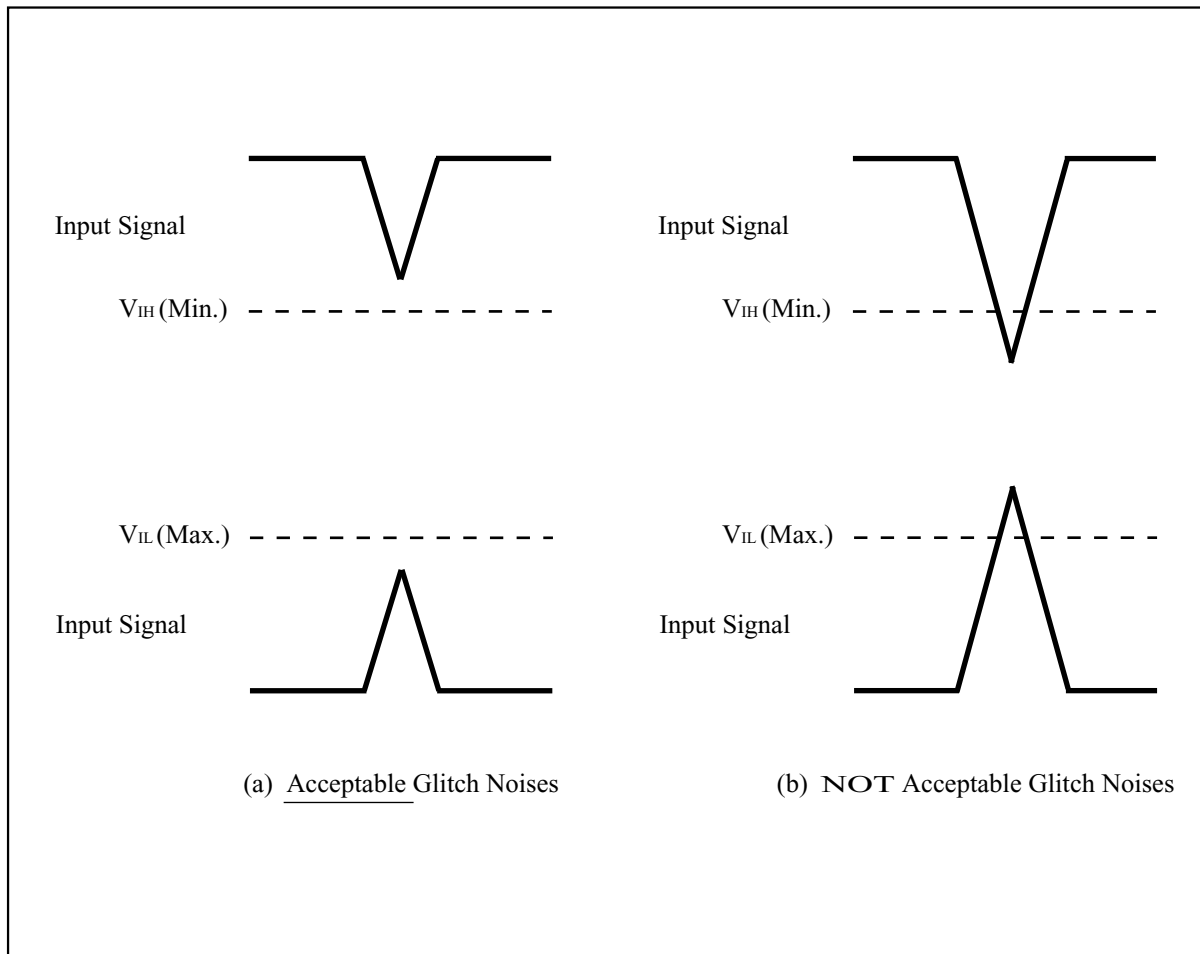


Figure A-2. Waveform for Glitch Noises

See the “DC Electrical Characteristics” described in specifications for  $V_{IH}$  (Min.) and  $V_{IL}$  (Max.).

A-2 RELATED DOCUMENT INFORMATION<sup>(1)</sup>

Document No.	Document Name
AP-001-SD-E	Flash Memory Family Software Drivers
AP-006-PT-E	Data Protection Method of SHARP Flash Memory
AP-007-SW-E	RP#, $V_{PP}$ Electric Potential Switching Circuit

## NOTE:

1. International customers should contact their local SHARP or distribution sales office.

### A-3 STATUS REGISTER READ OPERATIONS

If AC timing for reading the status register described in specifications is not satisfied, a system processor can check the status register bit SR.15 instead of SR.7 to determine when the erase or program operation has been completed.

Table A-3-1. Status Register Definition (SR.15 and SR.7)

	NOTES:
SR.15 = WRITE STATE MACHINE STATUS: (DQ <sub>15</sub> ) 1 = Ready in All Partitions 0 = Busy in Any Partition	SR.15 indicates the status of WSM (Write State Machine). If SR.15="0", erase or program operation is in progress in any partition.
SR.7 = WRITE STATE MACHINE STATUS FOR EACH PARTITION: (DQ <sub>7</sub> ) 1 = Ready in the Addressed Partition 0 = Busy in the Addressed Partition	SR.7 indicates the status of the partition. If SR.7="0", erase or program operation is in progress in the addressed partition. Even if the SR.7 is "1", the WSM may be occupied by the other partition.

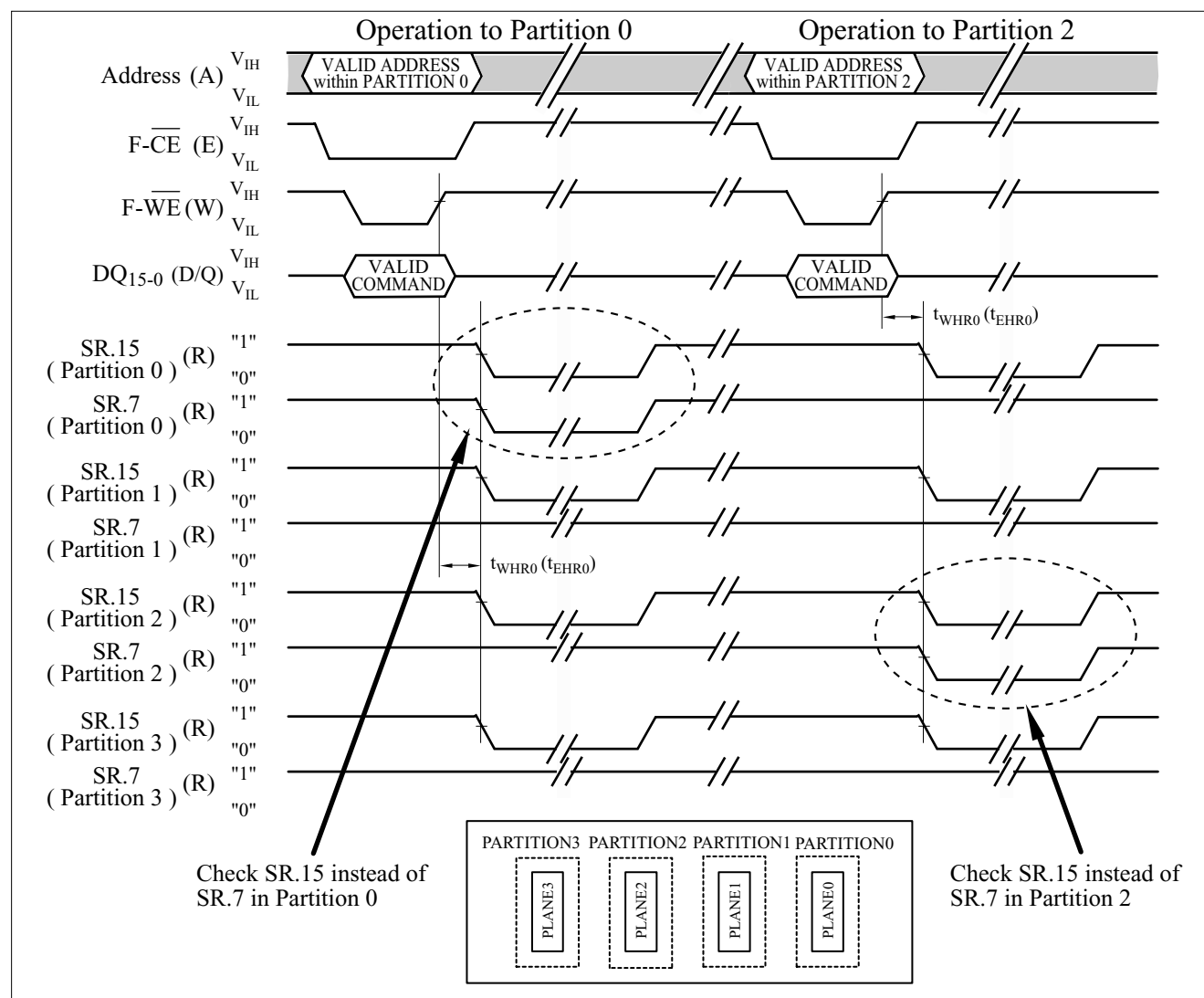


Figure A-3-1. Example of Checking the Status Register  
(In this example, the device contains four partitions.)

## B-1 POWER UP SEQUENCE OF Smartcombo RAM

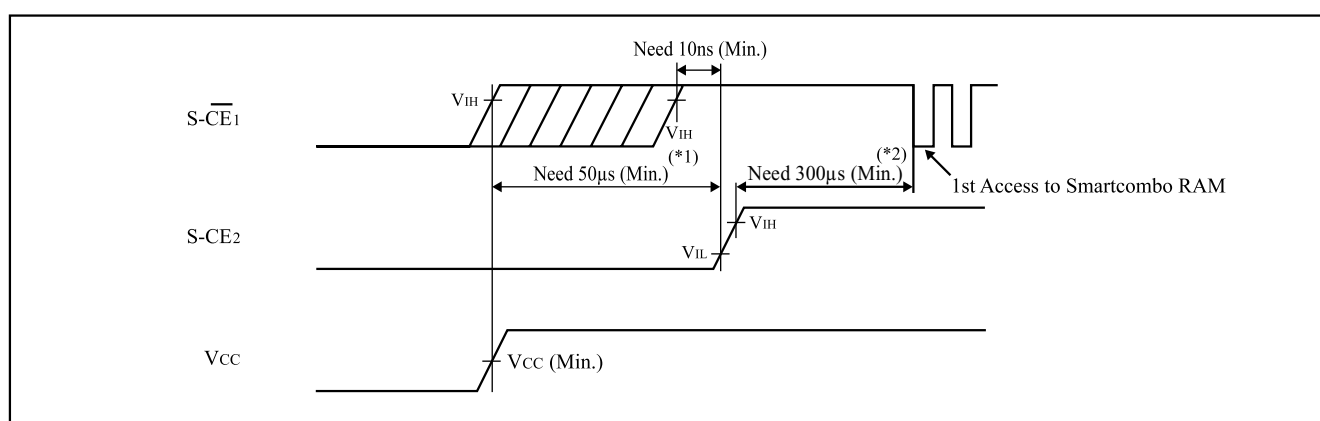
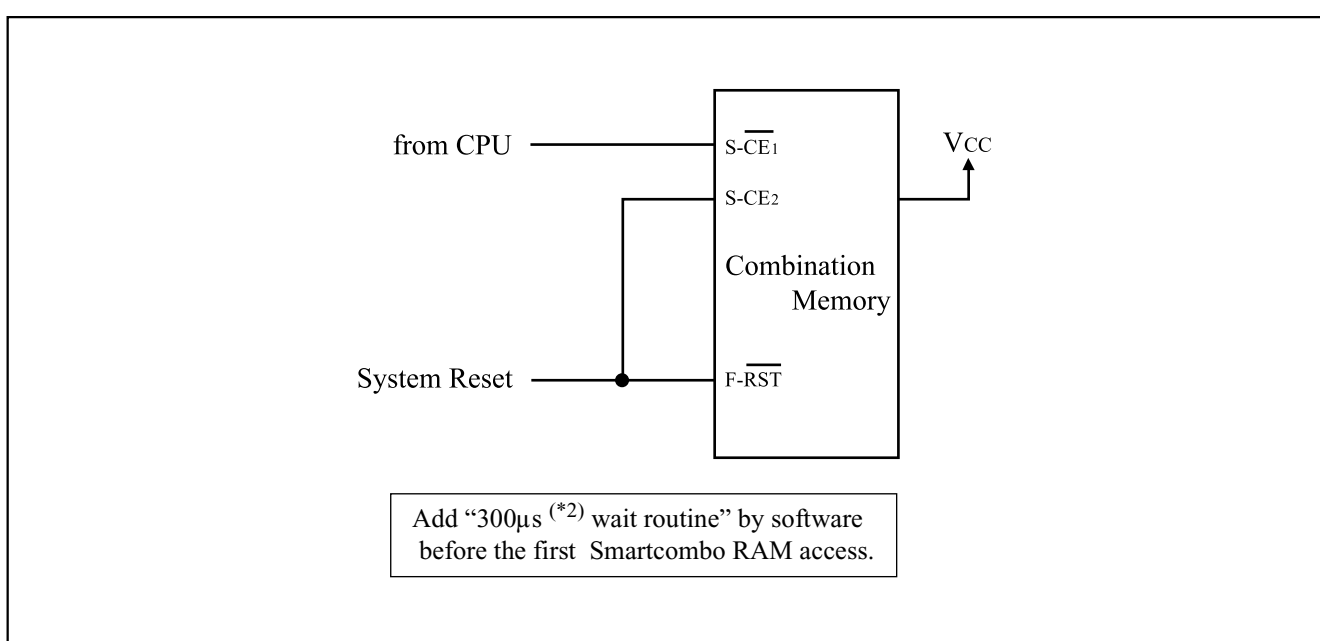
When turning on Smartcombo RAM power supply, the following sequence is needed.

### B-1.1 Sequence of Smartcombo RAM Power Supply

- (1) Supply power.
- (2) Keep S-CE<sub>2</sub> low longer than or equal to 50 $\mu$ s. (See NOTES \*1)
- (3) Keep S- $\overline{\text{CE}}_1$  and S-CE<sub>2</sub> high longer than or equal to 300 $\mu$ s. (See NOTES \*2)
- (4) End of Initialization.

By executing above (1) to (4), the initialization of chip inside and the power occurred inside become stable.

<Example of the actual connection>



#### NOTES:

- \*1) Connect System Reset signal to S-CE<sub>2</sub> and hold S-CE<sub>2</sub> low longer than or equal to 50 $\mu$ s.
- \*2) By adding "300 $\mu$ s Wait Routine" (S- $\overline{\text{CE}}_1$  and S-CE<sub>2</sub> high) in the software, delay the first access to Smartcombo RAM longer than or equal to 300 $\mu$ s.