Elektronische Bauelemente

SSRF50P04-16

50A, -40V, $R_{DS(ON)}$ 16mΩ

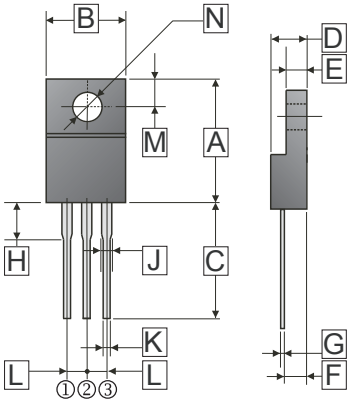
P-Ch Enhancement Mode Power MOSFET

RoHS Compliant Product
A suffix of "-C" specifies halogen free

DESCRIPTION

These miniature surface mount MOSFETs utilize a high cell density trench process to provide Low $R_{DS(on)}$ and to ensure minimal power loss and heat dissipation. Typical applications are DC-DC converters and power management in portable and battery-powered products such as computers, printers, PCMCIA cards, cellular and cordless telephones.

ITO-220



Dimensions in millimeters

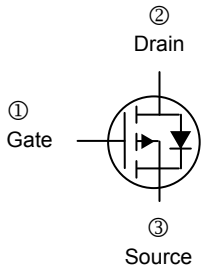
REF.	Millimeter		REF.	Millimeter	
	Min.	Max.		Min.	Max.
A	15.00	15.60	H	3.00	3.80
B	9.50	10.50	J	0.90	1.50
C	13.00 Min		K	0.50	0.90
D	4.30	4.70	L	2.34	2.74
E	2.50	3.10	M	2.50	2.90
F	2.40	2.80	N	ϕ3.1	ϕ3.4
G	0.30	0.70			

FEATURES

- Low $R_{DS(on)}$ provides higher efficiency and extends battery life.
- Low thermal impedance copper leadframe ITO-220 saves board space.
- Fast switching speed.
- High performance trench technology.

PRODUCT SUMMARY

SSRF50P04-16		
V_{DS}(V)	R_{DS}(on) (mΩ)	I_D(A)
-40	16@V_{GS}= -10V	50
	28@V_{GS}= -4.5V	38



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Drain-Source Voltage	V_{DS}	-40	V
Gate-Source Voltage	V_{GS}	±20	V
Continuous Drain Current [1]	I_D @T_C=25℃	50	A
Pulsed Drain Current [2]	I_{DM}	±100	A
Continuous Source Current (Diode Conduction) [1]	I_S	-30	A
Total Power Dissipation [1]	P_D @T_C=25℃	60	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 ~ 175	°C
THERMAL RESISTANCE RATINGS			
Maximum Thermal Resistance Junction-Ambient [1]	$R_{\theta JA}$	50	°C / W
Maximum Thermal Resistance Junction-Case	$R_{\theta JC}$	3.0	°C / W

Notes：
1 Package Limited.
2 Pulse width limited by maximum junction temperature.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

PARAMETER	SYMBO	MIN.	TYP.	MAX.	UNIT	TEST CONDITIONS
Static						
Gate-Threshold Voltage	$V_{GS(th)}$	-1	-	-	V	V_{DS}= V_{GS}, I_D = -250 μA
Gate-Body Leakage	I_{GSS}	-	-	±100	nA	V_{DS} = 0V, V_{GS}= ±25V
Zero Gate Voltage Drain Current	I_{DSS}	-	-	-1	μA	V_{DS}= -24V, V_{GS}= 0V
		-	-	-5		V_{DS}= -24V,V_{GS}= 0V,T_J=55°C
On-State Drain Current [1]	$I_{D(on)}$	-41	-	-	A	V_{DS} = -5V, V_{GS}= -10V
Drain-Source On-Resistance [1]	$R_{DS(ON)}$	-	-	16	mΩ	V_{GS}= -10V, I_D= -1 A
		-	-	28		V_{GS}= -4.5V, I_D= -1 A
Forward Transconductance [1]	g_{fs}	-	31	-	S	V_{DS}= -15V, I_D= -1 A
Diode Forward Voltage	V_{SD}	-	-0.7	-	V	I_S= -41 A, V_{GS}= 0 V
Dynamic [2]						
Total Gate Charge	Q_g	-	25	-	nC	V_{DS} = -15 V V_{GS} = -4.5 V I_D = -1 A
Gate-Source Charge	Q_{gs}	-	5.2	-		
Gate-Drain Charge	Q_{gd}	-	17	-		
Turn-on Delay Time	$T_{d(on)}$	-	15	-	nS	V_{DD}= -15 V I_D= -41 A V_{GEN} = 10 V R_L= 15 Ω R_G= 6 Ω
Rise Time	T_r	-	44	-		
Turn-off Delay Time	$T_{d(off)}$	-	46	-		
Fall Time	T_f	-	89	-		

Notes
1 Pulse test：Pulse width ≦ 300 μs, duty cycle ≦ 2%.
2 Guaranteed by design, not subject to production testing.