Analog Signal Input Class-D Amplifier for Piezo Speaker with DC-DC Converter

■ GENERAL DESCRIPTION

The NJW1262 is an analog signal input monaural class-D amplifier for Piezo speaker. And a built-in DC-DC converter generates fixed output voltage. Therefore, it realizes 7Vrms@1kHz output signal with louder sound and high efficiency.

The NJW1262 incorporates BTL amplifier, which eliminate AC coupling capacitors, and it is capable of driving Piezo speaker with simple external LC low-pass filters.

Class-D operation achieves lower power operation for Piezo speaker, thus the NJW1262 is suited for battery-powered applications.

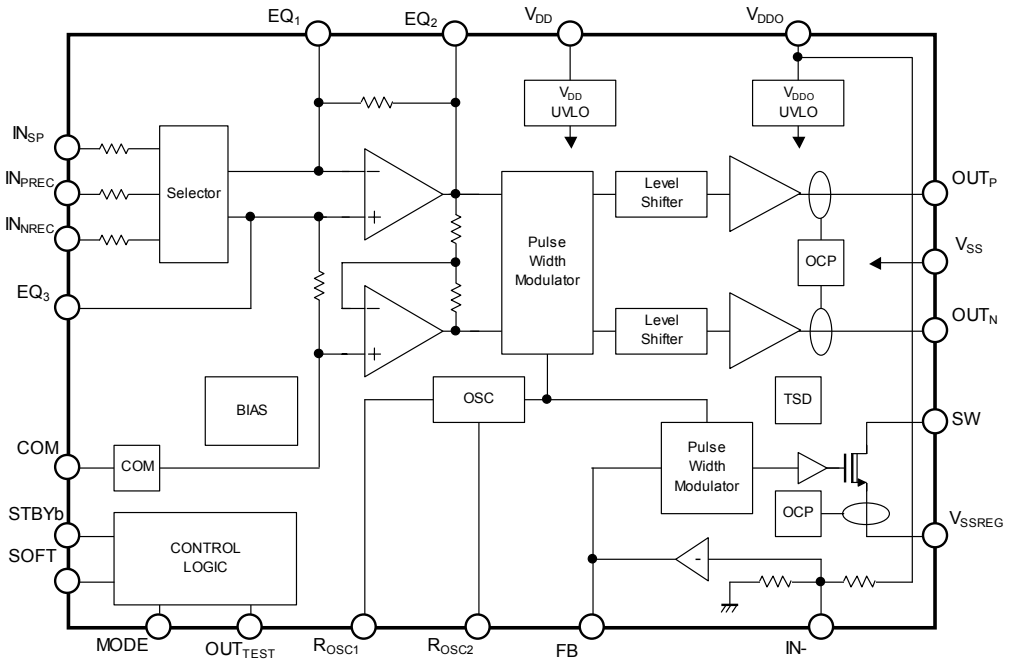
■ PACKAGE OUTLINE

NJW1262NL2

■ FEATURES

- Output Voltage VDD=3.0V to 4.2V
  VDDO=13.0V@SP MODE
  VDDO=4.5V@REC MODE
- Analog Audio Signal Input
- 2input selector (Speaker Mode and Receiver Mode)
- 1-channel BTL Output, Piezo Speaker Driving
- Built-in DC-DC Converter
- Built-in Low Voltage Detector
- Standby (Hi-Z), Soft Start, Soft Mute Control
- Built-in Pop noise reduction
- Built-in Short Protector)
- Built-in Thermal Protection
- Package Outline: EPCSP32

■ BLOCK DIAGRAM

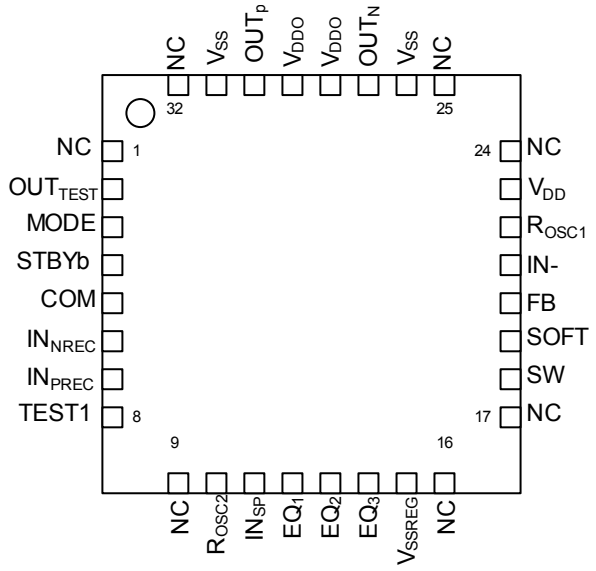


■ PIN CONFIGURATION

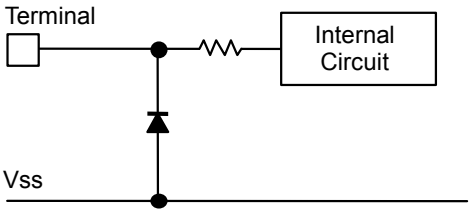
No.	SYMBOL	I/O	Function
23	V_{DD}	–	Power supply:V_{DD} =3.7 V
28,29	V_{DDO}	–	Output Power supply:V_{DDO} =13 V
11	IN_{SP}	I	Noninverted signal input (SP Mode) terminal
7	IN_{PREC}	I	Noninverted signal input (REC Mode) terminal
6	IN_{NREC}	I	Inversion signal Input (REC Mode)
12	EQ_1	I/O	LPF Setting terminal
13	EQ_2	I/O	LPF Setting terminal
14	EQ_3	I/O	LPF Setting terminal
5	COM	I/O	Bias terminal
19	SOFT	I/O	Capacitor connection terminal for soft start
4	STBYb	I	Standby control terminal (STBYb =L: Standby)
3	MODE	I	SP/REC mode switch terminal (MODE =H: SP Mode, MODE =L: REC Mode) The mode maintains the logic when the STBYb terminal is started up.
22	R_{OSC1}	I/O	Class-D Amplifier Oscillator resistance connection terminal
10	R_{OSC2}	I/O	Switching Regulator Oscillator resistance connection terminal
26,31	V_{SS}	–	GND:V_{SS} =0 V
30	OUT_P	O	Noninverted signal output terminal
27	OUT_N	O	Inversion signal output terminal
2	OUT_{TEST}	O	Test Pin (50kΩ ground) Should be floating or V_{SS} fixation.
18	SW	O	Inductor connection terminal
15	V_{SSREG}	–	GND:V_{SSREG} =0 V
21	IN-	I/O	Phase compensating device connection terminal for switching regulator
20	FB	I/O	Phase compensating device connection terminal for switching regulator
8	TEST1	I	Test Pin (50kΩ ground) Should be floating or V_{SS} fixation.
1, 9,16,17, 24,25,32	NC		NC pin Should be floating or V_{SS} fixation.

Note: $V_{BAT} = V_{DD}$
Note: Do not do floating the input terminal.

■ TERMINAL CONFIGURATION



■ INPUT TERMINAL



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	CONDITIONS	RATING	UNIT
Supply Voltage	V_{DD} V_{DDO}	V_{DD} V_{DDO}	-0.3 to +5.5 -0.3 to +36	V
Input Voltage	V_{IN}	IN_{SP}, IN_{PREC}, IN_{NREC}, STBYb, MODE, OUT_{TEST}	-0.3 to V_{DD}+0.3	V
Operating Temperature	Topr		-40 to +85	°C
Storage Temperature	Tstg		-40 to +125	°C
Power Dissipation	P_{DMAX2}	2 layers (EIAJ), T_j = 125°C	760	mW
	P_{DMAX4}	4 layers (EIAJ), T_j = 125°C	1800	mW
Thermal resistance	θ_{ja2}	2 layers (EIAJ), T_j = 125°C	132	°C /W
	θ_{ja4}	4 layers (EIAJ), T_j = 125°C	54	°C /W

Note 1) All voltage are relative to "V_{SS} =0V" reference.
Note 2) Power dissipation is a value in condition where it is mounted on 2-layer/ 4-layer board based on EIA/JEDEC.
Note 3) The IC must be used inside of the "Absolute maximum ratings". Otherwise, a stress may cause permanent damage to the LSI.
Note 4) De-coupling capacitors must be connected between each power supply terminal and GND (V_{DD}-V_{SS}, V_{DDO}-V_{SS}).
Note 5) The maximum power dissipation in the system is calculated, as shown below.

$$P_{DMAX} = \frac{T_{jMAX}[°C] - T_a[°C]}{\theta_{ja}[°C/W]}$$

Pdmax: Maximum Power Dissipation, Tjmax: Junction Temperature = 125°C
Ta: Ambient Temperature, θja: Thermal Resistance of package = 132°C/W

$$P_D = \frac{125°C - 50°C}{132°C/W} = 570[mW]$$

■ELECTRICAL CHARACTERISTICS

● DC Characteristics

T_a = 25 °C,V_{DD} = 3.7 V, V_{DDO} = 13.0 V(SP Mode), V_{DDO} = 4.5V (REC Mode), V_{SS} = V_{SSREG} = 0.0 V, Load= 1.5 μF, R_{OSC1}= 82 kΩ, R_{OSC2}= 82 kΩ, C_{LPF}= 330 pF, Cc=0.033 μF, Output Filter: [L_{OUT}= 22μH, R_{DAMP}= 3.9 Ω]
SW regulator: [L_{SW}= 6.8μH, C_{SW}= 20μF+ 0.1μF, C_{cmpn1}= 4.7 nF, R_{cmpn}= 68 kΩ]
Input Signal :IN_{SP}= 100 mVrms, IN_{PREC}- IN_{NREC} =100 mVrms, Input Frequency= 1 kHz

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{DD}		3.0	3.7	4.2	V
Boost voltage	V_{SWSP}	SP Mode	11.9	13	14.1	V
	V_{SWREC}	REC Mode	4.2	4.5	4.8	V
Output Driver On-state Resistance (High-side)	R_{ONHSP}	SP Mode, OUT_P, OUT_N $V_{OUTP, N}$ = V_{DDO} - 0.1 V	1.3	2.0	2.4	Ω
	R_{ONHREC}	REC Mode, OUT_P, OUT_N $V_{OUTP, N}$ = V_{DD} - 0.1 V	1.3	2.2	2.8	Ω
Output Driver On-state Resistance (Low-side)	R_{ONLSP}	SP Mode, OUT_P, OUT_N $V_{OUTP, N}$ = 0.1 V	1.3	2.0	2.4	Ω
	R_{ONLREC}	REC Mode, OUT_P, OUT_N $V_{OUTP, N}$ =0.1 V	1.3	2.2	2.8	Ω
Switching Regulator Output Driver On-state Resistance	R_{ONSW}	SW V_{SW} = 0.1 V	0.05	0.4	0.7	Ω
Input Impedance	R_{INSP}	IN_{SP}	90	120	150	kΩ
	R_{INPREC}	IN_{PREC}	180	240	300	kΩ
	R_{INNREC}	IN_{NREC}	280	360	440	kΩ
Operating Current (Standby)	I_{ST}	STBYb: "L",No Load	-	-	1	μA
Operating Current (No signal input)	I_{BATSP}	SP Mode, Non-LC Filter, No Load	-	11	14	mA
	I_{BATREC}	REC Mode Non-LC Filter, No Load	-	4.0	5.0	mA

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input Voltage	V_{IH}	STBYb, MODE Pin	1.5	-	V_{DD}	V
	V_{IL}	STBYb, MODE Pin	0	-	0.5	V
Input Leakage Current	I_{LK}	STBYb, MODE Pin	-	-	±1	μA
SW Off Leak Current	I_{LKSW}	SW Pin	-	-	±1	μA
OUT_P Ground Resistance	R_{OUTP}	OUT_P Pin	70	100	130	kΩ
OUT_N Ground Resistance	R_{OUTN}	OUT_N Pin	70	100	130	kΩ
Class-D Amplifier Oscillation Frequency	f_{OSCD}		180	250	320	kHz
Switching Regulator Oscillation Frequency	f_{OSCSW}		500	600	750	kHz
Soft Start Resistance	R_{SST}	SOFT Pin	35	50	65	kΩ
Soft Mute Resistance	R_{SMT}	SOFT Pin	35	50	65	kΩ
Start-up Time	T_{ON}		5.0	6.7	8.4	ms
Stop Time	T_{OFF}		10	13.3	16.6	ms
Class-D Amplifier Voltage Gain	Av_{SP}	SP Mode, No Load C_{LPF}=100 pF	-	27.6	-	dB
	Av_{REC}	REC Mode, No Load C_{LPF}=100 pF	-	5.1	-	dB
MODE Setup Time	T_{STUP}	Refer to Figure 1.	10	-	-	μs
MODE Holding Time	T_{HLD}	Refer to Figure 1.	50	-	-	μs
Offset Voltage	V_{OFFSET}	REC Mode 2ms After OUT_P and OUT_N pin start switching	-20	-	20	mV

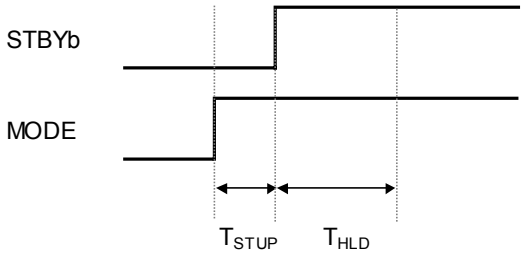


Figure 1: STBYb/MODE input timing

● **AC Characteristics**

T_a = 25 °C,V_{DD} = 3.7 V, V_{DDO} = 13.0 V(SP Mode), V_{DDO} = 4.5V (REC Mode), V_{SS} = V_{SSREG} = 0.0 V, Load = 1.5 μF, R_{OSC1}= 82 kΩ, R_{OSC2}= 82 kΩ, C_{LPF}= 330 pF, Cc=0.033 μF, Output Filter: [L_{OUT}= 22μH, R_{DAMP}= 3.9 Ω]
SW regulator: [L_{SW}= 6.8μH, C_{SW}= 20μF+ 0.1μF, C_{cmpn1}= 4.7 nF, R_{cmpn}= 68 kΩ]
Input Signal :IN_{SP}= 100 mVrms, IN_{PREC}- IN_{NREC} =100 mVrms, Input Frequency= 1 kHz

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
THD+N	$THD+N_{SP}$	SP Mode, V_{OUTSP} =2.5 Vrms	-	0.2	-	%
	$THD+N_{REC}$	REC Mode V_{OUTREC} =1 Vrms	-	0.08	-	%
Maximum Output Voltage	V_{OUTSP}	SP Mode, THD+N=2 %	-	7	-	V_{rms}
	V_{OUTREC}	REC Mode, THD+N=2 %	-	2.7	-	Vrms
S/N	SN	REC MODE, V_{OUTREC} =1 Vrms A-weight	-	80	-	dB
Noise Floor	V_N	REC MODE, A-weight	-	100	-	μVrms

Note) A noise by the Class-D amplifier oscillation frequency and the switching regulator oscillation frequency may be felt in receiver mode. Therefore, please test the circuit carefully to fit your application.

■ FUNCTIONAL DESCRIPTION

● Signal Input Terminal (IN_{SP}, IN_{PREC}, IN_{NREC})

Analog signal input. The input signal is selected by the operational mode.

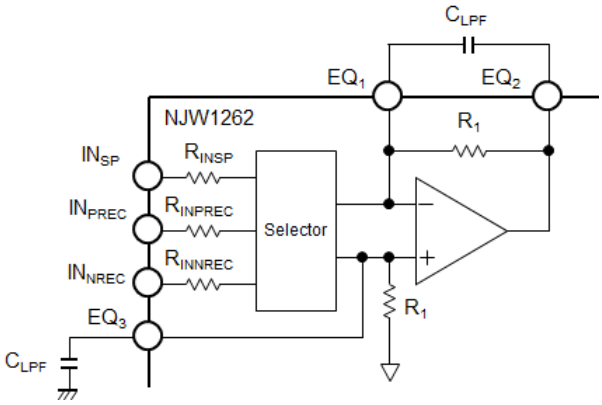
● Capacitor connection terminal for LPF (EQ1, EQ2, EQ3)

The amount of current passing through a capacitive load increases proportionately with frequency of audio signal. Input filters should be put in the input line to reduce load current at high frequency-band. The input low pass filters are composed of feedback resister (R_1) and capacitor (C_{LPF}).

Refer to the following expression.

R_1= 120kΩ, C_{LPF}= 330pF

$$f_{LPF} = \frac{1}{2\pi R_1 C_{LPF}} = \frac{1}{2 \times 3.14 \times 120k\Omega \times 330pF} \quad 4.0[kHz]$$



R_1=120[kΩ]

Figure 2: Input LPF composition

● Signal Output Terminal (OUT_P, OUT_N)

The output signals are PWM signals, which will be converted to analog signal via external 2nd-order or higher LC filter. Should be connected to the damping resistor (R_{DAMP}) between OUT_P pin and coil, and between OUT_N pin and coil to reduce the current consumption with signal-input close to cutoff-frequency of LPF (f_c).

Set the value of LOUT, CL, and RDAMP to become Q<1.

Refer to the following expression.

L_{OUT} =22μH, C_L=1.5μF, R_{DAMP}=3.9Ω, Equivalent series resistance of L (R_{DCR}) =0.8Ω

$$f_c = \frac{1}{2\pi\sqrt{2L_{OUT}C_L}} = \frac{1}{2 \times 3.14 \times \sqrt{2 \times 22\mu H \times 1.5\mu F}} \quad 19.6[kHz]$$

$$Q = \frac{1}{R_{DAMP} + R_{DCR}} \sqrt{\frac{L_{OUT}}{2 \times C_L}} = \frac{1}{3.9\Omega + 0.4\Omega} \times \sqrt{\frac{22\mu H}{2 \times 1.5\mu F}} \quad 0.63$$

● Standby Terminal (STBYb)

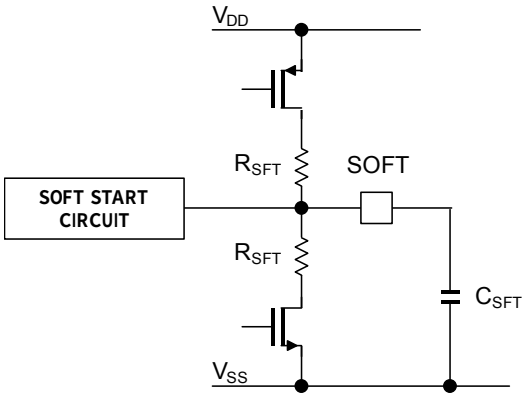
By setting the STBYb pin to “L” level, it switches the NJW1262 into standby condition. During the standby condition, output pins (OUT_P, OUT_N, SW) become high impedance and class-D amplifier output is connected with V_{SS} with about 100kΩ. Keep the STBYb pin to “L” level at least 13.3ms once switched into the standby condition.

For normal operation, the STBYb pin requires “H” level. Time from the standby release to class-D power amplifier operation is 6.7ms(TYP). Do not change to the standby mode until the power amplifier operation.

Set the standby mode at power supply ON/OFF.

● Capacitor connection terminal for soft start (SOFT)

Capacitor connection terminal for soft start and soft mute.



R_{SFT}=50[kΩ]
C_{SFT}=0.1[μF]

● Step-up switching regulator

The switching regulator is used as power supply (V_{DDO}) for power amplifier of class-D. The PWM controlled switching regulator works with external components, which are coil, capacitor, Schottky barrier diode.

● Mode

SP/REC mode selection terminal. The output power-supply voltage, the input selector, and the voltage gain change when the mode is switched.

MODE="H":SP (Speaker) Mode Audio input terminal: IN_{SP}(Shingle end input)

Class-D amplifier output power-supply voltage: Step-up switching regulator

$$V_{SWSP} = 1.0V \times \left(1 + \frac{R_1}{R_{2SP}}\right) = 13.0V\,(TYP)$$

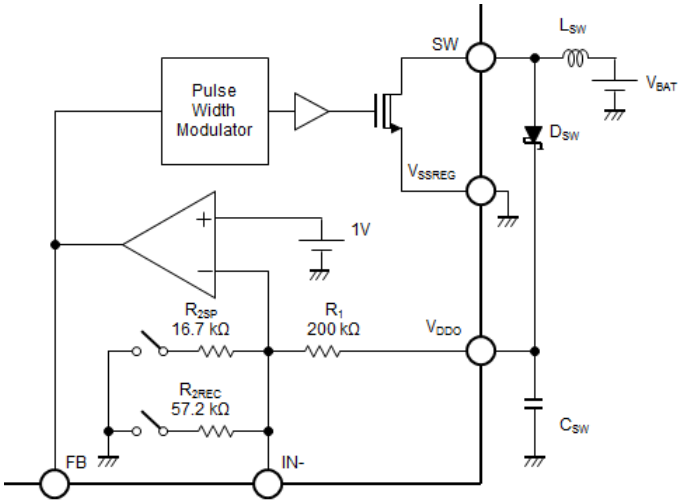
Voltage gain: 27.6 dB (TYP)

MODE="L":REC (Receiver) Mode Audio input terminal: IN_{PREC}、IN_{NREC}(Difference input)

Class-D amplifier output power-supply voltage: Step-up switching regulator

$$V_{SWREC} = 1.0V \times \left(1 + \frac{R_1}{R_{2REC}}\right) = 4.5V\,(TYP)$$

Voltage gain: 5.1 dB (TYP)



Switching regulator circuit

Note) Reset it when you switch MODE. (STBYb"L")

● Low Voltage Detector

When the power-supply voltage drops down to below V_{DD}, the output driver is turned off output pins (OUT_P, OUT_N, SW) become high impedance and class-D amplifier output is connected with V_{SS} with about 100kΩ.

● Short Circuit Protection

The short-circuit protection circuit operates at the condition of the following.

-Short between OUT_P and OUT_N

- Power supply short and earth fault of OUT_P terminal
- Power supply short and earth fault of OUT_N terminal
- Power supply short of SW terminal

When OUT_P and OUT_N of the short-circuit protection circuit operates, the OUT_P and OUT_N become high impedance and class-D amplifier output is connected with V_{SS} with about 100kΩ. It restarts by pulse-by-pulse of built-in clock of class-D amplifier.

When SW terminal of the short-circuit protection circuit operates, the SW terminal become high impedance. It restarts by pulse-by-pulse of built-in clock of the switching regulator.

Note)

*1 The detectable current and the period for the protection depend on the power supply voltage, chip temperature and ambient temperature.

*2 The short protector is not effective for a long term short-circuit current but for an instantaneous accident. Continuous high current may cause permanent damage to the NJW1262.

● Thermal protection

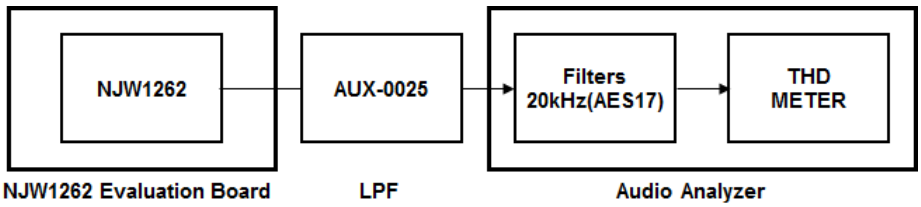
When the junction temperature is more than specified value, the output driver is turned off output pins (OUT_P, OUT_N, SW) become high impedance and class-D amplifier output is connected with V_{SS} with about 100kΩ.

When the junction temperature is less than specified value, protection is released.

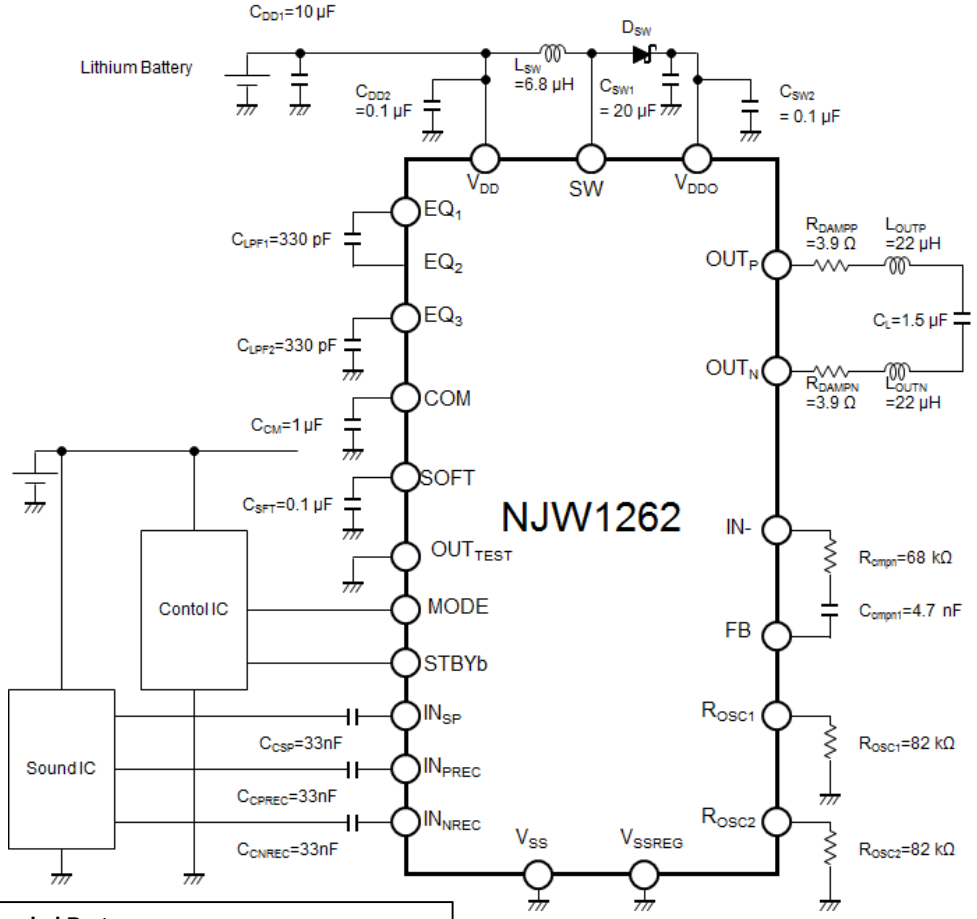
● OUT_{TEST} pin

This pin is JRC's test pin.

■ TOTAL HARMONIC DISTORTION MEASUREMENT CIRCUIT



■ TYPICAL APPLICATION CIRCUIT

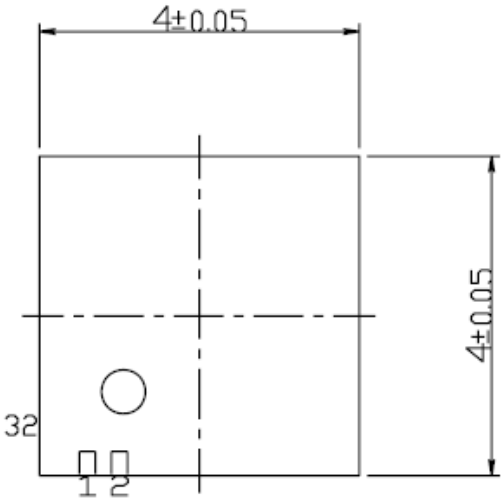


■ Recommended Parts
CL: VSLBP2115E1100-T1(muRata)
CSW1: GRM31CB31E106KA75L(muRata) ×2
CDD1: GRM31CB31E106KA75L(muRata)
CDD2,CSW2, CSFT: GRM155B31E104KA87D(muRata)
CCSP, CCPREC, CCNREC: GRM033B10J333KE01D(muRata)
CLPF1, CLPF2: GRM155B11H331KA01D(muRata)
CCM: GRM155B31A105KE15D(muRata)
LSW: LQH44PN6R8MPO(muRata)
LOUT: LQH44PN220MP0(muRata)
DSW: RSX201VA-30(ROHM)
RDAMP: ERJ-14YJ3R9U(Panasonic)
■ specifiedParts
Rosc1, Rosc2 = RK73H1JTTD8202F(KOA)

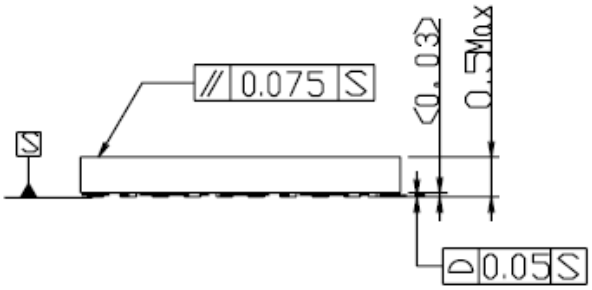
Note) De-coupling capacitors must be connected between each power supply terminal and GND (V_{DD}-V_{SS}, V_{DDO}-V_{SS}).
Note) C_{DD2} (V_{DD}-V_{SS}) should be connected at a nearest point to the IC on PCB.
Note) V_{SS} and V should be connected at a nearest point to the IC on PCB.
Note) IN_{SP}, IN_{PREC}, IN_{NREC}, EQ_1, EQ_2 and EQ_3 should be not designed near OUT_P,OUT_N and SW, which emit PWM noise.
Note) The transition time for MODE and STBYb signals must be less than 100µs. Otherwise, a malfunction may be occurred.
Note) The above circuit shows only application example and does not guarantee the any electrical characteristics. Therefore, please test the circuit carefully to fit your application.
Note) The speaker should be designed at a near the IC.

■ **PACKAGE INFORMATION**

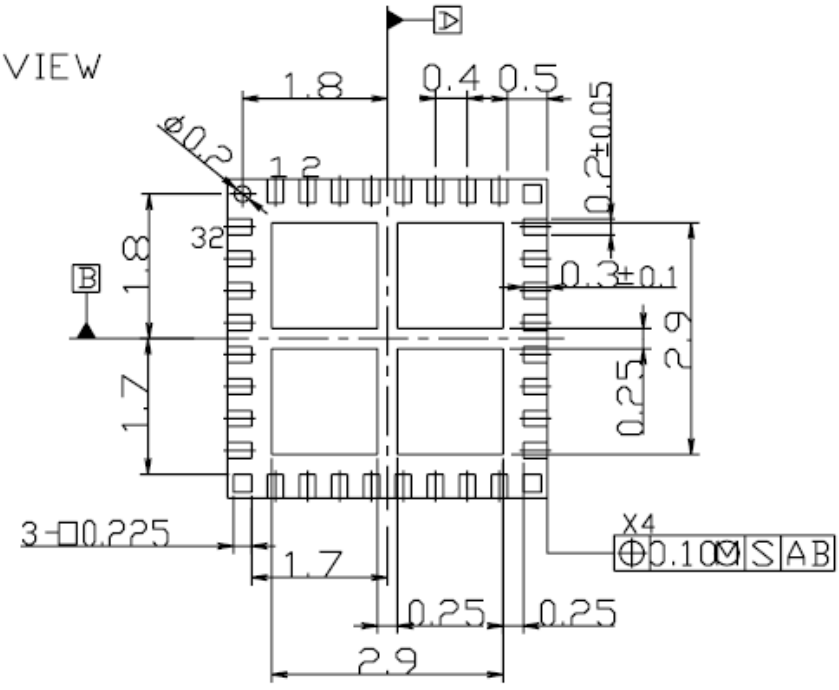
TOP VIEW



SIDE VIEW



BOTTOM VIEW



unit : mm

SUBSTRATE MATERIAL : Glass Epoxy Board
TERMINAL FINISH : Au Plating (Ni/Au)
MOLD MATERIAL : Epoxy Resin