

# RJK0656DPB

60V, 40A, 5.6mΩ max.

Silicon N Channel Power MOS FET

Power Switching

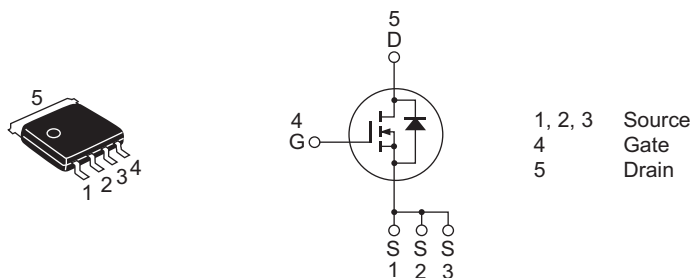
R07DS1054EJ0200  
(Previous: REJ03G1882-0100)  
Rev.2.00  
Apr 09, 2013

## Features

- High speed switching
- Low drive current
- Low on-resistance  
 $R_{DS(on)} = 4.5 \text{ m}\Omega$  typ. (at  $V_{GS} = 10 \text{ V}$ )
- Pb-free
- Halogen-free
- High density mounting

## Outline

RENESAS Package code: PTZZ0005DA-A  
(Package name: LFPAK)



## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	60	V
Gate to source voltage	$V_{GSS}$	$\pm 20$	V
Drain current	$I_D$	40	A
Drain peak current	$I_{D(pulse)}$ <sup>Note1</sup>	160	A
Body-drain diode reverse drain current	$I_{DR}$	40	A
Avalanche current	$I_{AP}$ <sup>Note 2</sup>	40	A
Avalanche energy	$E_{AS}$ <sup>Note 2</sup>	12	mJ
Channel dissipation	$P_{ch}$ <sup>Note3</sup>	65	W
Channel to Case Thermal Resistance	$\theta_{ch-C}$	1.92	$^\circ\text{C/W}$
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

- Notes: 1.  $PW \leq 10 \mu\text{s}$ , duty cycle  $\leq 1\%$   
 2. Value at  $L=10\mu\text{H}$ ,  $T_{ch} = 25^\circ\text{C}$ ,  $R_g \geq 50 \Omega$   
 3.  $T_c = 25^\circ\text{C}$

## Electrical Characteristics

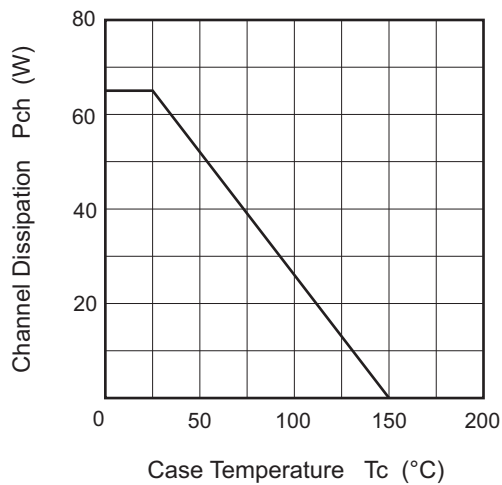
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0 \text{ V}$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.1$	$\mu\text{A}$	$V_{GS} = \pm 20 \text{ V}$ , $V_{DS} = 0 \text{ V}$
Zero gate voltage drain current	$I_{DSS}$	—	—	1	$\mu\text{A}$	$V_{DS} = 60 \text{ V}$ , $V_{GS} = 0 \text{ V}$
Gate to source cutoff voltage	$V_{GS(off)}$	2.0	—	4.0	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	4.5	5.6	$\text{m}\Omega$	$I_D = 20 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	—	58	—	S	$I_D = 20 \text{ A}$ , $V_{DS} = 10 \text{ V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	3000	—	pF	$V_{DS} = 10 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$
Output capacitance	$C_{oss}$	—	680	—	pF	
Reverse transfer capacitance	$C_{rss}$	—	175	—	pF	
Gate Resistance	$R_g$	—	0.5	—	$\Omega$	
Total gate charge	$Q_g$	—	40	—	nC	$V_{DD} = 25 \text{ V}$ , $V_{GS} = 10 \text{ V}$ , $I_D = 40 \text{ A}$
Gate to source charge	$Q_{gs}$	—	13	—	nC	
Gate to drain charge	$Q_{gd}$	—	7.0	—	nC	
Turn-on delay time	$t_{d(on)}$	—	16	—	ns	$V_{GS} = 10 \text{ V}$ , $I_D = 20 \text{ A}$ , $V_{DD} \cong 30 \text{ V}$ , $R_L = 1.5 \Omega$ , $R_g = 4.7 \Omega$
Rise time	$t_r$	—	9.0	—	ns	
Turn-off delay time	$t_{d(off)}$	—	36	—	ns	
Fall time	$t_f$	—	12	—	ns	
Body-drain diode forward voltage	$V_{DF}$	—	0.8	1.1	V	$I_F = 40 \text{ A}$ , $V_{GS} = 0 \text{ V}$ <sup>Note4</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	44	—	ns	$I_F = 40 \text{ A}$ , $V_{GS} = 0 \text{ V}$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

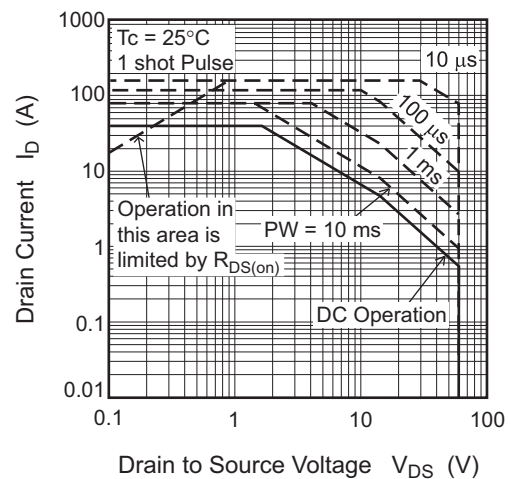
Notes: 4. Pulse test

## Main Characteristics

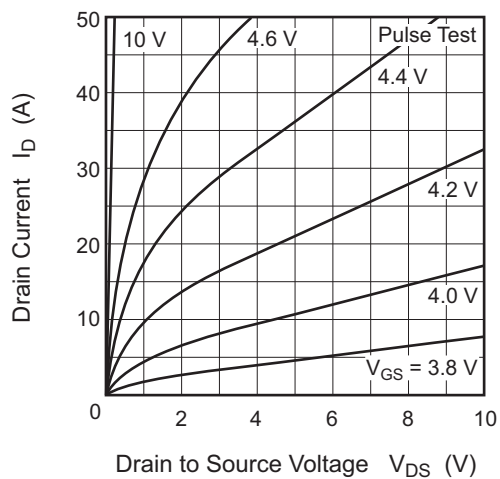
Power vs. Temperature Derating



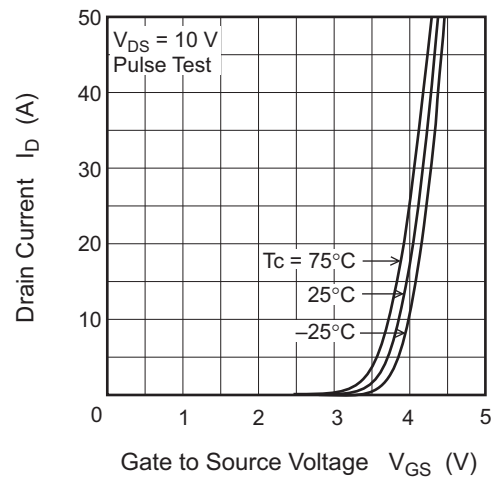
Maximum Safe Operation Area



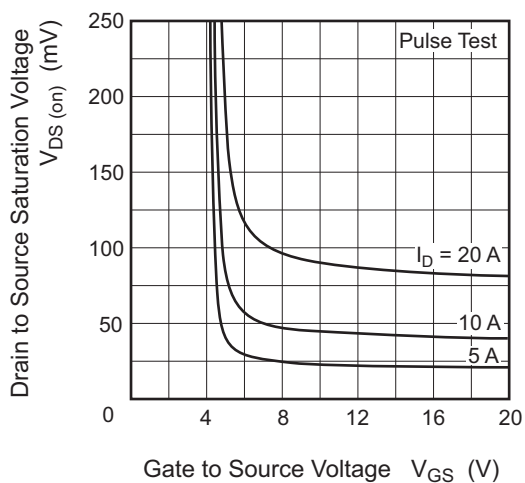
Typical Output Characteristics



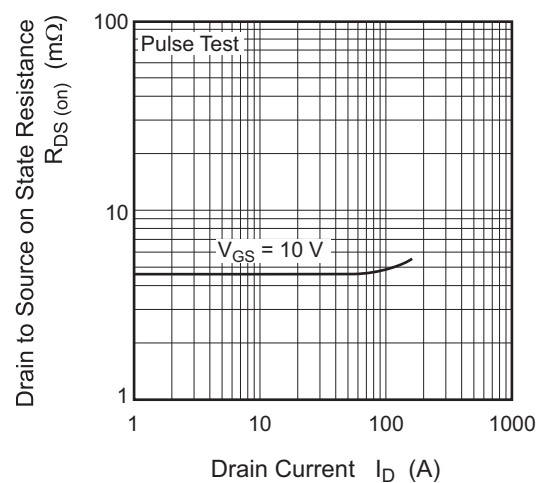
Typical Transfer Characteristics

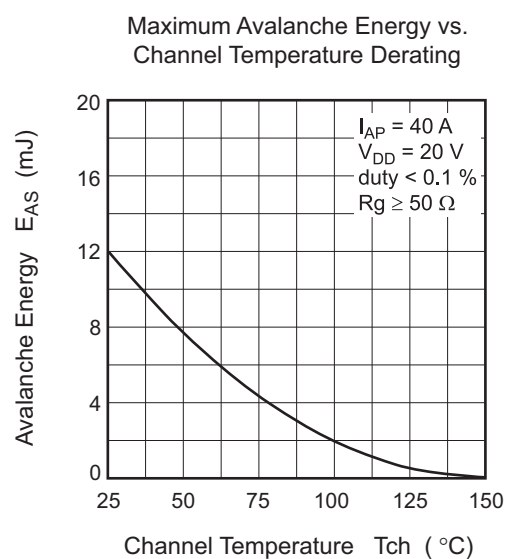
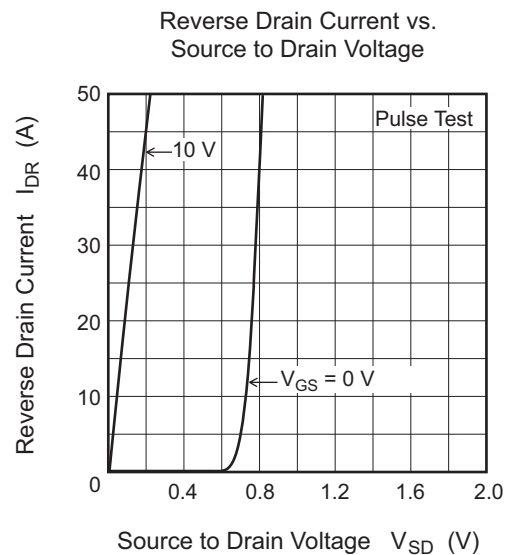
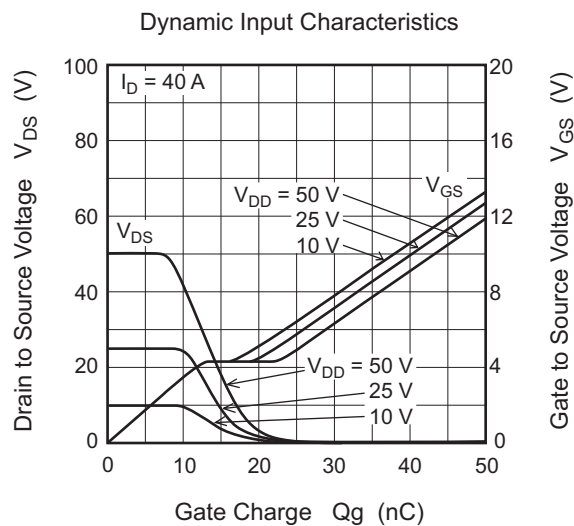
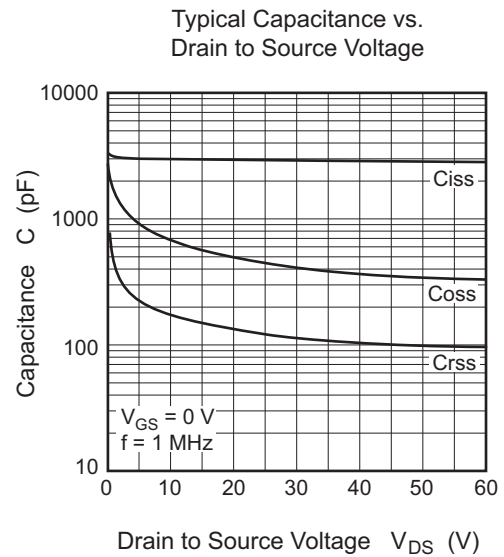
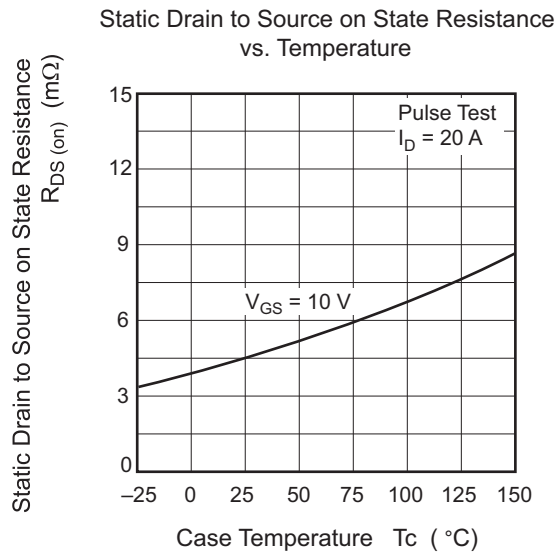


Drain to Source Saturation Voltage vs. Gate to Source Voltage

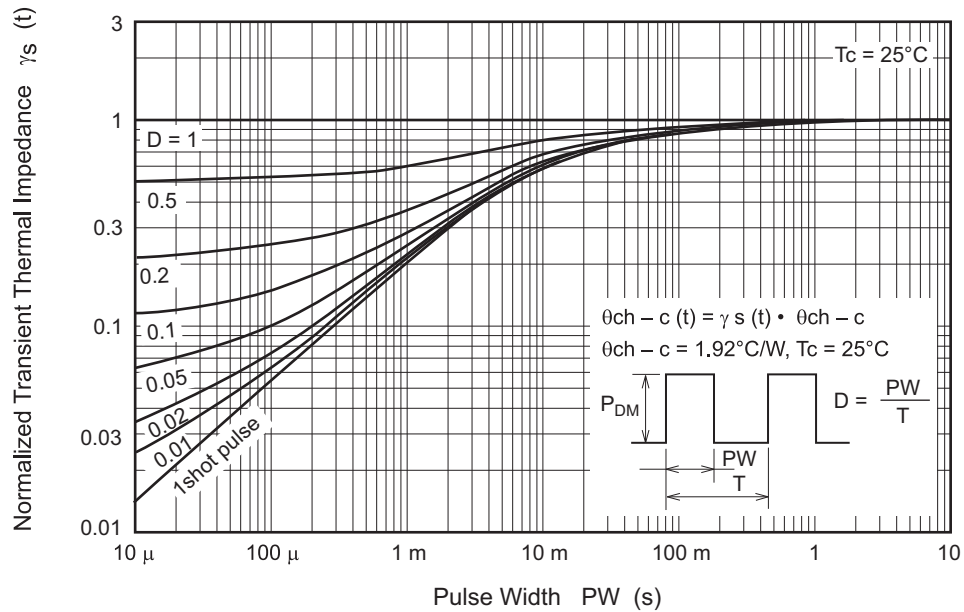


Static Drain to Source on State Resistance vs. Drain Current

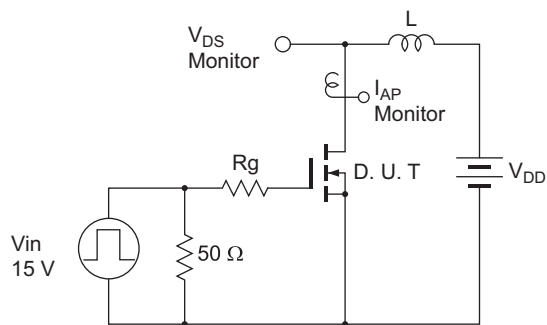




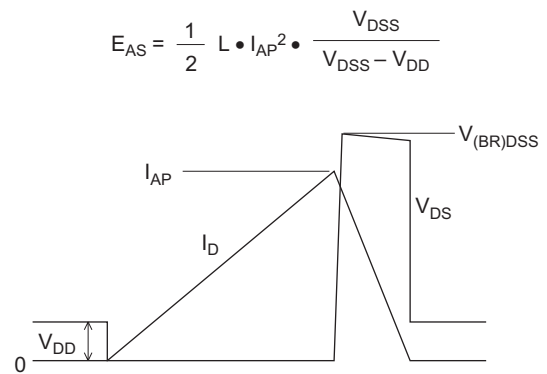
Normalized Transient Thermal Impedance vs. Pulse Width



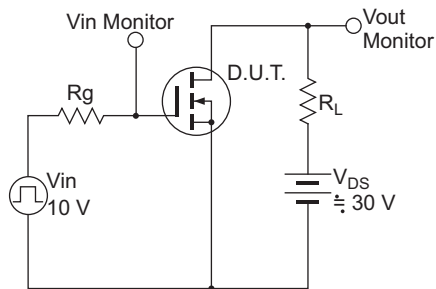
Avalanche Test Circuit



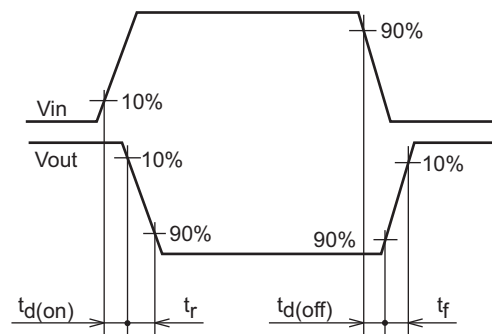
Avalanche Waveform



Switching Time Test Circuit



Switching Time Waveform





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