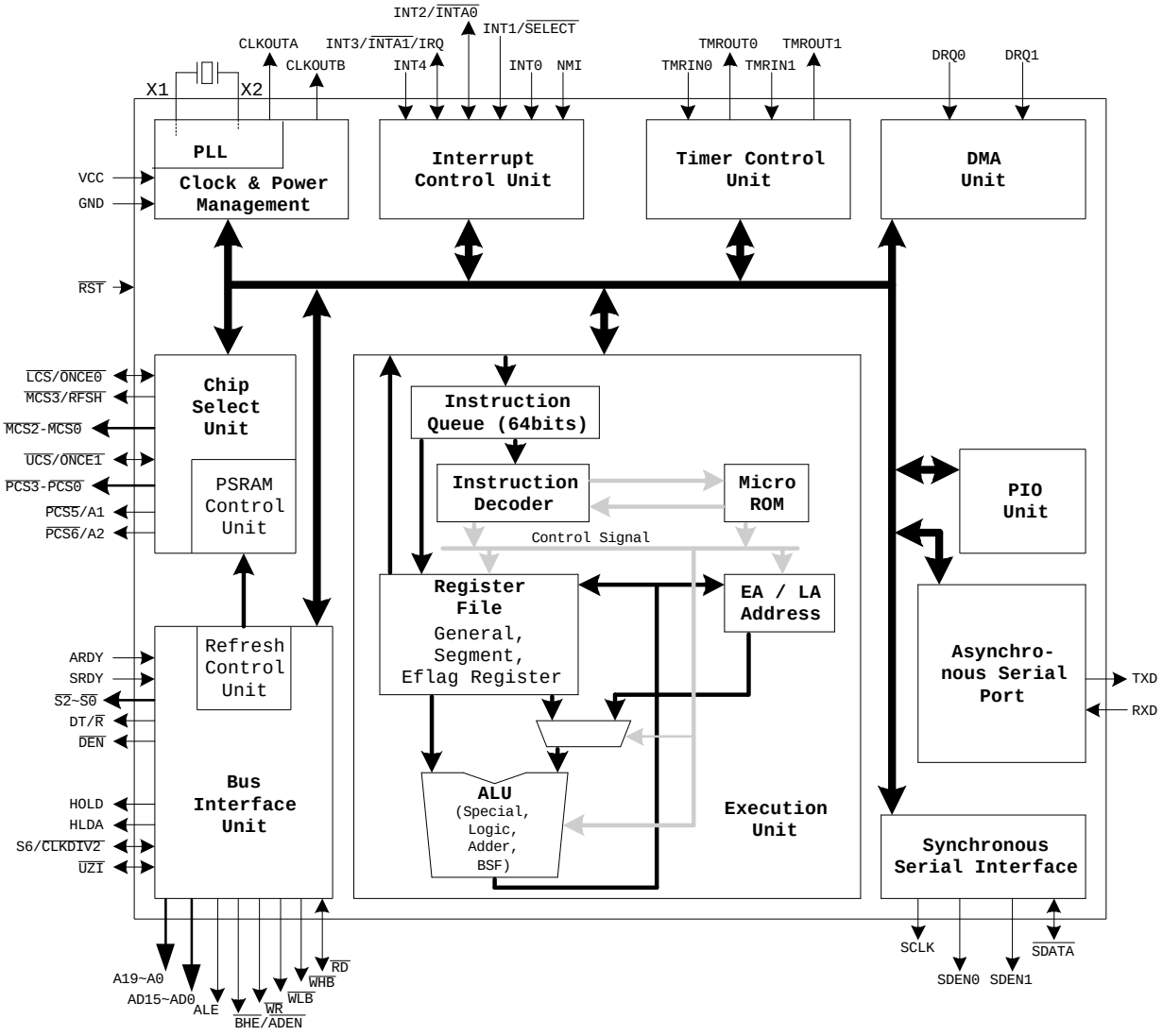
R1122I
Brief Sheet
16-BIT RISC MICROCONTROLLER

1. Features

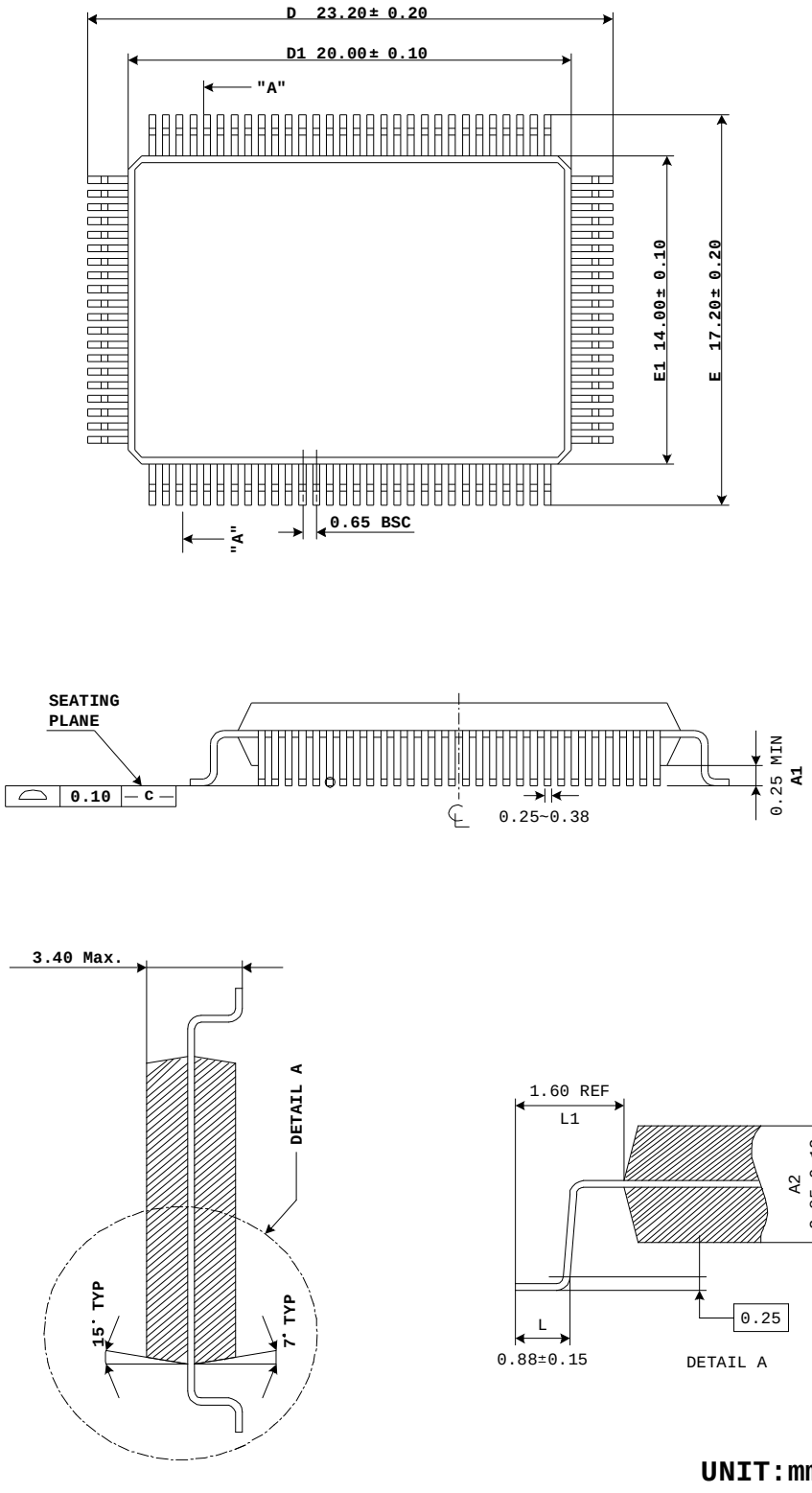
- Five-stages pipeline
- RISC architecture
- Static Design & Synthesizable design
- Integrate PLL(*1~*8)
- Maximum frequency is 40MHz, External bus, Internal bus and core are in the same clock base
- Bus interface
  - Multiplexed address and Data bus
  - Supports direct address bus [A19: A0]
  - 8-bit or 16-bit external bus dynamic access
  - 1M byte memory address space
  - 64K byte I/O space
- Software is compatible with generic 80C186 microprocessor
- Support two Asynchronous serial channels with hardware handshaking signals.
- Support CPU ID
- Supports 32 PIO pins
- Support 64kx16, 128kx16, 256kx16 EDO or FP DRAM with auto-refresh control
- Three independent 16-bit timers and one independent programmable watchdog timer
- The Interrupt controller with seven maskable external interrupts and one non-maskable external interrupt(NMI)
- Two independent DMA channels
- The I/O pin output is 3.3 volt level and the input is 3.3 volt to 5 volt tolerance
- 3.3V operation voltage
- Programmable chip-select logic for Memory or I/O bus cycle decoder
- Programmable wait-state generator
- Boot ROM bus size with 8-bit or 16-bit
- A green product
- Package Type
  - PQFP100 pins & LQFP100 pins

2. Block Diagram

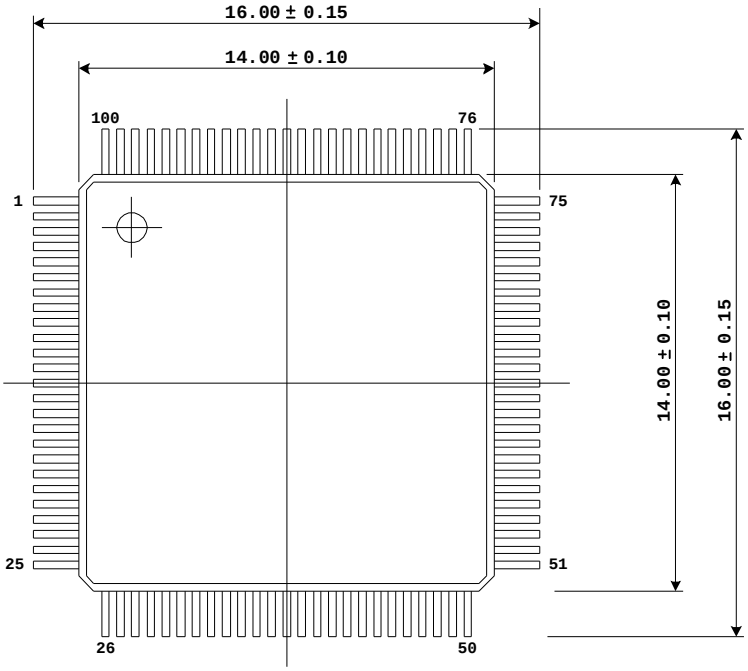


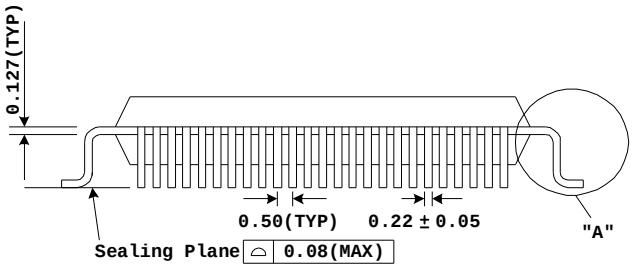
3. Package Information

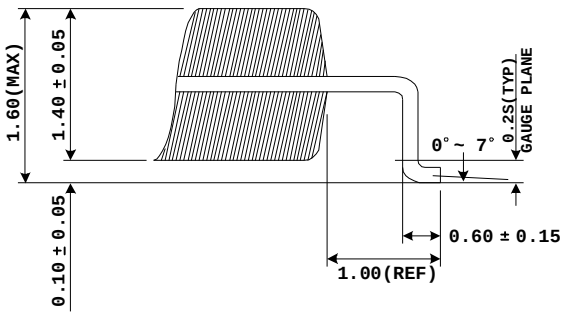
PQFP 100 pins



LQFP 100 pins







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