1A Buck-Boost DC/DC and Dual 600mA Buck DC/DC Converters

FEATURES

- **Three High Efficiency DC/DC Converters: Buck-Boost (V_{OUT}: 1.8V to 5.25V, I_{OUT}: 1A) Dual Buck (V_{OUT}: 0.6V to V_{IN}, I_{OUT}: 600mA)**
- **1.8V to 5.5V Input Voltage Range**
- **Pin-Selectable Burst Mode® Operation**
- **30µA Total Quiescent Current in Burst Mode Operation**
- Independent Power Good Indicator Outputs
- Integrated Soft-Start
- Thermal and Overcurrent Protection
- <2µA Current in Shutdown
- Small 4mm × 4mm QFN and Thermally Enhanced TSSOP Packages

APPLICATIONS

- Bar Code Readers
- Medical Instruments
- Handy Terminals
- PDAs, Handheld PCs
- GPS Receivers

DESCRIPTION

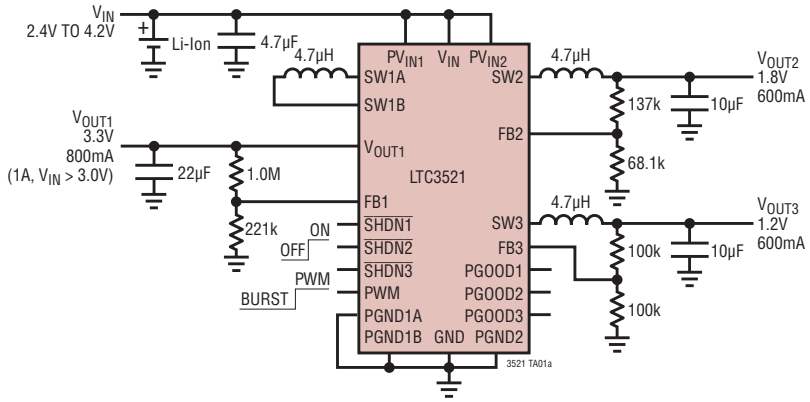
The LTC®3521 combines a 1A buck-boost DC/DC converter and dual 600mA synchronous buck DC/DC converters. The 1.1MHz switching frequency minimizes the solution footprint while maintaining high efficiency. All three converters feature soft-start and internal compensation to minimize the solution footprint and simplify the design process.

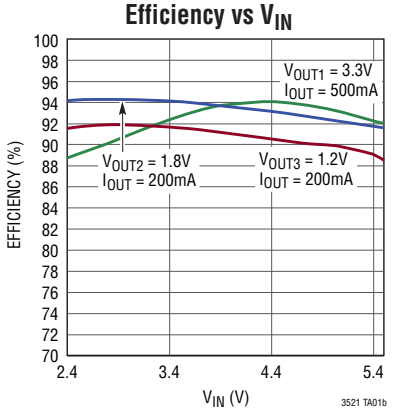
The buck converters are current mode controlled and utilize an internal synchronous rectifier to improve efficiency. The buck converters support 100% duty cycle operation to extend battery life. If the PWM pin is held low, the buck converters automatically transition from Burst Mode operation to PWM mode at high loads. With the PWM pin held high, the buck converters remain in low noise, 1.1MHz PWM mode.

The buck-boost converter features continuous conduction operation to maximize efficiency and minimize noise. At light loads, the buck-boost converter can be operated in Burst Mode operation to improve efficiency and reduce no-load standby current.

The LTC3521 provides a <2µA shutdown mode, overtemperature shutdown and current limit protection on all converters. The LTC3521 is available in a 24-pin 0.75mm × 4mm × 4mm QFN package, and a 20-pin thermally enhanced TSSOP package.

TYPICAL APPLICATION

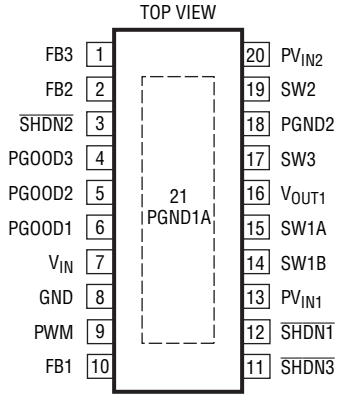




ABSOLUTE MAXIMUM RATINGS (Note 1)

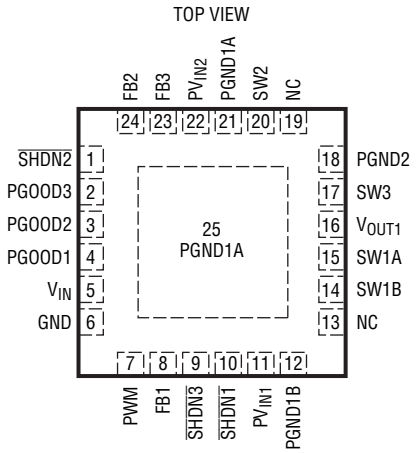
PV_{IN1}, PV_{IN2}, V_{IN} Voltage ..... –0.3V to 6V
SW1A, SW1B, SW2, SW3 Voltage
DC ..... –0.3V to 6V
Pulsed < 100ns ..... –1V to 7V
Voltage, All Other Pins ..... –0.3V to 6V
Operating Junction Temperature Range
(Notes 2, 5) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 40°C/W (NOTE 4)
UNDERSIDE METAL INTERNALLY CONNECTED TO V^- (PCB CONNECTION OPTIONAL)
EXPOSED PAD (PIN 21) IS PGND1A AND MUST BE SOLDERED TO PCB GROUND



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 25) IS PGND1A AND MUST BE SOLDERED TO PCB GROUND

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3521EFE#PBF	LTC3521EFE#TRPBF	LTC3521FE	20-Lead Plastic TSSOP	–40°C to 125°C
LTC3521IFE#PBF	LTC3521IFE#TRPBF	LTC3521FE	20-Lead Plastic TSSOP	–40°C to 125°C
LTC3521EUF#PBF	LTC3521EUF#TRPBF	3521	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3521IUF#PBF	LTC3521IUF#TRPBF	3521	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN}, PV_{IN1}, PV_{IN2} = 3.6V, V_{OUT1} = 3.3V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Voltage		●	1.8		5.5	V
Quiescent Current—Shutdown	$V_{\overline{SHDN1}}$ = $V_{\overline{SHDN2}}$ = $V_{\overline{SHDN3}}$ = 0V (Note 6)	●		0.01	2	µA
Burst Mode Quiescent Current	V_{FB1} = 0.66V, V_{FB2} = 0.66V, V_{FB3} = 0.66V, V_{PWM} = 0V			30		µA
Oscillator Frequency		●	0.85	1.1	1.35	MHz
$\overline{SHDN1}$, $\overline{SHDN2}$, $\overline{SHDN3}$, PWM Input High Voltage		●	1.4			V
$\overline{SHDN1}$, $\overline{SHDN2}$, $\overline{SHDN3}$, PWM Input Low Voltage		●			0.4	V
Power Good Outputs Low Voltage	I_{PGOOD1} = I_{PGOOD2} = I_{PGOOD3} = 1mA			0.1	0.2	V
Power Good Outputs Leakage Current	V_{PGOOD1} = V_{PGOOD2} = V_{PGOOD3} = 5.5V			0.1	10	µA
Buck Converters						
PMOS Switch Resistance				0.205		Ω
NMOS Switch Resistance				0.170		Ω
NMOS Switch Leakage Current	V_{SW2} = V_{SW3} = 5.5V, V_{IN} = 5.5V			0.1	5	µA
PMOS Switch Leakage Current	V_{SW2} = V_{SW3} = 0V, V_{IN} = 5.5V			0.1	10	µA
Feedback Voltage	(Note 4)	●	0.585	0.6	0.612	V
Feedback Input Current	V_{FB2} = V_{FB3} = 0.6V			1	50	nA
PMOS Current Limit	(Note 3)	●	750	1050		mA
Maximum Duty Cycle	V_{FB2} = V_{FB3} = 0.55V	●	100			%
Minimum Duty Cycle	V_{FB2} = V_{FB3} = 0.66V	●			0	%
PGOOD Threshold	$V_{FB2,3}$ Falling		–12	–9	–6	%
Power Good Hysteresis	$V_{FB2,3}$ Returning Good			2		%
Buck-Boost Converter						
Output Voltage		●	1.8		5.25	V
PMOS Switch Resistance				0.110		Ω
NMOS Switch Resistance				0.085		Ω
NMOS Switch Leakage Current	V_{SW1A} = V_{SW1B} = 5.5V, V_{IN} = 5.5V			0.1	5	µA
PMOS Switch Leakage Current	V_{SW1A} = V_{SW1B} = 0V, V_{IN} = 5.5V			0.1	10	µA
Feedback Voltage	(Note 4)	●	0.585	0.6	0.612	V
Feedback Input Current	V_{FB1} = 0.6V			1	50	nA
Average Current Limit	(Note 3)	●	1.65	2.1		A
Reverse Current Limit	(Note 3)			375		mA
Maximum Duty Cycle	V_{FB1} = 0.55V	●	85	94		%
Minimum Duty Cycle	V_{FB1} = 0.66V	●			0	%
PGOOD Threshold	V_{FB1} Falling		–12	–9	–6	%
Power Good Hysteresis	V_{FB1} Returning Good			3		%

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3521 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3521E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3521I is guaranteed over the full –40°C to 125°C operating junction temperature range. The maximum ambient temperature is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

ELECTRICAL CHARACTERISTICS

Note 3: Current measurements are performed when the LTC3521 is not switching. The current limit values in operation will be somewhat higher due to the propagation delay of the comparators.

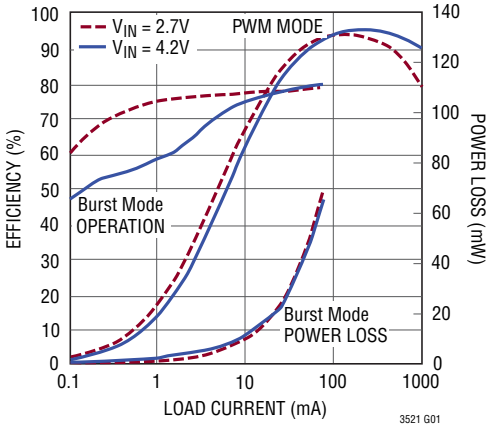
Note 4: The LTC3521 is tested in a proprietary test mode that connects each FB pin to the output of the respective error amplifier.

Note 5: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

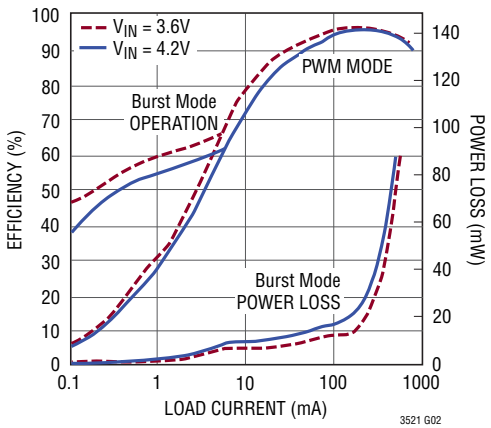
Note 6: Shutdown current is measured on the V_{IN} pin and does not include PMOS switch leakage.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

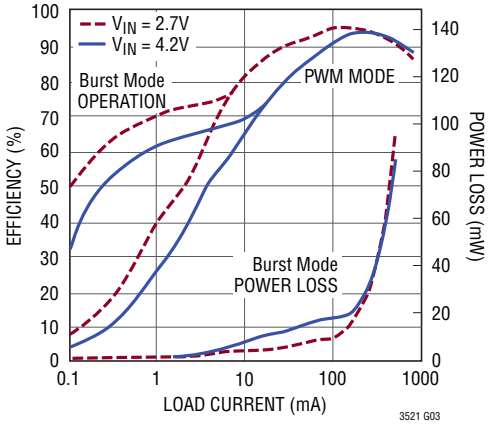
Buck-Boost Efficiency vs Load Current, Li-Ion to 3.3V



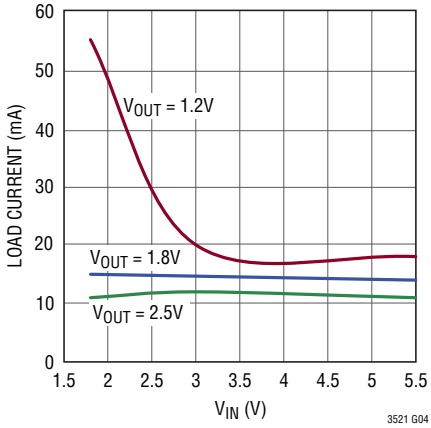
Buck Efficiency vs Load Current, Li-Ion to 2.5V



Buck Efficiency vs Load Current, Li-Ion to 1.8V

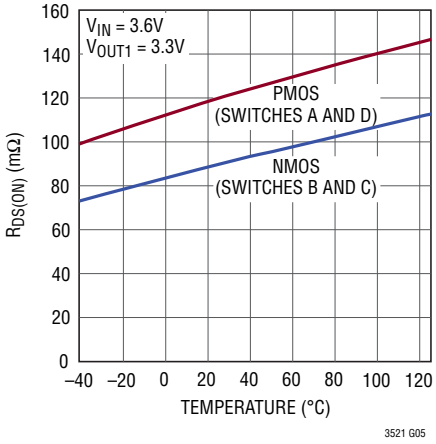


Buck Burst Mode Current Threshold vs V_{IN}

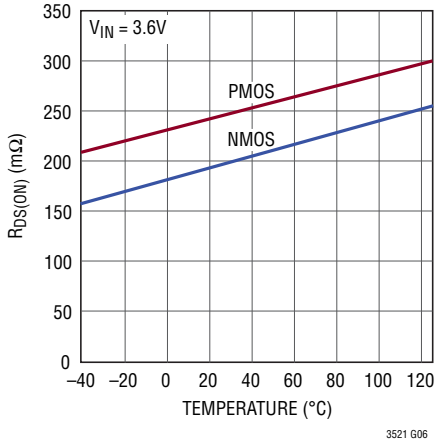


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

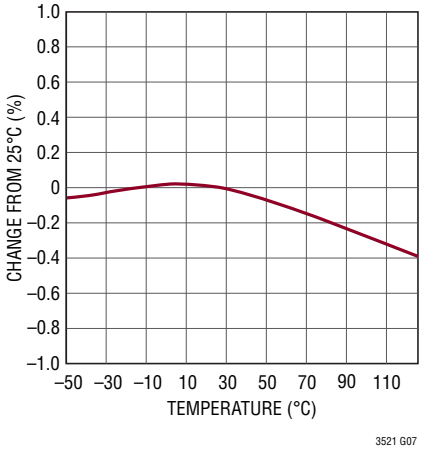
Buck-Boost Switches $R_{DS(ON)}$ vs Temperature



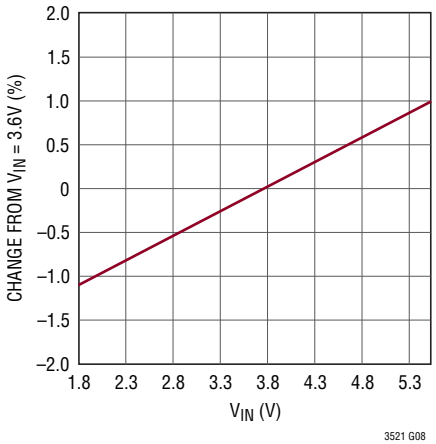
Buck Switches $R_{DS(ON)}$ vs Temperature



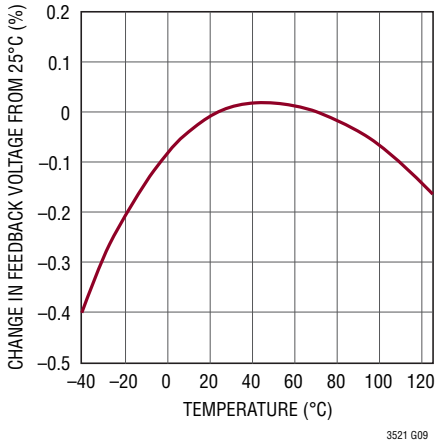
Switching Frequency vs Temperature



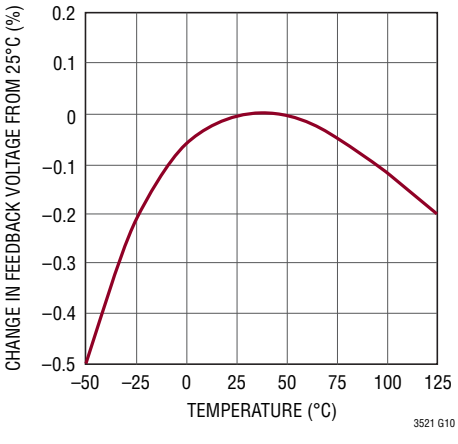
Switching Frequency vs V_{IN}



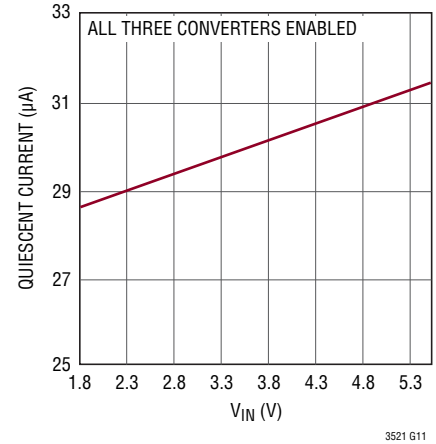
Buck-Boost Feedback Voltage vs Temperature



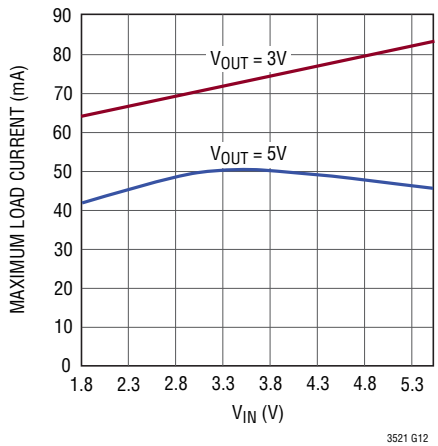
Buck Feedback Voltage vs Temperature



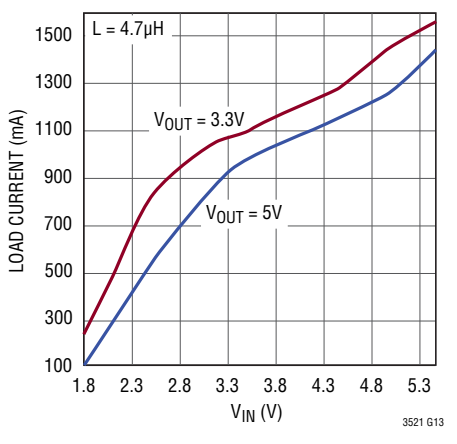
Burst Mode Quiescent Current vs V_{IN}



Buck-Boost Maximum Load Current vs V_{IN}, Burst Mode Operation

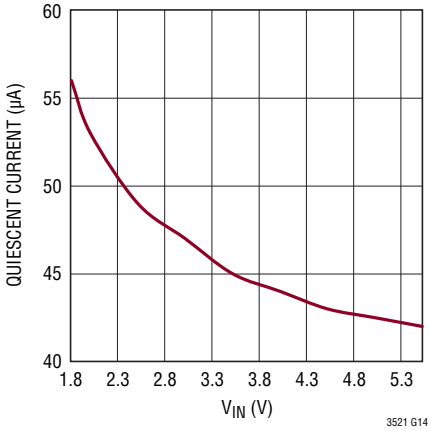


Buck-Boost Maximum Load Current vs V_{IN}, PWM Mode

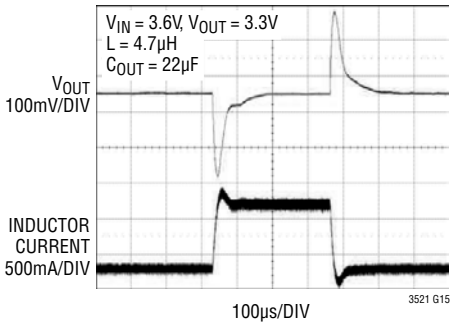


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

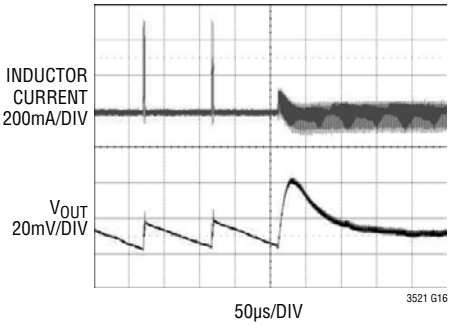
No Load Quiescent Current vs V_{IN}



Buck-Boost Load Step, 0mA to 750mA

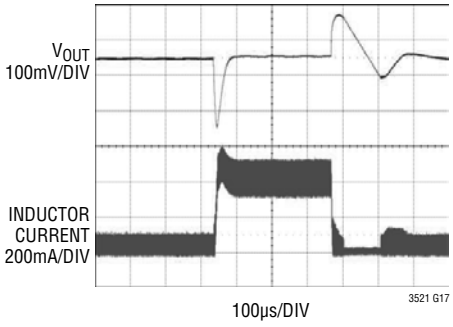


Buck-Boost Burst Mode Operation to PWM Transition



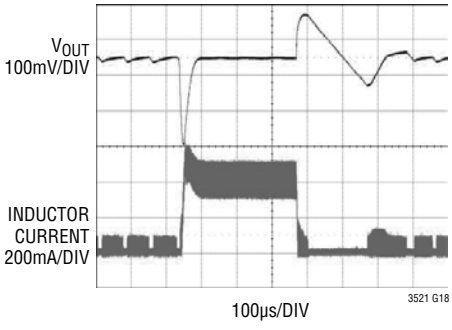
V_{IN} = 3.6V L = 4.7µH
V_{OUT} = 3.3V C_{OUT} = 22µF

Buck Load Step, PWM Mode, 10mA to 400mA



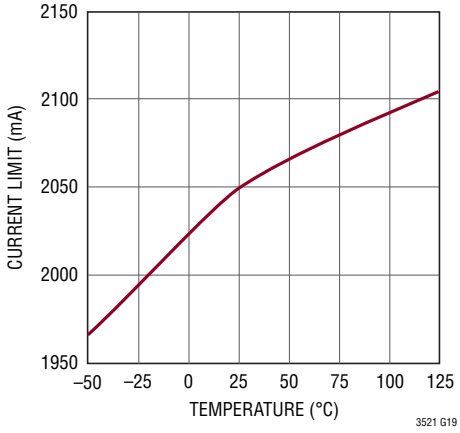
V_{IN} = 3.6V L = 4.7µH
V_{OUT} = 1.8V C_{OUT} = 10µF

Buck Load Step, Burst Mode, 10mA to 400mA

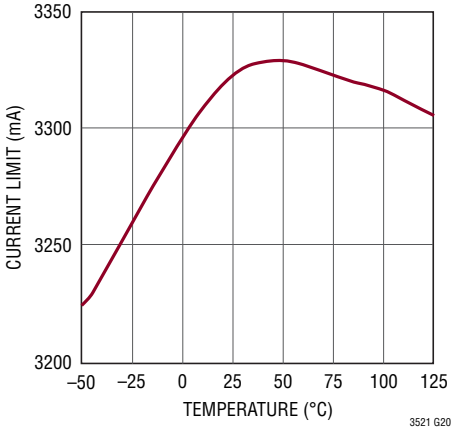


V_{IN} = 3.6V L = 4.7µH
V_{OUT} = 1.8V C_{OUT} = 10µF

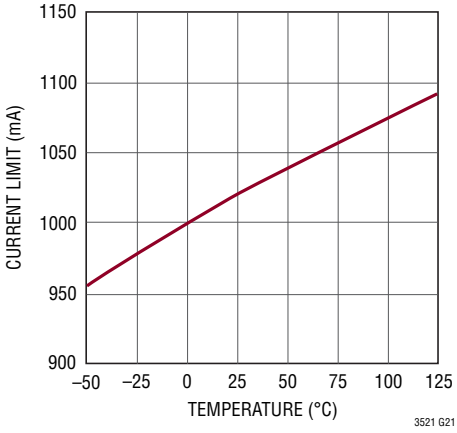
Buck-Boost Current Limit vs Temperature



Buck-Boost Peak Current Limit vs Temperature



Buck Current Limit vs Temperature



PIN FUNCTIONS (FE/UF Packages)

FB3 (Pin 1/Pin 23): Feedback Voltage for the Buck Converter Derived from a Resistor Divider Connected to the Buck V_{OUT3} Output Voltage. The buck output voltage is given by the following equation, where R1 is a resistor between FB3 and ground, and R2 is a resistor between FB3 and the buck output voltage:

$$V_{OUT3} = 0.6V\left(1+\frac{R2}{R1}\right)$$

FB2 (Pin 2/Pin 24): Feedback Voltage for the Buck Converter Derived from a Resistor Divider Connected to the Buck V_{OUT2} Output Voltage. The buck output voltage is given by the following equation, where R1 is a resistor between FB2 and ground, and R2 is a resistor between FB2 and the buck output voltage:

$$V_{OUT2} = 0.6V\left(1+\frac{R2}{R1}\right)$$

$\overline{SHDN2}$ (Pin 3/Pin 1): Forcing this pin above 1.4V enables the buck converter output at SW2. Forcing this pin below 0.4V disables the buck converter. This pin cannot be left floating.

PGOOD3 (Pin 4/Pin 2): This pin is an open-drain output which pulls low under any of the following conditions: V_{OUT3} buck output voltage is out of regulation, the part is in overtemperature shutdown, the part is in undervoltage lockout, or the $\overline{SHDN3}$ pin is pulled low.

PGOOD2 (Pin 5/Pin 3): This pin is an open-drain output which pulls low under any of the following conditions: V_{OUT2} buck output voltage is out of regulation, the part is in overtemperature shutdown, the part is in undervoltage lockout, or the $\overline{SHDN2}$ pin is pulled low.

PGOOD1 (Pin 6/Pin 4): This pin is an open-drain output which pulls low under any of the following conditions: V_{OUT1} buck-boost output voltage is out of regulation, the part is in overtemperature shutdown, the part is in undervoltage lockout, the buck-boost converter is in current limit, or the $\overline{SHDN1}$ pin is pulled low. See the Operation section of this data sheet for details on the functionality of this pin in PWM mode.

V_{IN} (Pin 7/Pin 5): Low Current Power Supply Connection Used to Power the Internal Circuitry of the LTC3521. This pin should be bypassed by a 4.7µF, or larger, ceramic capacitor. The bypass capacitor should be placed as close to the pin as possible and should have a short return path to ground. Pins V_{IN}, PV_{IN1}, and PV_{IN2} must be connected together in the application circuit.

GND (Pin 8/Pin 6): Small Signal Ground. This pin is used as a ground reference for the internal circuitry of the LTC3521.

PWM (Pin 9/Pin 7): Logic Input Used to Choose Between Burst Mode Operation and PWM Mode for All Three Converters. This pin cannot be left floating.

PWM = Low: Burst Mode operation is enabled on all three converters. The buck converters will operate in Burst Mode operation at light current but will automatically transition to PWM operation at high currents. The buck converters can supply maximum output current (600mA) in this mode. The buck-boost converter will operate in variable frequency mode and can only supply a reduced load current (typically 50mA).

PWM = High: All three converters are forced into PWM mode operation. The buck converters will remain at constant-frequency operation until their minimum on-time is reached. The buck-boost converter will remain in PWM mode at all load currents.

FB1 (Pin 10/Pin 8): Feedback Voltage for the Buck-Boost Converter Derived from a Resistor Divider on the Buck-Boost Output Voltage. The buck-boost output voltage is given by the following equation, where R1 is a resistor between FB1 and ground, and R2 is a resistor between FB1 and the buck output voltage:

$$V_{OUT1} = 0.6V\left(1+\frac{R2}{R1}\right)$$

$\overline{SHDN3}$ (Pin 11/Pin 9): Forcing this pin above 1.4V enables the buck converter output at SW3. Forcing this pin below 0.4V disables the buck converter. This pin cannot be left floating.

$\overline{SHDN1}$ (Pin 12/Pin 10): Forcing this pin above 1.4V enables the buck-boost converter. Forcing this pin below 0.4V disables the buck-boost converter. This pin cannot be left floating.

PIN FUNCTIONS (FE/UF Packages)

PV_{IN1} (Pin 13/Pin 11): High current power supply connection used to supply switch A of the buck-boost converter. This pin should be bypassed by a 4.7µF, or larger, ceramic cap. The bypass capacitor should be placed as close to the pin as possible and should have a short return path to ground. Pins V_{IN}, PV_{IN1}, and PV_{IN2} must be connected together in the application circuit.

NC (Pin 13, UF Package Only): No Internal Connection.

SW1B (Pin 14/Pin 14): Buck-Boost Switch Node. This pin must be connected to one side of the buck-boost inductor.

SW1A (Pin 15/Pin 15): Buck-Boost Switch Node. This pin must be connected to one side of the buck-boost inductor.

V_{OUT1} (Pin 16/Pin 16): Buck-Boost Output Voltage Node. This pin should be connected to a low ESR ceramic capacitor. The capacitor should be placed as close to the IC as possible and should have a short return to ground.

SW3 (Pin 17/Pin 17): Buck converter Switch Node. This pin must be connected to the opposite side of the inductor connected to V_{OUT3}.

PGND2 (Pin 18/Pin 18): High Current Ground Connection for Both Buck Converters. The PCB trace connecting this pin to ground should be made as short and wide as possible.

SW2 (Pin 19/Pin 20): Buck Converter Switch Node. This pin must be connected to the opposite side of the inductor connected to V_{OUT2}.

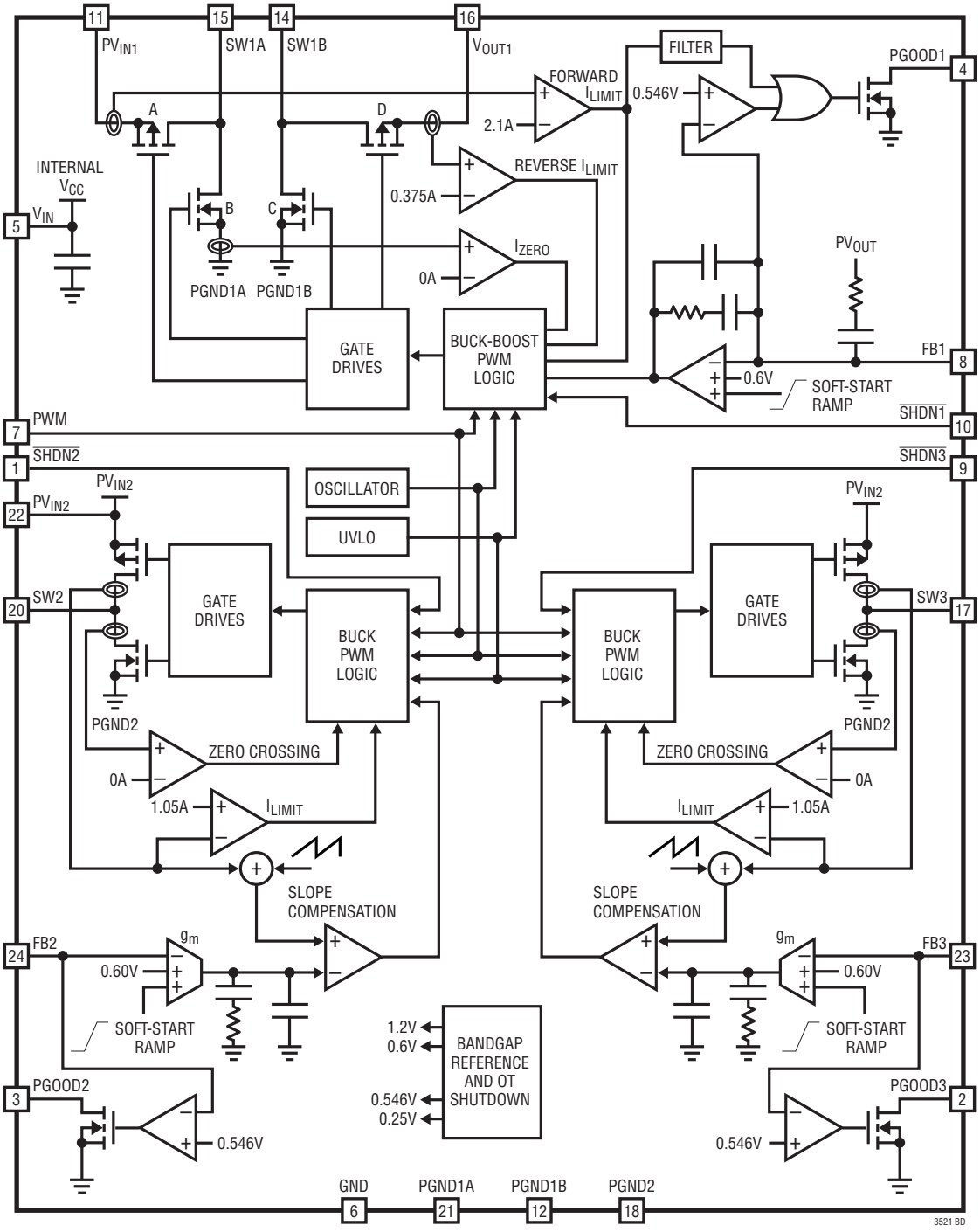
NC (Pin 19, UF Package Only): No Internal Connection.

PV_{IN2} (Pin 20/Pin 22): High Current Power Supply Connection Used to Supply the Buck Converter Power Switches. This pin should be bypassed by a 10µF or larger ceramic cap. The bypass capacitor should be placed as close to the pin as possible and should have a short return path to ground. Pins V_{IN}, PV_{IN1}, and PV_{IN2} must be connected together in the application circuit.

PGND1A (Exposed Pad Pin 21/Pin 21, Exposed Pad Pin 25): High Current Ground Connection for the Buck-Boost Switch B. The PCB trace connecting this pin to ground should be made as short and wide as possible.

PGND1B (Pin 12, UF Package Only): High Current Ground Connection for the Buck-Boost Switch C. The PCB trace connecting this pin to ground should be made as short and wide as possible.

BLOCK DIAGRAM (UF Package)



OPERATION

The LTC3521 combines dual synchronous buck DC/DC converters and a 4-switch buck-boost DC/DC converter in a 4mm × 4mm QFN package and a 20-pin thermally enhanced TSSOP package. The buck-boost converter utilizes a proprietary switching algorithm which allows its output voltage to be regulated above, below or equal to the input voltage. The buck converters provide a high efficiency lower voltage output and support 100% duty cycle operation to extend battery life. In Burst Mode operation, the total quiescent current for the LTC3521 is reduced to 30µA. All three converters are synchronized to the same internal 1.1MHz oscillator.

BUCK CONVERTER OPERATION

PWM Mode Operation

When the PWM pin is held high, the LTC3521 buck converters use a constant-frequency, current mode control architecture. Both the main (P-channel MOSFET) and synchronous rectifier (N-channel MOSFET) switches are internal. At the start of each oscillator cycle, the P-channel switch is turned on and remains on until the current waveform with superimposed slope compensation ramp exceeds the error amplifier output. At this point, the synchronous rectifier is turned on and remains on until the inductor current falls to zero or a new switching cycle is initiated. As a result, the buck converters operate with discontinuous inductor current at light loads, which improves efficiency. At extremely light loads, the minimum on-time of the main switch will be reached and the buck converters will begin turning off for multiple cycles in order to maintain regulation.

Burst Mode Operation

When the PWM pin is forced low, the buck converters will automatically transition between Burst Mode operation at sufficiently light loads (below approximately 15mA) and PWM mode at heavier loads. Burst Mode entry is determined by the peak inductor current. Therefore, the load current at which Burst Mode operation will be entered depends on the input voltage, the output voltage and the inductor value. Typical curves for Burst Mode entry threshold are provided in the Typical Performance Characteristics section of this data sheet. In dropout and near dropout conditions, Burst Mode operation is disabled.

Dropout Operation

As the input voltage decreases to a value approaching the output regulation voltage, the duty cycle increases toward the maximum on-time. Further reduction of the supply voltage will force the main switch to remain on for more than one cycle until 100% duty cycle operation is reached where the main switch remains on continuously. In this dropout state, the output will be determined by the input voltage less the resistive voltage drop across the main switch and series resistance of the inductor.

Slope Compensation

Current mode control requires the use of slope compensation to prevent subharmonic oscillations in the inductor current at high duty cycle operation. This is accomplished internally on the LTC3521 through the addition of a compensating ramp to the current sense signal. In some current mode ICs, current limiting is performed by clamping the error amplifier voltage to a fixed maximum. This leads to a reduced output current capability at low step-down ratios. In contrast, the LTC3521 performs current limiting prior to addition of the slope compensation ramp and therefore achieves a peak inductor current limit that is independent of duty cycle.

Short-Circuit Protection

When the output is shorted to ground, the error amplifier will saturate high and the P-channel MOSFET switch will turn on at the start of each cycle and remain on until the current limit trips. During this minimum on-time, the inductor current will increase rapidly and will decrease very slowly during the remainder of the period due to the very small reverse voltage produced by a hard output short. To eliminate the possibility of inductor current runaway in this situation, the buck converter switching frequency is reduced to 250kHz when the voltage on the buck FB pin falls below 0.25V. The buck soft-start circuit is reset when the buck FB pin falls below 0.25V to provide a smooth restart once the short-circuit condition at the output voltage is no longer present. Additionally, the PMOS current limit is decreased from 1050mA to 700mA when the voltage on the buck FB pin falls below 0.25V.

OPERATION

Soft-Start

The buck converters have an internal voltage mode soft-start circuit with a nominal duration of 800µs. The converters remain in regulation during soft-start and will therefore respond to output load transients which occur during this time. In addition, the output voltage rise time has minimal dependency on the size of the output capacitor or load current.

Error Amplifier and Compensation

The LTC3521 buck converters utilize an internal transconductance error amplifier. Compensation of the feedback loop is performed internally to reduce the size of the application circuit and simplify the design process. The compensation network has been designed to allow use of a wide range of output capacitors while simultaneously ensuring rapid response to load transients.

PGOOD Comparators

The PGOOD2 and PGOOD3 pins are open-drain outputs which indicate the status of the buck converters. If the buck output voltage falls 9% below the regulation voltage, the respective PGOOD open-drain output will pull low. The output voltage must rise 2% above the falling threshold before the pull-down will turn off. In addition, there is a 60µs typical deglitching delay in the flag in order to prevent false trips due to voltage transients on load steps. The respective PGOOD output will also pull low during overtemperature shutdown, undervoltage lockout or if the respective buck converter $\overline{SHDN}$ pin is pulled low to indicate these fault conditions.

BUCK-BOOST CONVERTER OPERATION

PWM Mode Operation

When the PWM pin is held high, the LTC3521 buck-boost converter operates in a constant-frequency PWM mode with voltage mode control. A proprietary switching algorithm allows the converter to switch between buck, buck-boost and boost modes without discontinuity in inductor current or loop characteristics. The switch topology for the buck-boost converter is shown in Figure 1.

When the input voltage is significantly greater than the output voltage, the buck-boost converter operates in buck mode. Switch D turns on continuously and switch C remains off. Switches A and B are pulse width modulated to produce the required duty cycle to support the output regulation voltage. As the input voltage decreases, switch A remains on for a larger portion of the switching cycle. When the duty cycle reaches approximately 85%, the switch pair AC begins turning on for a small fraction of the switching period. As the input voltage decreases further, the AC switch pair remains on for longer durations and the duration of the BD phase decreases proportionally. As the input voltage drops below the output voltage, the AC phase will eventually increase to the point that there is no longer any BD phase. At this point, switch A remains on continuously while switch pair CD is pulse width modulated to obtain the desired output voltage. At this point, the converter is operating solely in boost mode.

This switching algorithm provides a seamless transition between operating modes and eliminates discontinuities in average inductor current, inductor current ripple and loop transfer function throughout all three operational

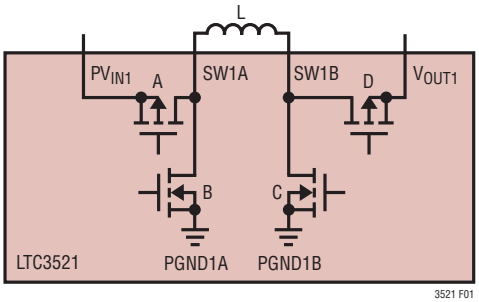


Figure 1. Buck-Boost Switch Topology

OPERATION

modes. These advantages result in increased efficiency and stability in comparison to the traditional 4-switch buck-boost converter.

Error Amplifier and Compensation

The buck-boost converter utilizes a voltage mode error amplifier with an internal compensation network as shown in Figure 2.

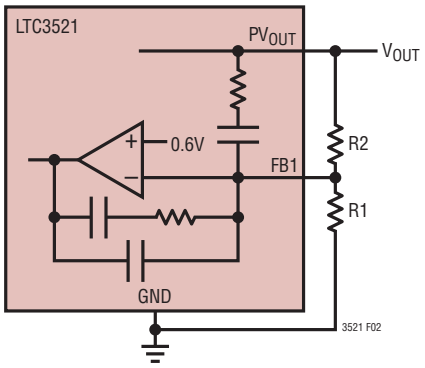


Figure 2. Buck-Boost Error Amplifier and Compensation

Notice that resistor R2 of the external resistor divider network plays an integral role in determining the frequency response of the compensation network. The ratio of R2 to R1 must be set to program the desired output voltage but this still allows the value of R2 to be adjusted to optimize the transient response of the converter. Increasing the value of R2 generally leads to greater stability at the expense of reduced transient response speed. Increasing the value of R2 can yield substantial transient response improvement in cases where the phase margin has been reduced due to the use of a small value output capacitor or a large inductance (particularly with large boost step-up ratios). Conversely, decreasing the value of R2 increases the loop bandwidth which can improve the speed of the converter's transient response. This can be useful in improving the transient response if a large valued output capacitor is utilized. In this case, the increased bandwidth created by decreasing R2 is used to counteract the reduced converter bandwidth caused by the large output capacitor.

Current Limit Operation

The buck-boost converter has two current limit circuits. The primary current limit is an average current limit circuit which injects an amount of current into the feedback node which is proportional to the extent that the switch A current exceeds the current limit value. Due to the high gain of this loop, the injected current forces the error amplifier output to decrease until the average current through switch A decreases approximately to the current limit value. The average current limit utilizes the error amplifier in an active state and thereby provides a smooth recovery with little overshoot once the current limit fault condition is removed. Since the current limit is based on the average current through switch A, the peak inductor current in current limit will have a dependency on the duty cycle (i.e., on the input and output voltages in the overcurrent condition).

The speed of the average current limit circuit is limited by the dynamics of the error amplifier. On a hard output short, it would be possible for the inductor current to increase substantially beyond current limit before the average current limit circuit would react. For this reason, there is a second current limit circuit which turns off switch A if the current ever exceeds approximately 165% of the average current limit value. This provides additional protection in the case of an instantaneous hard output short.

Reverse Current Limit

The reverse current comparator on switch D monitors the inductor current entering PV_{OUT}. When this current exceeds 375mA (typical), switch D will be turned off for the remainder of the switching cycle.

OPERATION

Burst Mode Operation

With the PWM pin held low, the buck-boost converter operates utilizing a variable frequency switching algorithm designed to improve efficiency at light load and reduce the standby current at zero load. In Burst Mode operation, the inductor is charged with fixed peak amplitude current pulses. These current pulses are repeated as often as necessary to maintain the output regulation voltage. The maximum output current which can be supplied in Burst Mode operation is dependent upon the input and output voltage as given by the following formula:

$$I_{OUT(MAX),BURST} = \frac{0.1 \bullet V_{IN}}{V_{IN} + V_{OUT}} (A)$$

In Burst Mode operation, the error amplifier is not used but is instead placed in a low current standby mode to reduce supply current and improve light load efficiency.

Soft-Start

The buck-boost converter has an internal voltage mode soft-start circuit with a nominal duration of 600µs. The converter remains in regulation during soft-start and will therefore respond to output load transients that occur during this time. In addition, the output voltage rise time has minimal dependency on the size of the output capacitor or load. During soft-start, the buck-boost converter is forced into PWM operation regardless of the state of the PWM pin.

PGOOD Comparator

The PGOOD1 pin is an open-drain output which indicates the status of the buck-boost converter. In Burst Mode operation (PWM = Low), the PGOOD1 open-drain output will pull low when the feedback voltage falls 9% below the regulation voltage. There is approximately 3% hysteresis in this threshold when the output voltage is returning good. In addition, there is a 60µs typical deglitching delay to prevent false trips due to short duration voltage transients in response to load steps.

In PWM mode, operation of the PGOOD1 comparator is complicated by the fact that the feedback pin voltage is driven to the reference voltage independent of the output voltage through the action of the voltage mode error amplifier. Since the soft-start is voltage mode, the feedback voltage will track the output voltage correctly during soft-start, and the PGOOD1 output will correctly indicate the point at which the buck-boost attains regulation at the end of soft-start. Therefore, the PGOOD1 output can be utilized for sequencing purposes. Once in regulation, the feedback voltage will no longer track the output voltage, and the PGOOD1 pin will not directly respond to a loss of regulation in the output. However, the only means by which a loss of regulation can occur is if the current limit has been reached, thereby preventing the buck-boost converter from delivering the required output current. In such cases, the occurrence of current limit will cause the PGOOD1 flag to fall indicating a fault state. There can be cases, however, when the buck-boost converter is continuously in current limit, causing the PGOOD1 output to pull low, while the output voltage still remains slightly above the PGOOD1 comparator trip point.

The PGOOD1 output also pulls low during overtemperature shutdown, undervoltage lockout or if the $\overline{SHDN1}$ pin is pulled low.

COMMON FUNCTIONS

Thermal Shutdown

If the die temperature exceeds 150°C, all three converters will be disabled. All power devices will be turned off and all switch nodes will be high impedance. The soft-start circuits for all three converters are reset during thermal shutdown to provide a smooth recovery once the overtemperature condition is eliminated. All three converters will restart (if enabled) when the die temperature drops to approximately 140°C.

Undervoltage Lockout

If the supply voltage decreases below 1.7V (typical) then all three converters will be disabled and all power devices will be turned off. The soft-start circuits for all three converters are reset during undervoltage lockout to provide a smooth restart once the input voltage rises above the undervoltage lockout threshold.

APPLICATIONS INFORMATION

The basic LTC3521 application circuit is shown as the Typical Application on the front page of this data sheet. The external component selection is determined by the desired output voltages, output currents and ripple voltage requirements of each particular application. Basic guidelines and considerations for the design process are provided in this section.

Buck Inductor Selection

The choice of buck inductor value influences both the efficiency and the magnitude of the output voltage ripple. Larger inductance values will reduce inductor current ripple and lead to lower output voltage ripple. For a fixed DC resistance, a larger value inductor will yield higher efficiency by lowering the peak current closer to the average. However, a larger inductor within the same family will generally have a greater series resistance, thereby offsetting this efficiency advantage.

Given a desired peak-to-peak current ripple, ΔI_L, the required inductance can be calculated via the following expression, where f represents the switching frequency in MHz:

$$L = \frac{1}{f\Delta I_L} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)(\mu H)$$

A reasonable choice for ripple current is ΔI_L = 240mA which represents 40% of the maximum 600mA load current. The DC current rating of the inductor should be at least equal to the maximum load current, plus half the ripple current, in order to prevent core saturation and loss of efficiency during operation. To optimize efficiency, the inductor should have a low series resistance.

In particularly space-restricted applications, it may be advantageous to use a much smaller value inductor at the expense of larger ripple current. In such cases, the converter will operate in discontinuous conduction for a wider range of output loads and efficiency will be reduced. In addition, there is a minimum inductor value required to maintain stability of the current loop (given the fixed internal slope compensation). Specifically, if the buck converter is going to be utilized at duty cycles over 40%, the inductance value must be at least L_{MIN}, as given by the following equation:

$$L_{MIN} = 2.5 \bullet V_{OUT}\ (\mu H)$$

Table 1 depicts the recommended inductance for several common output voltages.

Table 1. Buck Recommended Inductance

OUTPUT VOLTAGE	MINIMUM INDUCTANCE	MAXIMUM INDUCTANCE
0.6V	1.5µH	2.2µH
1.2V	2.2µH	4.7µH
1.8V	3.3µH	6.8µH
2.5V	4.7µH	8.2µH

Buck Output Capacitor Selection

A low ESR output capacitor should be utilized at the buck output in order to minimize voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have low ESR and are available in small footprints. In addition to controlling the ripple magnitude, the value of the output capacitor also sets the loop crossover frequency and can, therefore, impact loop stability. There is both a minimum and maximum capacitance value required to ensure stability of the loop. If the output capacitance is too small, the loop crossover frequency will increase to the point where the switching delay and the high frequency parasitic poles of the error amplifier will degrade the phase margin. In addition, the wider bandwidth produced by a small output capacitor will make the loop more susceptible to switching noise. At the other extreme, if the output capacitor is too large, the crossover frequency can decrease too far below the compensation zero and lead to a degraded phase margin. Table 2 provides a guideline for the range of allowable values of low ESR output capacitors. Larger value output capacitors can be accommodated provided they have sufficient ESR to stabilize the loop.

Table 2. Buck Output Capacitor Range

V_{OUT}	C_{MIN}	C_{MAX}
0.6V	15µF	300µF
0.8V	15µF	230µF
1.2V	10µF	150µF
1.8V	10µF	90µF
2.7V	10µF	70µF
3.3V	6.8µF	50µF

APPLICATIONS INFORMATION

Buck Input Capacitor Selection

The PV_{IN2} pin provides current to the buck converter power switch and is the supply pin for the IC's internal circuitry. It is recommended that a low ESR ceramic capacitor with a value of at least 4.7µF be used to bypass this pin. The capacitor should be placed as close to the pin as possible and have a short return to ground.

Buck Output Voltage Programming

The output voltage is set by a resistive divider, according to the following formula:

$$V_{OUT2,3} = 0.6V\left(1+\frac{R2}{R1}\right)$$

The external divider is connected to the output, as shown in Figure 3. It is recommended that a feedforward capacitor, C_{FF}, be placed in parallel with resistor R2 to improve the noise immunity of the feedback node. Table 3 provides the recommended resistor and feedforward capacitor combinations for common output voltage options.

Table 3. Buck Resistor Divider Values

V_{OUT}	R1	R2	C_{FF}
0.6V	–	0	–
0.8V	200k	69.8k	22pF
1.0V	118k	80.6k	22pF
1.2V	100k	102k	22pF
1.5V	78.7k	121k	22pF
1.8V	68.1k	137k	22pF
2.7V	63.4k	226k	33pF
3.3V	60.4k	274k	33pF

Buck-Boost Output Voltage Programming

The buck-boost output voltage is set by a resistive divider according to the following formula:

$$V_{OUT1} = 0.6V\left(1+\frac{R2}{R1}\right)$$

The external divider is connected to the output, as shown in Figure 4. The buck-boost converter utilizes voltage mode control and the value of R2 plays an integral role in the dynamics of the feedback loop. In general, a larger value for R2 will increase stability and reduce the speed of the transient response. A smaller value of R2 will reduce stability but increase the transient response speed. A good starting point is to choose R2 = 1MΩ, then calculate the required value of R1 to set the desired output voltage according to the above formula. If a large output capacitor is used, the bandwidth of the converter is reduced. In such cases R2 can be reduced to improve the transient response. If a large inductor or small output capacitor is utilized, the loop will be less stable and the phase margin can be improved by increasing the value of R2.

Buck-Boost Inductor Selection

To achieve high efficiency, a low ESR inductor should be utilized for the buck-boost converter. The inductor must have a saturation rating greater than the worst case average inductor current plus half the ripple current. The peak-to-peak inductor current ripple will be larger in buck and boost mode than in the buck-boost region. The peak-to-peak inductor current ripple for each mode can

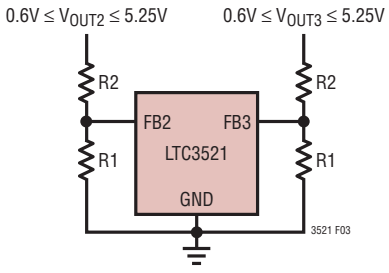


Figure 3. Setting the Buck Output Voltage

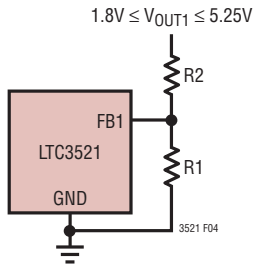


Figure 4. Setting the Buck-Boost Output Voltage

APPLICATIONS INFORMATION

be calculated from the following formulas, where f is the frequency in MHz and L is the inductance in µH:

$$\Delta I_{L,P-P,BUCK} = \frac{1}{fL} \bullet \frac{V_{OUT}(V_{IN} - V_{OUT})}{V_{IN}}$$

$$\Delta I_{L,P-P,BOOST} = \frac{1}{fL} \bullet \frac{V_{IN}(V_{OUT} - V_{IN})}{V_{OUT}}$$

In addition to affecting output current ripple, the size of the inductor can also affect the stability of the feedback loop. In boost mode, the converter transfer function has a right half plane zero at a frequency that is inversely proportional to the value of the inductor. As a result, a large inductor can move this zero to a frequency that is low enough to degrade the phase margin of the feedback loop. It is recommended that the chosen inductor value be less than 10µH if the buck-boost converter is to be used in the boost region.

Buck-Boost Output Capacitor Selection

A low ESR output capacitor should be utilized at the buck-boost converter output in order to minimize output voltage ripple. Multilayer ceramic capacitors are an excellent choice as they have low ESR and are available in small footprints. The capacitor should be chosen large enough to reduce the output voltage ripple to acceptable levels. Neglecting the capacitor ESR and ESL, the peak-to-peak output voltage ripple can be calculated by the following formulas, where f is the frequency in MHz, C_{OUT} is the capacitance in µF, L is the inductance in µH and I_{LOAD} is the output current in amps:

$$\Delta V_{P-P,BOOST} = \frac{I_{LOAD}(V_{OUT} - V_{IN})}{C_{OUT} \bullet V_{OUT} \bullet f}$$

$$\Delta V_{P-P,BUCK} = \frac{1}{8 \bullet L \bullet C_{OUT} \bullet f^2} \bullet \frac{(V_{IN} - V_{OUT})V_{OUT}}{V_{IN}}$$

Since the output current is discontinuous in boost mode, the ripple in this mode will generally be much larger than the magnitude of the ripple in buck mode. In addition to controlling the ripple magnitude, the value of the output capacitor also affects the location of the resonant frequency in the open loop converter transfer function. If the output capacitor is too small, the bandwidth of the converter will extend high enough to degrade the phase margin. To prevent this from happening, it is recommended that a minimum value of 10µF be used for the buck-boost output capacitor.

Buck-Boost Input Capacitor Selection

The supply current to the buck-boost converter is provided by the PV_{IN1} pin. It is recommended that a low ESR ceramic capacitor with a value of at least 4.7µF be located as close to this pin as possible.

Inductor Style and Core Material

Different inductor core materials and styles have an impact on the size and price of an inductor at any given peak current rating. Toroid or shielded pot cores in ferrite or permalloy materials are small and reduce emissions, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of inductor style depends upon the price, sizing, and EMI requirements of a particular application. Table 4 provides a sampling of inductors that are well suited to many LTC3521 application circuits.

Table 4. Representative Surface Mount Inductors

MANUFACTURER	PART NUMBER	VALUE	MAX CURRENT	DCR	HEIGHT
Taiyo Yuden	NP03SB4R7M	4.7µH	1.2A	0.047Ω	1.8mm
	NP03SB6R8M	6.8µH	1A	0.084Ω	1.8mm
Coilcraft	MSS7341-502NL	5µH	2.3A	0.024Ω	4.1mm
	DT1608C-472ML	4.7µH	1.2A	0.085Ω	2.92mm
Cooper-Bussmann	SD7030-5R0-R	5µH	2.4A	0.026Ω	3mm
	SD20-6R2-R	6.2µH	1.12A	0.072Ω	2mm
Sumida	CDR6D23MNNP-4R2	4.2µH	2.6A	0.052Ω	2.5mm
	CDRH4D16FB/ND-6R8N	6.8µH	1A	0.081Ω	1.8mm

APPLICATIONS INFORMATION

Capacitor Vendor Information

Both the input and output capacitors used with the LTC3521 must be low ESR and designed to handle the large AC currents generated by switching converters. The vendors in Table 5 provide capacitors that are well suited to LTC3521 application circuits.

Table 5. Capacitor Vendor Information

MANUFACTURER	WEB SITE	REPRESENTATIVE PART NUMBERS
Taiyo Yuden	www.t-yuden.com	JMK212BJ106K 10µF, 6.3V
		JMK212BJ226K 22µF, 6.3V
TDK	www.component.tdk.com	C2012X5R0J106K 10µF, 6.3V
Murata	www.murata.com	GRM21BR60J106K 10µF, 6.3V
		GRM32ER61C226K 22µF, 16V
AVX	www.avxcorp.com	SM055C106KHN480 10µF

Minimizing solution size is usually a priority. Please be aware that ceramic capacitors can exhibit a significant reduction in effective capacitance when a bias is applied. The capacitors exhibiting the highest reduction are those packaged in the smallest case size.

PCB Layout Considerations

The LTC3521 switches large currents at high frequencies. Special care should be given to the PCB layout to ensure stable, noise-free operation. Figure 5 depicts the recommended PCB layout to be utilized for the LTC3521. A few key guidelines follow:

1. All circulating high current paths should be kept as short as possible. This can be accomplished by keeping the routes to all bold components in Figure 5 as short and as wide as possible. Capacitor ground connections should via down to the ground plane in the shortest route possible. The bypass capacitors on PV_{IN1} and PV_{IN2} should be placed as close to the IC as possible and should have the shortest possible paths to ground.
2. The small-signal ground pad (GND) should have a single point connection to the power ground. A convenient way to achieve this is to short the pin directly to the Exposed Pad as shown in Figure 5.
3. The components shown in bold, and their connections, should all be placed over a complete ground plane.
4. To prevent large circulating currents from disrupting the output voltage sensing, the ground for each resistor divider should be returned directly to the small signal ground pin (GND).
5. Use of vias in the die attach pad will enhance the thermal environment of the converter, especially if the vias extend to a ground plane region on the exposed bottom surface of the PCB.

APPLICATIONS INFORMATION

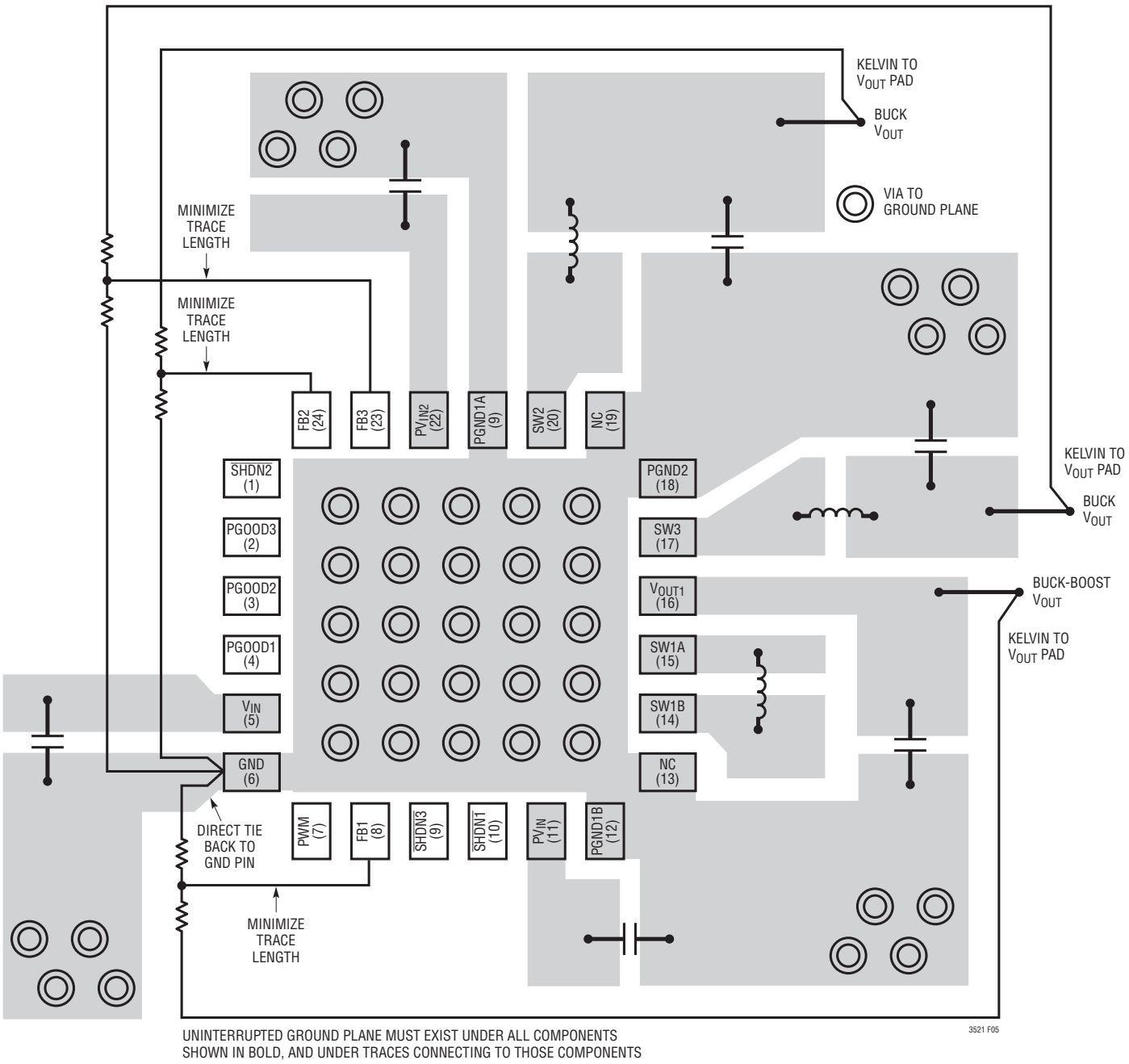
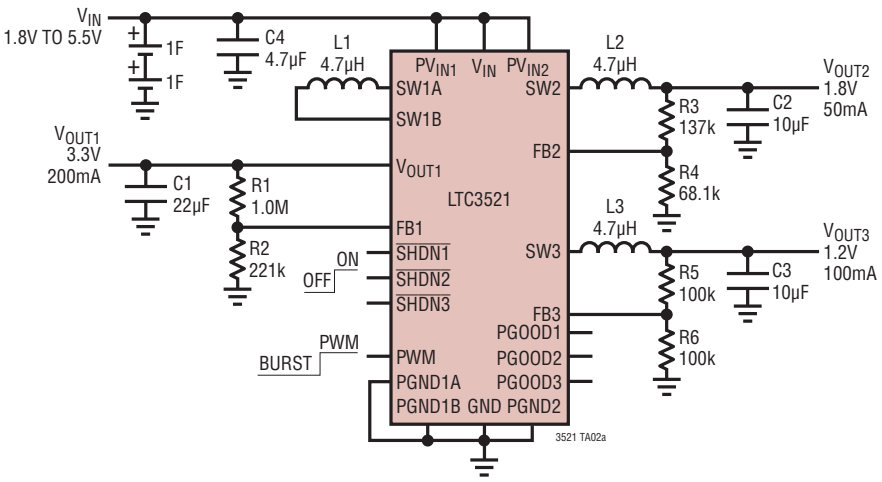


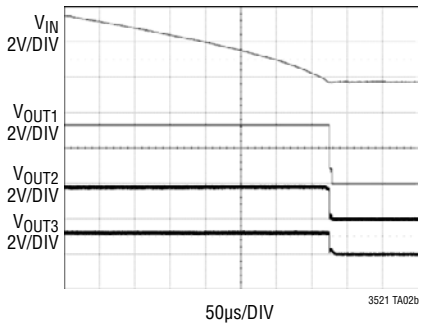
Figure 5. LTC3521 Recommended PCB Layout

TYPICAL APPLICATION

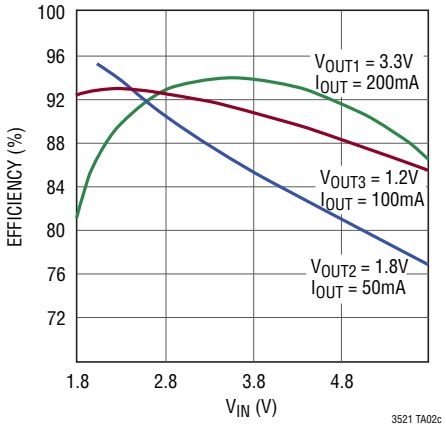
Dual Supercapacitor to 3.3V at 200mA, 1.8V at 50mA and 1.2V at 100mA Backup Power Supply



Converter Output Voltages

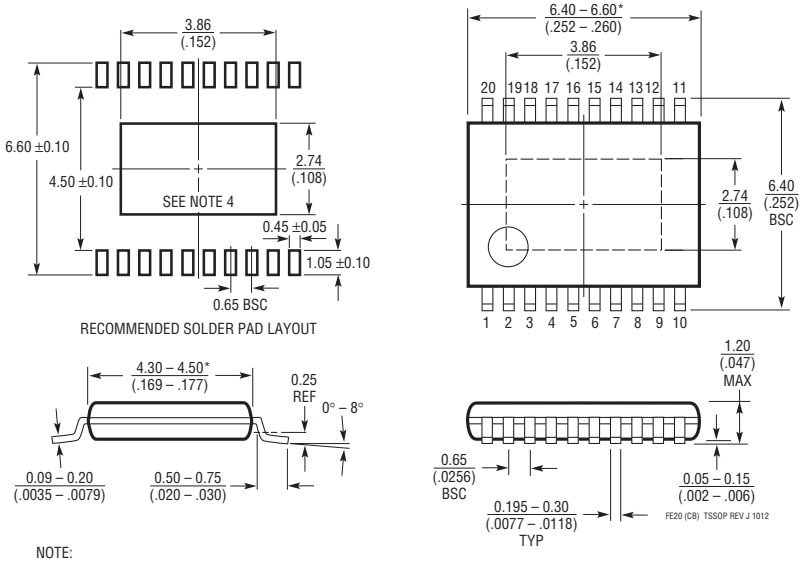


Efficiency vs V_{IN}



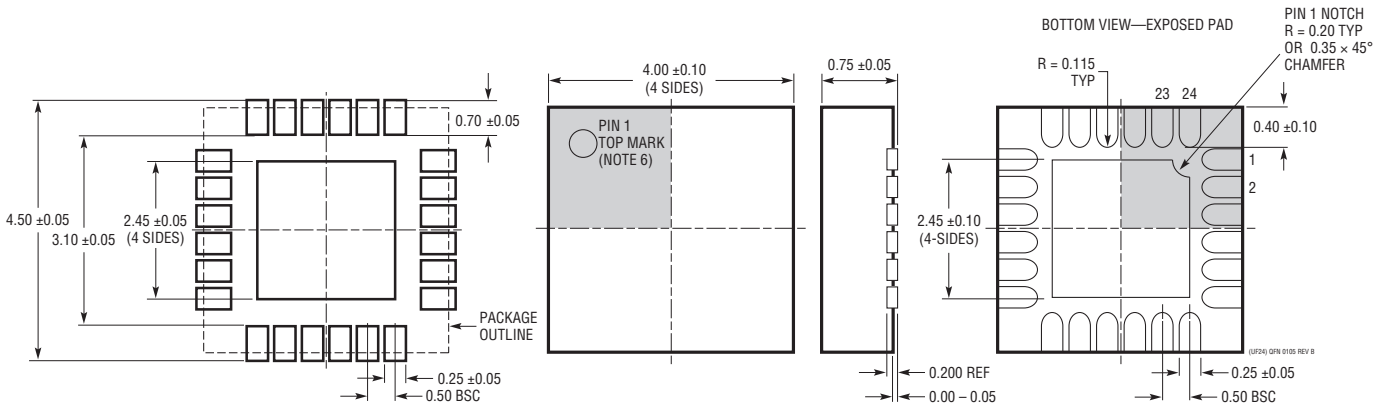
PACKAGE DESCRIPTION

FE Package
20-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev J)
Exposed Pad Variation CB



NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT
*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

UF Package
24-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1697 Rev B)



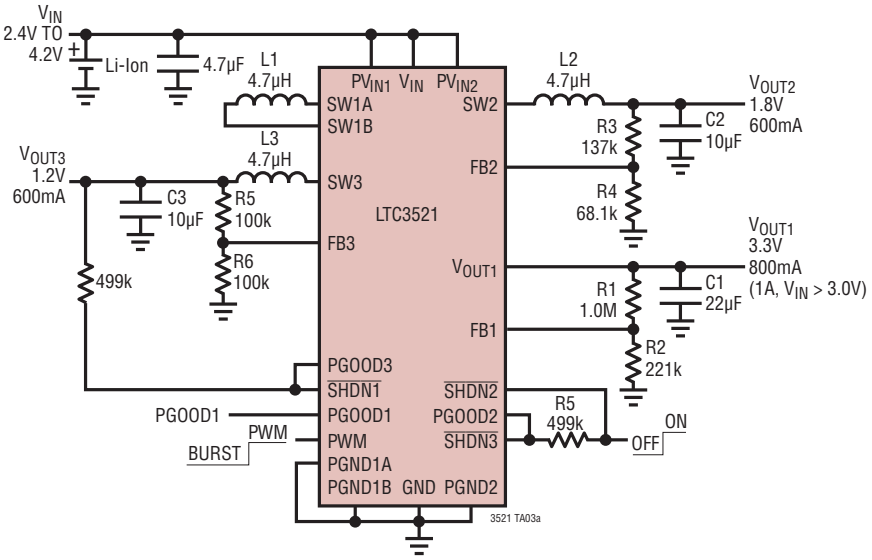
NOTE:
1. DRAWING PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-X)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE, IF PRESENT
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

REVISION HISTORY

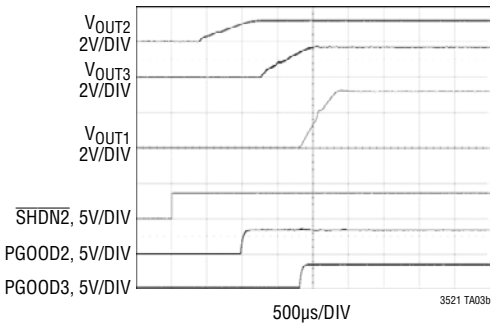
REV	DATE	DESCRIPTION	PAGE NUMBER
A	11/10	Addition of PGND1A reflected throughout data sheet	
		Addition of V_{IN} to Typical Applications	1, 19, 22
		Revised Note 2	3
		Changes to Block Diagram	9
		Change to Operation Soft-Start section	11, 13
B	08/13	Corrected pin numbers on Block Diagram UF package	9

TYPICAL APPLICATION

Li-Ion to 3.3V at 800mA, 1.8V at 600mA and 1.2V at 600mA with Sequenced Start-Up



Sequenced Start-Up Waveforms



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3100	700mA I_{SW}, 1.5MHz, Synchronous Step-Up, 250mA Synchronous Step-Down DC/DC Converter and 100mA LDO	94% Efficiency, V_{IN}: 0.7V to 5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 15µA, I_{SD} < 1µA, 3mm × 3mm QFN-16 Package
LTC3101	Wide V_{IN}, Multioutput DC/DC Converter and PowerPath™ Controller, 800mA Buck-Boost, Dual 350mA Buck Converters, 50mA Always-On LDO	95% Efficiency, V_{IN}: 1.8V to 5.5V, I_Q = 38µA, Standby I_Q = 15µA, 4mm × 4mm QFN-24 Package
LTC3409	600mA I_{OUT}, 1.7MHz/2.6MHz, Synchronous Step-Down DC/DC Converter	96% Efficiency, V_{IN}: 1.6V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 65µA, I_{SD} < 1µA, DFN Package
LTC3441/LTC3442/ LTC3443	1.2A I_{OUT}, 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MIN)}$: 2.4V to 5.25V, I_Q = 50µA, I_{SD} < 1µA, DFN Package
LTC3520	1A 2MHz, Synchronous Buck-Boost and 600mA Buck Converter	95% Efficiency, V_{IN}: 2.2V to 5.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 55µA, I_{SD} < 1µA, 4mm × 4mm QFN-24 Package
LTC3522	400mA 2MHz, Synchronous Buck-Boost and 200mA Buck Converter	95% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 25µA, I_{SD} < 1µA, 3mm × 3mm QFN-16 Package
LTC3531/LTC3531-3/ LTC3531-3.3	200mA I_{OUT}, 1.5MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 1.8V to 5.5V, $V_{OUT(MIN)}$: 2V to 5V, I_Q = 16µA, I_{SD} < 1µA, ThinSOT and DFN Packages
LTC3532	500mA I_{OUT}, 2MHz, Synchronous Buck-Boost DC/DC Converter	95% Efficiency, V_{IN}: 2.4V to 5.5V, $V_{OUT(MIN)}$: 2.4V to 5.25V, I_Q = 35µA, I_{SD} < 1µA, MS10 and DFN Packages
LTC3547	Dual 300mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, V_{IN}: 2.5V to 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40µA, I_{SD} < 1µA, DFN-8 Package

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