TY Semicondutor®

Product specification

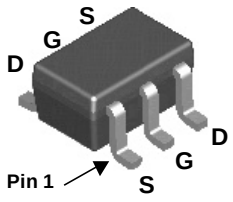
FDG6317NZ

Features

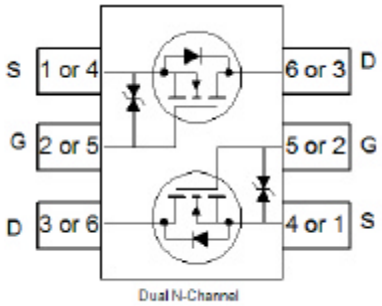
- 0.7 A, 20 V. $R_{DS(ON)}$ = 400 mΩ @ V_{GS} = 4.5 V
  $R_{DS(ON)}$ = 550 mΩ @ V_{GS} = 2.5 V
- ESD protection diode (note 3)
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- Compact industry standard SC70-6 surface mount package

Applications

- DC/DC converter
- Power management
- Loadswitch



SC70-6



The pinouts are symmetrical; pin 1 and pin 4 are interchangeable.

Absolute Maximum Ratings

T_A=25°C unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DSS}	Drain-Source Voltage	20	V
V_{GSS}	Gate-Source Voltage	± 12	V
I_D	Drain Current – Continuous (Note 1)	0.7	A
	– Pulsed	2.1	
P_D	Power Dissipation for Single Operation (Note 1)	0.3	W
T_J, T_{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	415	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
.67	FDG6317NZ	7''	8mm	3000 units

Electrical Characteristics

T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 µA	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 µA, Referenced to 25°C		13		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 16 V, V_{GS} = 0 V			1	µA
I_{GSS}	Gate–Body Leakage	V_{GS} = ± 12 V, V_{DS} = 0 V			± 10	µA
I_{GSS}	Gate–Body Leakage	V_{GS} = ± 4.5 V, V_{DS} = 0 V			± 1	µA
On Characteristics (Note 2)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250 µA	0.6	1.2	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = –250 µA, Referenced to 25°C		–2		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 4.5 V, I_D = 0.7 A V_{GS} = 2.5 V, I_D = 0.6 A V_{GS} = 4.5 V, I_D = 0.7 A, T_J=125°C		300 450 390	400 550 560	mΩ
$I_{D(on)}$	On–State Drain Current	V_{GS} = 4.5 V, V_{DS} = 5 V	1			A
g_{FS}	Forward Transconductance	V_{DS} = 5 V, I_D = 0.7 A		1.8		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 10 V, V_{GS} = 0 V, f = 1.0 MHz		66.5		pF
C_{oss}	Output Capacitance			19		pF
C_{rss}	Reverse Transfer Capacitance			10		pF
R_G	Gate Resistance	V_{GS} = 15 mV, f = 1.0 MHz		5.8		Ω
Switching Characteristics (Note 2)						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 10 V, I_D = 1 A, V_{GS} = 4.5 V, R_{GEN} = 6 Ω		5.5	11	ns
t_r	Turn–On Rise Time			7	15	ns
$t_{d(off)}$	Turn–Off Delay Time			7.5	15	ns
t_f	Turn–Off Fall Time			2.5	5	ns
Q_g	Total Gate Charge	V_{DS} = 10 V, I_D = 0.7 A, V_{GS} = 4.5 V		0.76	1.1	nC
Q_{gs}	Gate–Source Charge			0.18		nC
Q_{gd}	Gate–Drain Charge			0.20		nC
Drain–Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain–Source Diode Forward Current				0.25	A
V_{SD}	Drain–Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 0.25 A (Note 2)		0.8	1.2	V
t_{rr}	Diode Reverse Recovery Time	I_F = 0.7 A, d_{iF}/d_t = 100 A/µs		8.3		nS
Q_{rr}	Diode Reverse Recovery Charge			1.2		nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design. $R_{\theta JA}$ = 415°C/W when mounted on a minimum pad .

2. Pulse Test: Pulse Width < 300µs, Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.