10 Base-T Interface Module

EPE6199S

- Optimized for Level One LXT905 •
- Two pairs of TX and RX in 40 pin SOIC package •
- Robust design allows for toughest soldering process •
- Complies with or exceeds IEEE 802.3, 10 Base-T Requirements •

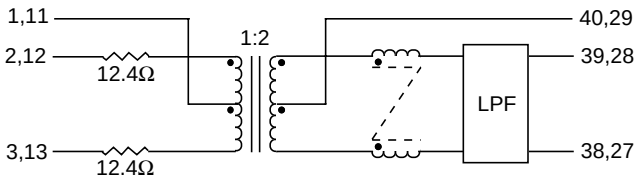
Electrical Parameters @ 25° C

Group Delay (nS Max.)		Insertion Loss (dB Max.)		Return Loss (dB Min.)		Attenuation (dB Min.) (1)						Common Mode Rejection (dB Min.)				Crosstalk (dB Min.)
5-10 MHz		1-10 MHz		5-10 MHz		@ 25 MHz		@ 30 MHz		@ 40 MHz		@ 50 MHz		@ 100 MHz		@ 1-10 MHz
Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	Xmit	Rcv	
3	---	-1	-1	-15	-15	-10	---	-20	---	-30	---	-30	-30	-25	-25	-30

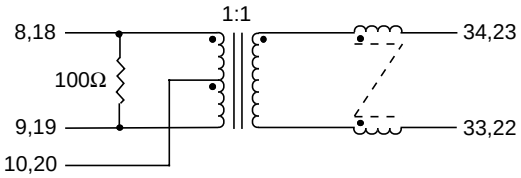
• **Isolation** : meets or exceeds 802.3 IEEE Requirements • **Characteristic Filter Impedance** : 100 Ω •
(1) Referenced @ 5 MHz response.

Schematic

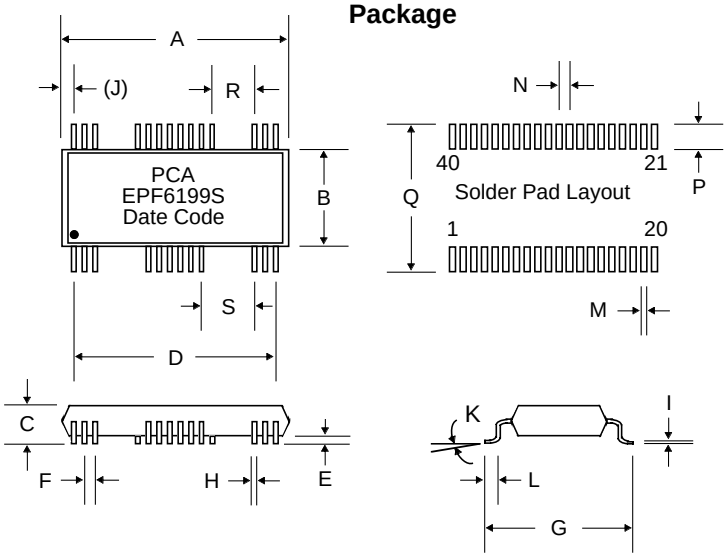
Transmit Channel



Receive Channel



Package



Dimensions

Dim.	(Inches) Min.	Max.	Nom.	(Millimeters) Min.	Max.	Nom.
A	1.105	1.125		28.67	28.58	
B	.470	.490		11.94	12.45	
C	.200	.220		5.08	5.59	
D	.950	Typ.		24.13	Typ.	
E	.005	.015		.127	.381	
F	.050	Typ.		1.27	Typ.	
G	.620	.640		15.75	16.26	
H	.016	.022.		.406	.559	
I	.008	.012		.203	.305	
(J)	.083	Typ.		2.10	Typ.	
K	0°	8°		0°	8°	
L	.025	.045		.635	1.14	
M			.030			.762
N			.050			1.27
P			.090			2.29
Q			.670			17.02
R	.200	Typ.	2 plcs	5.08	Typ.	2 plcs
S	.250	Typ.	2 plcs	6.35	Typ.	2 plcs

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CSE6199Sa Rev.- 6/5/97

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10 Base-T Interface Module

EPE6199S

The circuit below is a guideline for interconnecting PCA's EPE6199S with LXT905 10 Base-T PHY chip over UTP cable. Further details of system design, such as chip pin-out, etc. can be obtained from the specific chip manufacturer.

Typical insertion loss of the isolation transformer is 0.7dB. This parameter covers the entire spectrum of the encoded signals in 10 Base-T protocols. However, the predistortion resistor network introduces some loss which has to be taken into account in determining how well your design meets the Standard Template requirements. Additionally, the following need to be considered while selecting resistor values :

a. Each channel needs 100Ω termination, thus the Thevenin's equivalent resistance seen by a channel looking into the transmit outputs from the chip must be equal to a value close to 100Ω. The LXT 905 driver output impedances are very low. . Thus only 11.8Ω on TPON & TPOP are enough to provide a balanced 25 Ω termination given that turns ratio is 1:2. Following these guidelines will guarantee that the return loss specifications are satisfied at all extremes of cable impedance (i.e. 85Ω to 115Ω) while the module is installed in your system. The receiver channel termination is rather straight forward: two 50Ω loads provide the balanced termination to the cable.

b. That the template requirements are satisfied under the worst case Vcc (i.e. 4.5V), will impose a further constraint on resistor selection, in that they ought to be the minimum derived from the calculations. Users can allow for pads on their PCB for a shunting resistor across pins 6 and 8 of EPE6199S for more flexibility in setting voltage levels at the outputs.

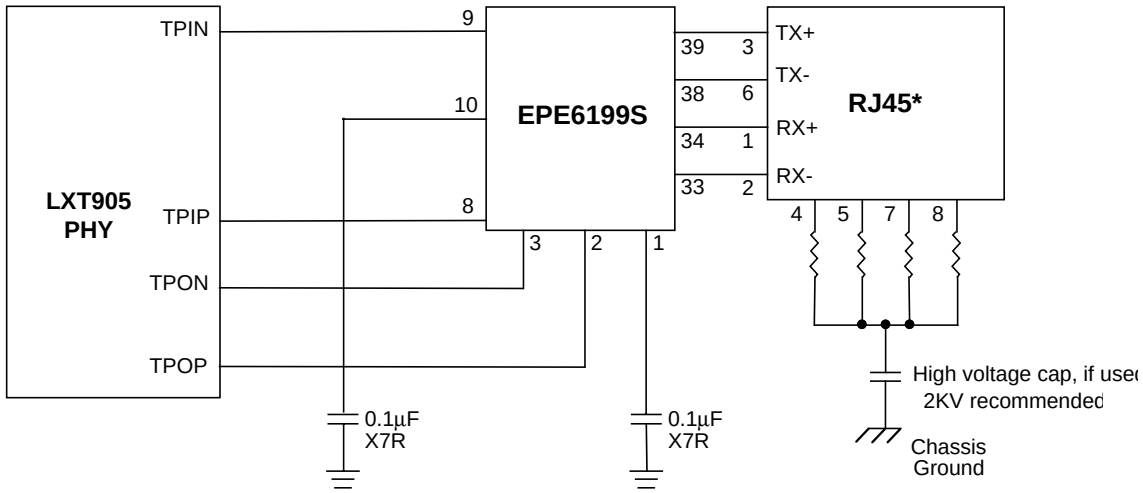
Note that some systems have auto polarity detection and some do not. If not, be certain to follow the proper polarity.

The pulldown resistors used around the RJ45 connector have been known to suppress unwanted radiation that unused wires pick up from the immediate environment. Their placement and use are to be considered carefully before a design is finalized.

It is recommended that there be a neat separation of ground planes in the layout. It is generally accepted practice to limit the plane off at least 0.08 inches away from the chip side pins of EPE6199S. There need not be any ground plane beyond this point.

For best results, PCB designer should design the outgoing traces preferably to be 50Ω, balanced and well coupled to achieve minimum radiation from these traces.

Typical Application Circuit for UTP for one port only.



Notes : * Pin-outs shown are for Hubs and Repeaters.

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