

ESD8008

Transient Voltage Suppressors

Low Capacitance ESD Protection for High Speed Data

The ESD8008 transient voltage suppressor is designed specifically to protect four high speed differential pairs. Ultra-low capacitance and low ESD clamping voltage make this device an ideal solution for protecting voltage sensitive high speed data lines. The flow-through style package allows for easy PCB layout and matched trace lengths necessary to maintain consistent impedance for the high speed lines.

Features

- Integrated 4 Pairs (8 Lines) High Speed Data
- Single Connect, Flow through Routing
- Low Capacitance (0.35 pF Max, I/O to GND)
- Protection for the Following IEC Standards:
IEC 61000-4-2 Level 4
- UL Flammability Rating of 94 V-0
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

Typical Applications

- V-by-One HS
- Thunderbolt
- Display Port
- LVDS

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Operating Junction Temperature Range	T _J	-55 to +125	°C
Storage Temperature Range	T _{stg}	-55 to +150	°C
Lead Solder Temperature - Maximum (10 Seconds)	T _L	260	°C
IEC 61000-4-2 Contact (ESD)	ESD	±15	kV
IEC 61000-4-2 Air (ESD)	ESD	±15	kV

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

See Application Note AND8308/D for further description of survivability specs.



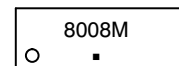
ON Semiconductor®

<http://onsemi.com>



UDFN14
CASE 517CN

MARKING DIAGRAM



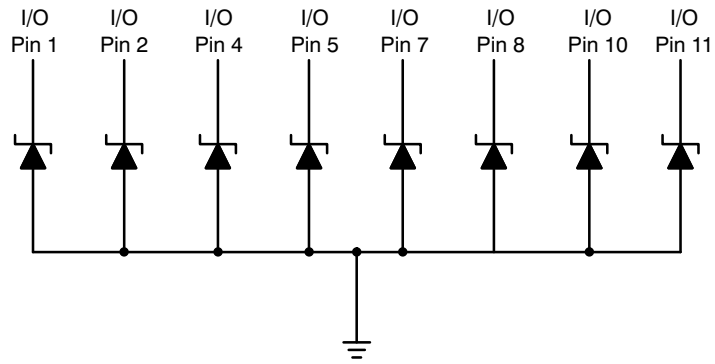
- 8008 = Specific Device Code
- M = Date Code
- = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping
ESD8008MUTAG	UDFN14 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

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Center Pins, Pin 3, 6, 9, 12, 13, 14

Note: Common GND – Only Minimum of 1 GND connection required

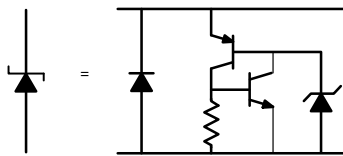


Figure 1. Pin Schematic

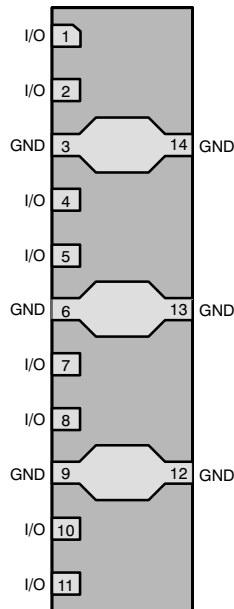


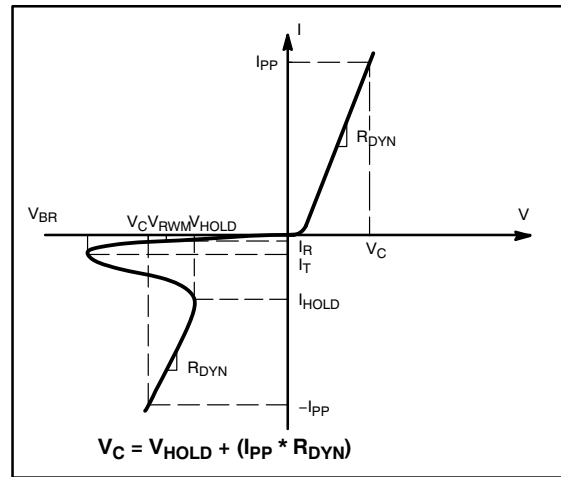
Figure 2. Pin Configuration

Note: Only minimum of one pin needs to be connected to ground for functionality of all pins.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
V _{RWM}	Working Peak Voltage
I _R	Maximum Reverse Leakage Current @ V _{RWM}
V _{BR}	Breakdown Voltage @ I _T
I _T	Test Current
V _{HOLD}	Holding Reverse Voltage
I _{HOLD}	Holding Reverse Current
R _{DYN}	Dynamic Resistance
I _{PP}	Maximum Peak Pulse Current
V _C	Clamping Voltage @ I _{PP} V _C = V _{HOLD} + (I _{PP} * R _{DYN})



ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit						
Reverse Working Voltage	V _{RWM}	I/O Pin to GND			3.3	V						
Breakdown Voltage	V _{BR}	I _T = 1 mA, I/O Pin to GND	5.5			V						
Reverse Leakage Current	I _R	V _{RWM} = 3.3 V, I/O Pin to GND			0.5	μA						
Holding Reverse Voltage	V _{HOLD}	I/O Pin to GND		1.19		V						
Holding Reverse Current	I _{HOLD}	I/O Pin to GND		25		mA						
Clamping Voltage (Note 1)	V _C	IEC61000-4-2, ±8 kV Contact	See Figures 3 and 4			V						
Clamping Voltage TLP (Note 2) See Figures 7 through 10	V _C	<table border="0"> <tr> <td>I_{PP} = 8 A</td> <td rowspan="2">} IEC 61000-4-2 Level 2 equivalent (±4 kV Contact, ±4 kV Air)</td> </tr> <tr> <td>I_{PP} = -8 A</td> </tr> <tr> <td>I_{PP} = 16 A</td> <td rowspan="2">} IEC 61000-4-2 Level 4 equivalent (±8 kV Contact, ±15 kV Air)</td> </tr> <tr> <td>I_{PP} = -16 A</td> </tr> </table>	I _{PP} = 8 A	} IEC 61000-4-2 Level 2 equivalent (±4 kV Contact, ±4 kV Air)	I _{PP} = -8 A	I _{PP} = 16 A	} IEC 61000-4-2 Level 4 equivalent (±8 kV Contact, ±15 kV Air)	I _{PP} = -16 A		4.8 -4.7		V
I _{PP} = 8 A	} IEC 61000-4-2 Level 2 equivalent (±4 kV Contact, ±4 kV Air)											
I _{PP} = -8 A												
I _{PP} = 16 A	} IEC 61000-4-2 Level 4 equivalent (±8 kV Contact, ±15 kV Air)											
I _{PP} = -16 A												
Dynamic Resistance	R _{DYN}	I/O Pin to GND GND to I/O Pin		0.40 0.45		Ω						
Junction Capacitance	C _J	<table border="0"> <tr> <td>V_R = 0 V, f = 1 MHz between I/O Pins and GND</td> <td rowspan="4">}</td> </tr> <tr> <td>V_R = 0 V, f = 2.5 GHz between I/O Pins and GND</td> </tr> <tr> <td>V_R = 0 V, f = 5.0 GHz between I/O Pins and GND</td> </tr> <tr> <td>V_R = 0 V, f = 1 MHz, between I/O Pins</td> </tr> </table>	V _R = 0 V, f = 1 MHz between I/O Pins and GND	}	V _R = 0 V, f = 2.5 GHz between I/O Pins and GND	V _R = 0 V, f = 5.0 GHz between I/O Pins and GND	V _R = 0 V, f = 1 MHz, between I/O Pins		0.30 0.20 0.20 0.10	0.35 0.16	pF	
V _R = 0 V, f = 1 MHz between I/O Pins and GND	}											
V _R = 0 V, f = 2.5 GHz between I/O Pins and GND												
V _R = 0 V, f = 5.0 GHz between I/O Pins and GND												
V _R = 0 V, f = 1 MHz, between I/O Pins												

- For test procedure see Figures 5 and 6 and application note AND8307/D.
- ANSI/ESD STM5.5.1 – Electrostatic Discharge Sensitivity Testing using Transmission Line Pulse (TLP) Model.
TLP conditions: Z₀ = 50 Ω, t_p = 100 ns, t_r = 4 ns, averaging window; t₁ = 30 ns to t₂ = 60 ns.

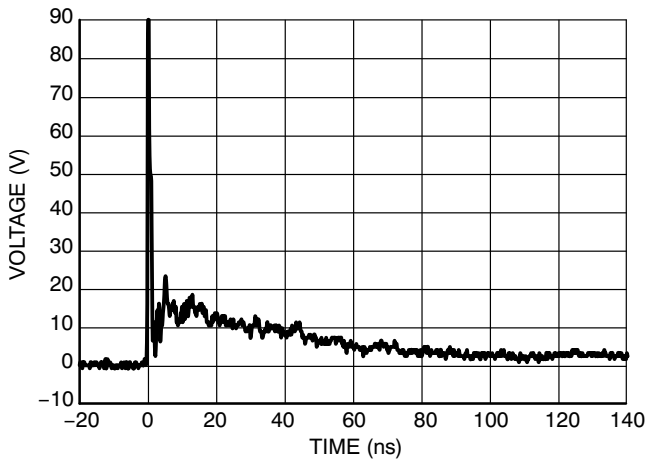


Figure 3. IEC61000-4-2 +8 kV Contact ESD Clamping Voltage

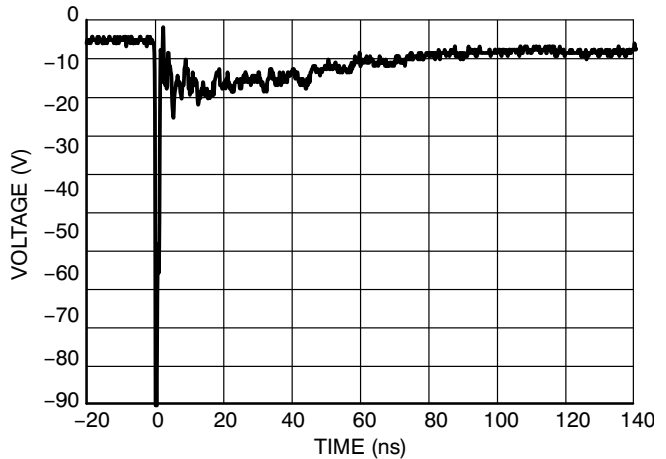


Figure 4. IEC61000-4-2 -8 kV Contact Clamping Voltage

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IEC 61000-4-2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

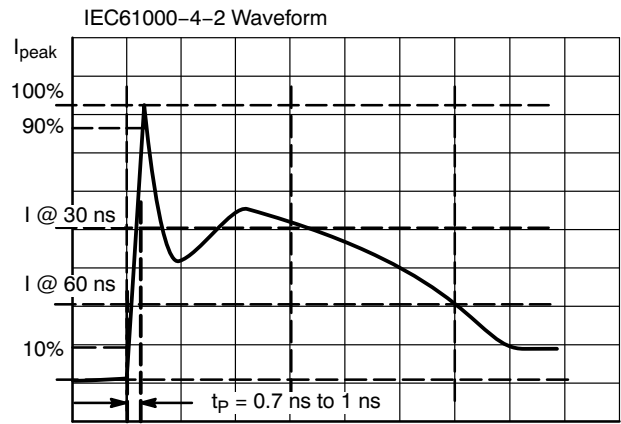


Figure 5. IEC61000-4-2 Spec

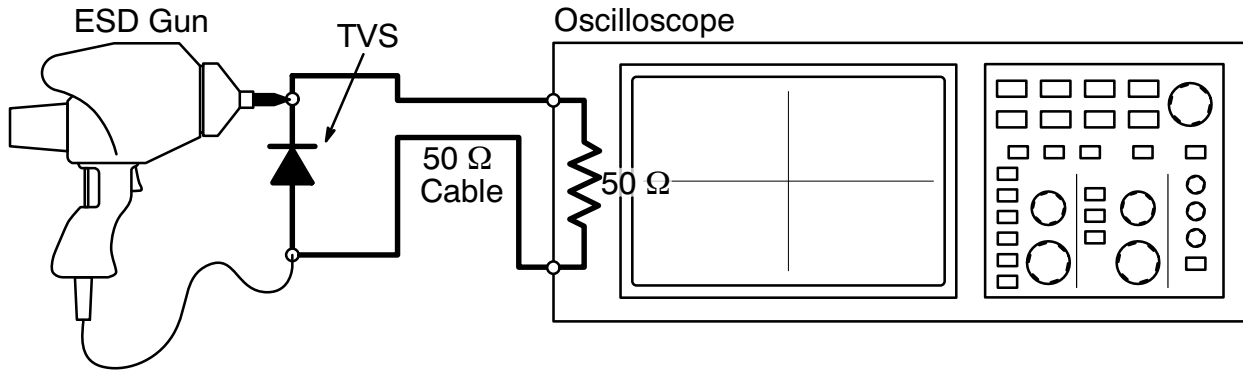


Figure 6. Diagram of ESD Clamping Voltage Test Setup

The following is taken from Application Note AND8308/D – Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000-4-2 waveform. Since the IEC61000-4-2 was written as a pass/fail spec for larger

systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

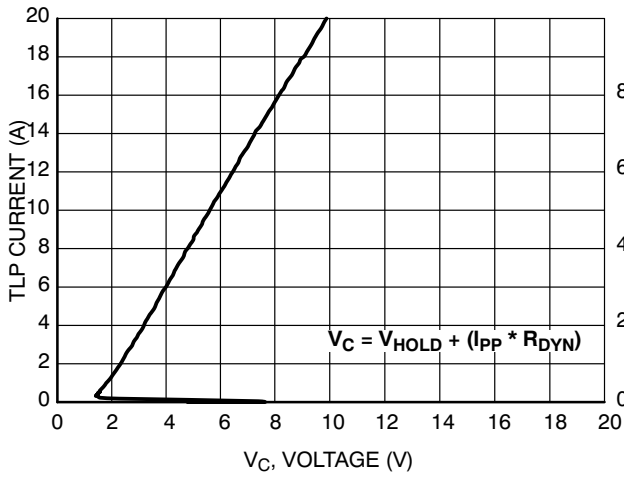


Figure 7. Positive TLP I-V Curve

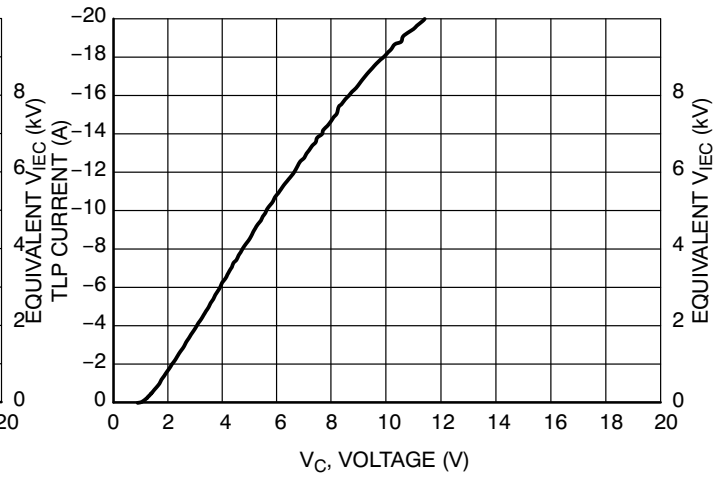


Figure 8. Negative TLP I-V Curve

NOTE: TLP parameter: $Z_0 = 50 \Omega$, $t_p = 100 \text{ ns}$, $t_r = 300 \text{ ps}$, averaging window: $t_1 = 30 \text{ ns}$ to $t_2 = 60 \text{ ns}$. V_{IEC} is the equivalent voltage stress level calculated at the secondary peak of the IEC 61000-4-2 waveform at $t = 30 \text{ ns}$ with 2 A/kV . See TLP description below for more information.

Transmission Line Pulse (TLP) Measurement

Transmission Line Pulse (TLP) provides current versus voltage (I-V) curves in which each data point is obtained from a 100 ns long rectangular pulse from a charged transmission line. A simplified schematic of a typical TLP system is shown in Figure 9. TLP I-V curves of ESD protection devices accurately demonstrate the product's ESD capability because the 10s of amps current levels and under 100 ns time scale match those of an ESD event. This is illustrated in Figure 10 where an 8 kV IEC 61000-4-2 current waveform is compared with TLP current pulses at 8 A and 16 A. A TLP I-V curve shows the voltage at which the device turns on as well as how well the device clamps voltage over a range of current levels.

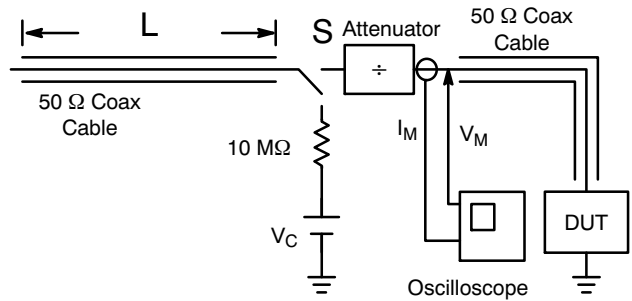


Figure 9. Simplified Schematic of a Typical TLP System

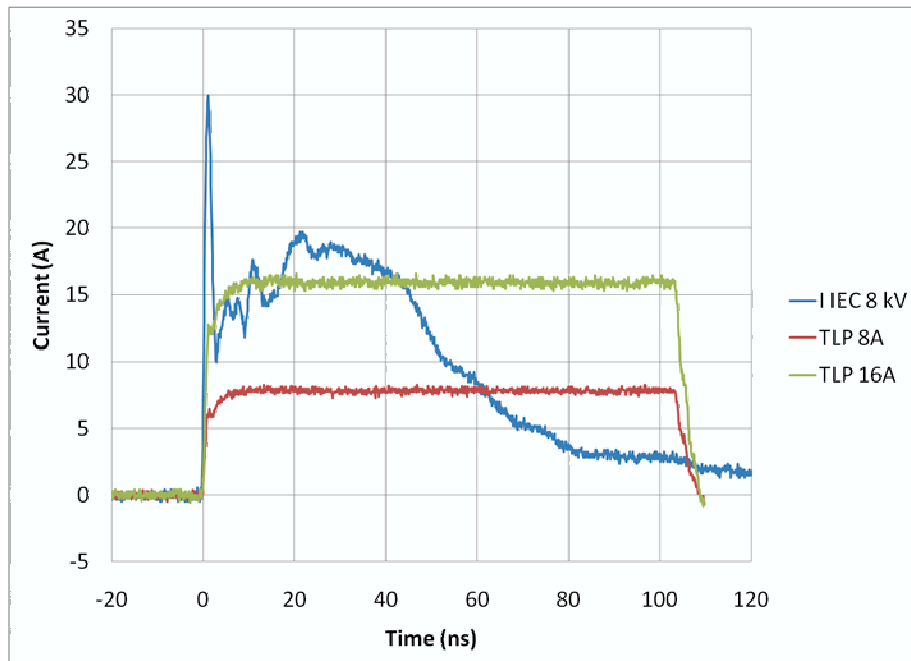


Figure 10. Comparison Between 8 kV IEC 61000-4-2 and 8 A and 16 A TLP Waveforms

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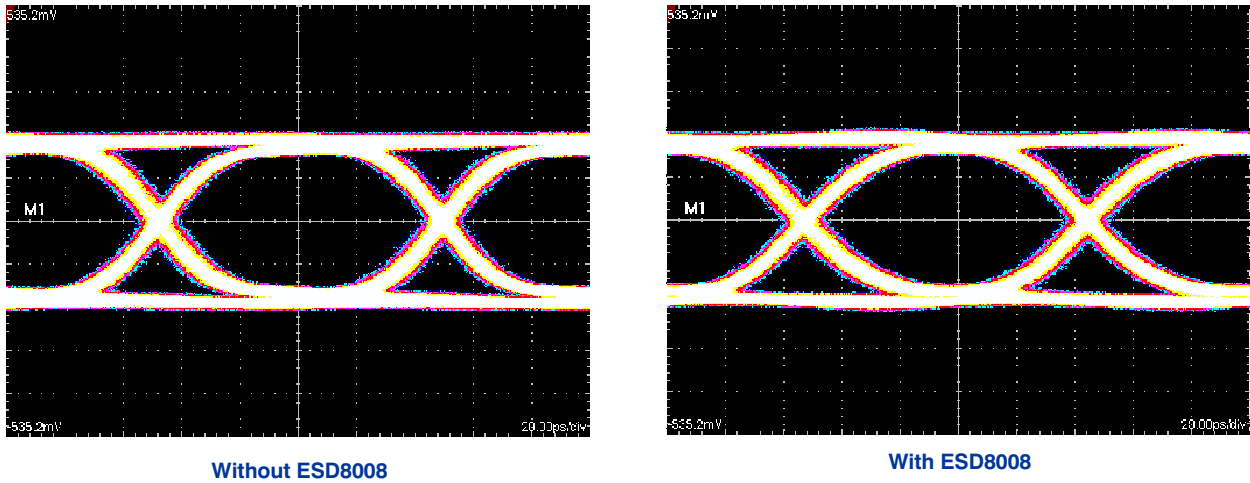
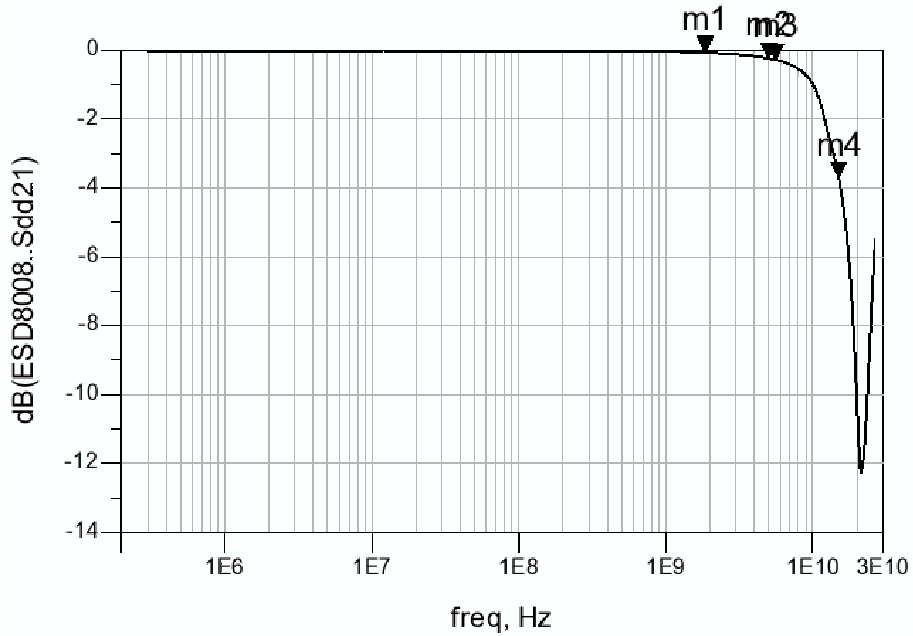


Figure 11. Thunderbolt Eye Diagram with and without ESD8008. 10 Gb/s, 400 mVpp

See application note AND9075/D for further description of eye diagram testing methodology.



Interface	Data Rate (Gbps)	Fundamental Frequency (GHz)	3 rd Harmonic Frequency (GHz)	ESD8008 Insertion Loss (-dB)
V-by-One HS Full HD (1920 x 1080p) 240 Hz, 36bit color depth	3.71	1.854 (m1)	5.562 (m3)	m1 = 0.070 m3 = 0.282
Thunderbolt	10	5 (m2)	15 (m4)	m2 = 0.240 m4 = 3.732

Figure 12. ESD8008 Insertion Loss

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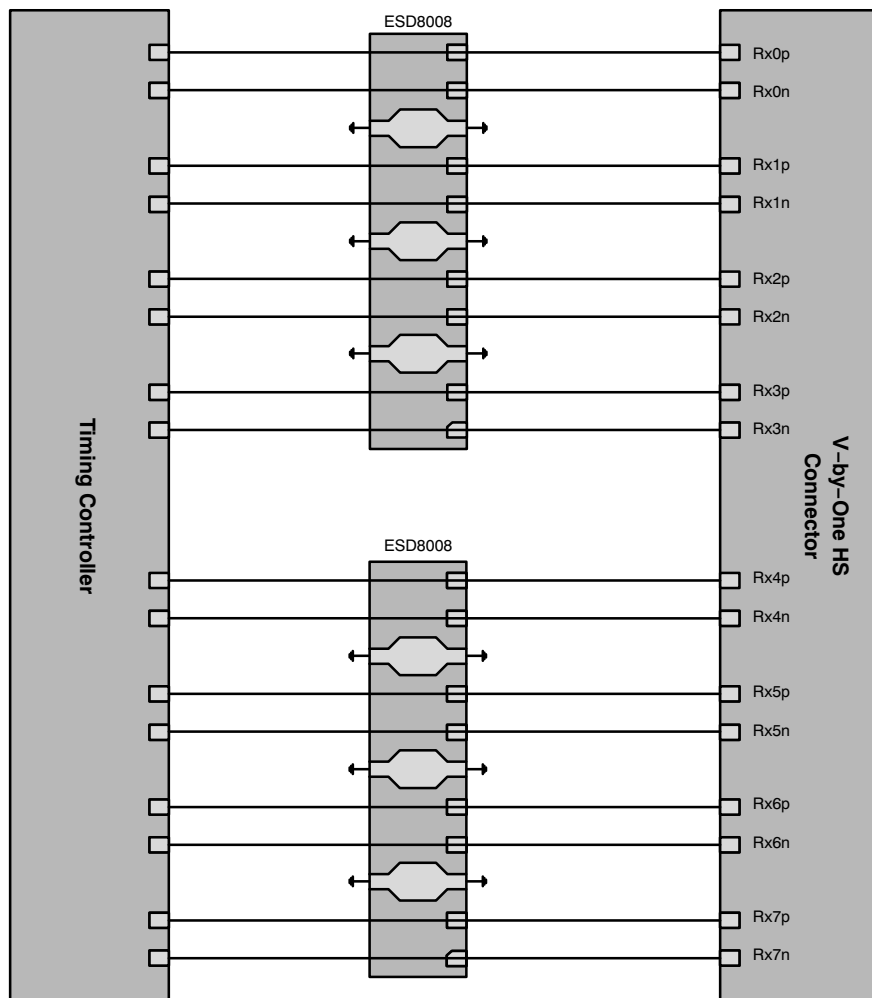
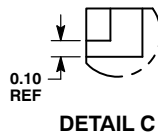
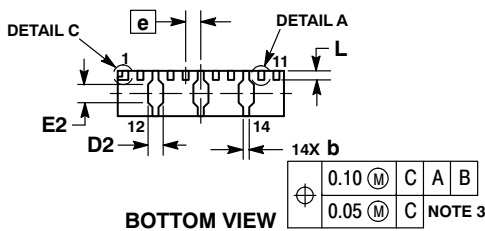
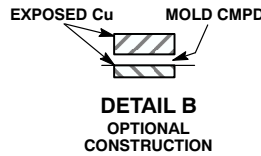
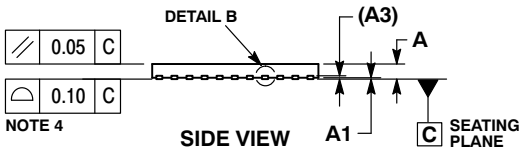
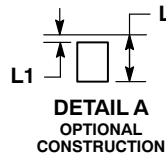
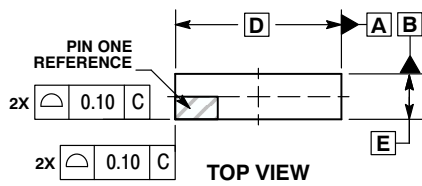


Figure 14. V-by-One HS Layout Diagram (for LCD Panel)

ESD8008

PACKAGE DIMENSIONS

UDFN14, 5.5x1.5, 0.5P CASE 517CN ISSUE O

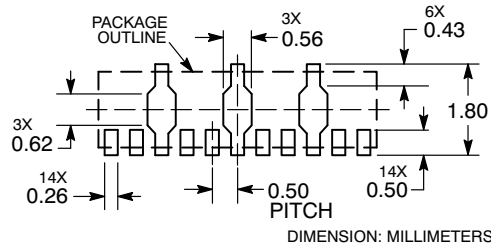


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.10 AND 0.20 MM FROM TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.45	0.55
A1	0.00	0.05
A3	0.13	REF
b	0.15	0.25
D	5.50 BSC	
D2	0.45	0.55
E	1.50 BSC	
E2	0.50	0.70
e	0.50 BSC	
L	0.20	0.40
L1	0.00	0.05

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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