1,048,576 WORD x 1 Bit High-Speed CMOS Static RAM

FEATURES

- **Fast Access Time : 20, 25, 35ns(max.)**
- **Low Power Dissipation**
  - **Standby** (TTL) : 40mA (max.)
    (CMOS) : 100μA (max.) L-ver. only
    2mA (max.)
  - **Operating** KM611001-20 : 130mA (max.)
    KM611001-25 : 110mA (max.)
    KM611001-35 : 100mA (max.)
- **Single 5V$\pm$10% power supply**
- **TTL compatible inputs and outputs**
- **Fully Static Operation**
  - **No clock or refresh required**
- **Three state Output**
- **Low Data Retention Voltage : 2V(min.) L-ver. only**
- **Standard Pin Configuration**
  - **KM611001P/LP : 28-pin DIP(400mil)**
  - **KM611001J/LJ : 28-pin SOJ (400mil)**

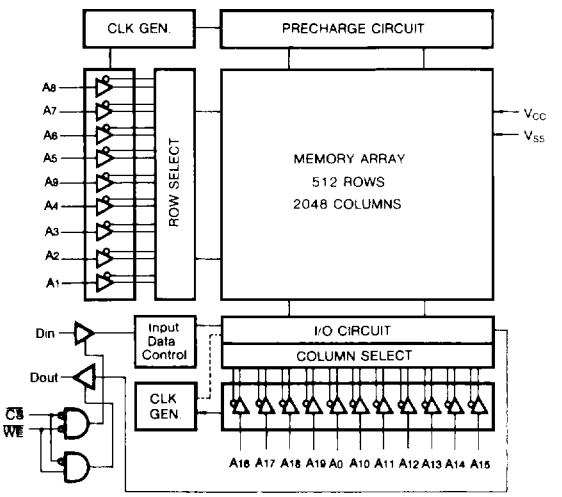
GENERAL DESCRIPTION

The KM611001/L is a 1,048,576-bit high-speed static random access memory organized as 1,048,576 words by 1 bit.

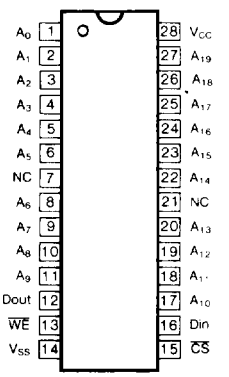
The KM611001/L has separate input and output lines for fast read and write access. The device is fabricated using Samsung's advanced CMOS process and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications.

The KM611001/L packaged in a 400mil 28-pin plastic DIP or SOJ with the conventional power supply paint.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION (Top Views)



Pin Name	Pin Function
A0-A19	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
DIN	Data Input
DOUT	Data Output
VCC	Power(+5V)
VSS	Ground
NC	No Connection

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ABSOLUTE MAXIMUM RATINGS*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}	V_{IN}, V_{OUT}	-0.5 to 7.0	V
Voltage on V_{CC} Supply Relative to V_{SS}	V_{CC}	-0.5 to 7.0	V
Power Dissipation	P_D	1.0	W
Storage Temperature	T_{stg}	-65 to + 150	°C
Operating Temperature	T_a	0 to 70	°C

* Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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RECOMMENDED OPERATING CONDITIONS (T_A=0 to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Ground	V_{SS}	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	V_{CC} + 0.5	V
Input Low Voltage	V_{IL}	-0.5*	—	0.8	V

* V_{IL}(min.)=-3.0V for $\leq$10ns pulse

DC AND OPERATING CHARACTERISTICS

(T_A=0 to 70°C, V_{CC}=5V$\pm$10%, unless otherwise specified)

Item	Symbol	Test Condition		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=Vss to V_{CC}		-	2	μA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{WE}$=V_{IL} V_{OUT}=Vss to V_{CC}		-	2	μA
Average Operating Current	I_{CC}	Min Cycle, 100% Duty $\overline{CS}$=V_{IL}, I_{OUT}=0mA	20ns	-	130	mA
			25ns	-	110	mA
			35ns	-	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, Min Cycle		-	40	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}$-0.2V, f=0MHz $V_{IN}\leq$0.2V or $V_{IN}\geq V_{CC}$-0.2V		-	2	mA
Output Low Voltage	V_{OL}	I_{OL}=8mA		-	0.4	V
Output High Voltage	V_{OH}	I_{OH}=-4mA		2.4	-	V

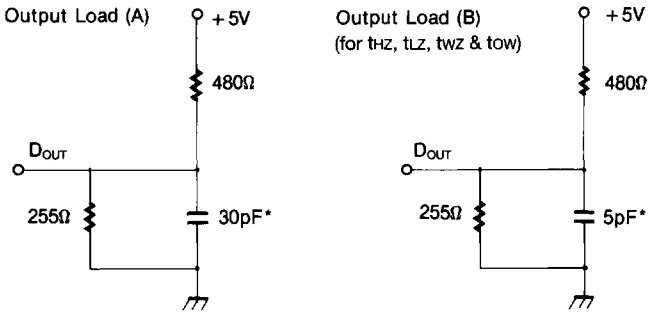
CAPACITANCE (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	7	pF
Input/Output Capacitance	C_{OUT}	V_{OUT}=0V	-	7	pF

* Capacitance is sampled and not 100% tested.

TEST CONDITIONS (T_A=0 to 70°C, V_{CC}=5V±10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0 to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Levels	1.5 V
Output Load	See below



* Including Scope and Jig Capacitance

READ CYCLE

Parameter	Symbol	-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	20		25		35		ns
Address Access Time	t_{AA}		20		25		35	ns
Chip Select to Output	t_{CO}		20		25		35	ns
Chip Select to Low-A Output	t_{LZ}	5		5		5		ns
Chip Disable to High-Z Output	t_{HZ}	0	12	0	15	0	15	ns
Output Hold from Address Change	t_{OH}	3		5		5		ns
Chip Selection to Power Up Time	t_{PU}	0		0		0		ns
Chip Deselection to Power Down Time	t_{PD}		20		25		35	ns

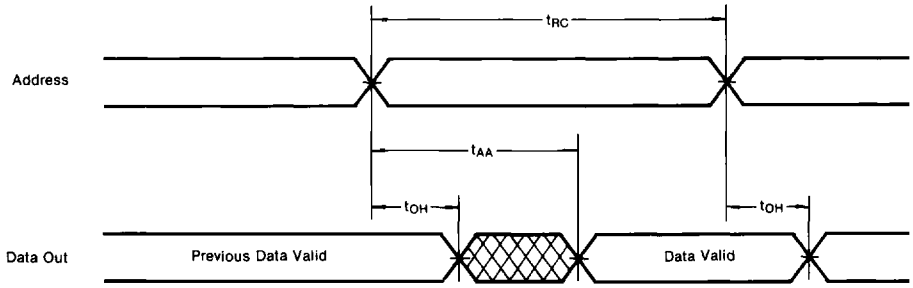
WRITE CYCLE

Parameter	Symbol	-20		-25		-35		Unit
		Min	Max	Min	Max	Min	Max	
Write Cycle Time	t_{WC}	20		25		35		ns
Chip Select to End of Write	t_{CW}	17		20		30		ns
Address Valid to End of Write	t_{AW}	17		20		30		ns
Address Set-up Time	t_{AS}	0		0		0		ns
Write Pulse Width	t_{WP}	15		20		25		ns
Write Recovery Time	t_{WR}	2		3		3		ns
Write to Output High-Z	t_{WZ}	0	8	0	10	0	12	ns
Data to Write Time Overlap	t_{DW}	12		15		20		ns
Data Hold from Write Time	t_{DH}	0		0		0		ns
End Write to Output Low-Z	t_{OW}	0		0		0		ns

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE (Address Controlled)

($\overline{CE}$=V_{IL}, $\overline{WE}$=V_{IH})



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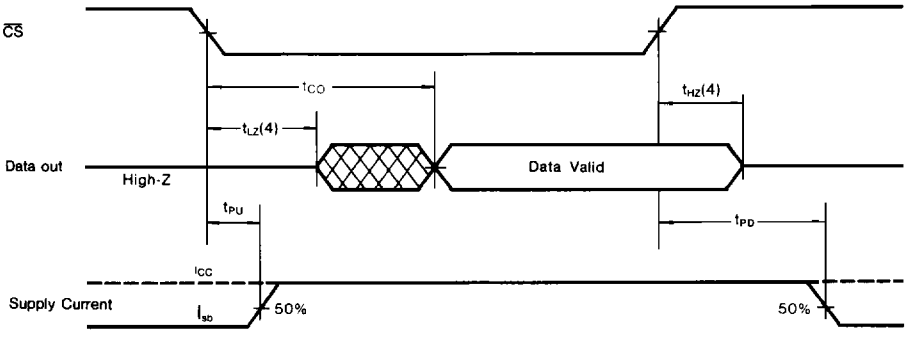
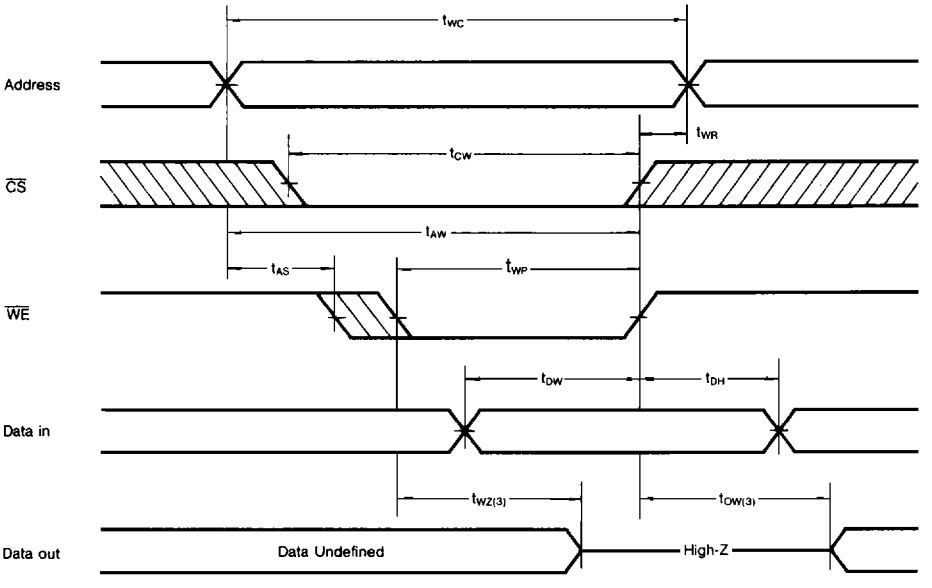
TIMING WAVEFORM OF READ CYCLE ($\overline{CS}$ Controlled)



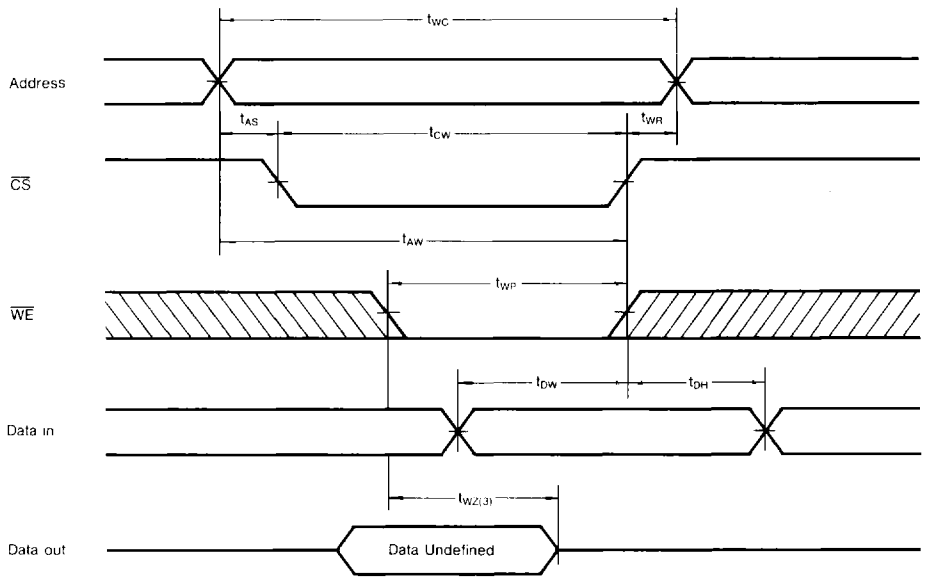
Note (READ CYCLE)

1. $\overline{WE}$ is high for read cycle.
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. At any given temperature and voltage condition, t_{HZ}(max.) is less than t_{LZ}(min.) both for a given device and from device to device.
4. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
5. Device is continuously selected with $\overline{CS}$=V_{IL}
6. Address valid prior to or coincident with $\overline{CS}$ transition low.

TIMING WAVEFORM OF WRITE CYCLE ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE ($\overline{CS}$ Controlled)



Notes (WRITE CYCLE)

1. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and low $\overline{WE}$.
2. All write cycle timing is referenced from the last valid address to the first transition address.
3. Transition is measured ±200mV from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
4. At any given temperature and voltage condition, t_{WZ}(max.) is less than t_{OW}(min.) both for a given device and from device to device.
5. $\overline{CS}$ or $\overline{WE}$ must be in high during address transition.

FUNCTIONAL DESCRIPTION

$\overline{CS}$	$\overline{WE}$	Dout PIN	Supply Current	Mode
H	X*	High-Z	I_{SB}, I_{SB1}	Not Select
L	H	Dout	I_{CC}	Read
L	L	High-Z	I_{CC}	Write

*Note: X means Don't Care