

PMN50XP

1. Product profile

1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology.

1.2 Features

- Low threshold voltage
- Low on-state losses

1.3 Applications

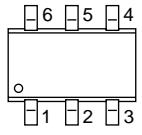
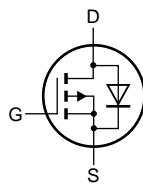
- Low power DC-to-DC converters
- Load switching
- Battery management
- Battery powered portable equipment

1.4 Quick reference data

- $V_{DS} \leq -20 \text{ V}$
- $R_{DSon} \leq 60 \text{ m}\Omega$
- $I_D \leq -4.8 \text{ A}$
- $Q_{GD} = 1.3 \text{ nC (typ)}$

2. Pinning information

Table 1: Pinning

Pin	Description	Simplified outline	Symbol
1, 2, 5, 6	drain (D)		
3	gate (G)		
4	source (S)	 SOT457 (TSOP6)	 003aaa671



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3. Ordering information

Table 2: Ordering information

Type number	Package			Version
	Name	Description		
PMN50XP	TSOP6	plastic surface mounted package (TSOP6); 6 leads		SOT457

4. Limiting values

Table 3: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage	$25^{\circ}\text{C} \leq T_j \leq 150^{\circ}\text{C}$	-	-20	V
V_{DGR}	drain-gate voltage (DC)	$25^{\circ}\text{C} \leq T_j \leq 150^{\circ}\text{C}; R_{GS} = 20\text{ k}\Omega$	-	-20	V
V_{GS}	gate-source voltage		-	± 12	V
I_D	drain current	$T_{sp} = 25^{\circ}\text{C}; V_{GS} = -4.5\text{ V}$; see Figure 2 and 3	-	-4.8	A
		$T_{sp} = 100^{\circ}\text{C}; V_{GS} = -4.5\text{ V}$; see Figure 2	-	-3	A
I_{DM}	peak drain current	$T_{sp} = 25^{\circ}\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; see Figure 3	-	-19.4	A
P_{tot}	total power dissipation	$T_{sp} = 25^{\circ}\text{C}$; see Figure 1	-	2.2	W
T_{stg}	storage temperature		-55	+150	$^{\circ}\text{C}$
T_j	junction temperature		-55	+150	$^{\circ}\text{C}$
Source-drain diode					
I_S	source current	$T_{sp} = 25^{\circ}\text{C}$	-	-1.9	A
I_{SM}	peak source current	$T_{sp} = 25^{\circ}\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	-7.5	A