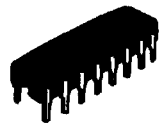
HD44270P/CP Series

Single Chip CODEC/Filter Combo LSI

HD44270P Series



(DP-16A)

HD44270CP Series

(CP-18)

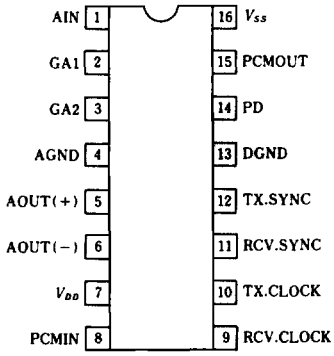
■FEATURES

- Single Chip CMOS CODEC with Filter in 16-pins DIL Package and 18-pins PLCC package.
- Power Supply Voltage ±5V±5%, Low Power Dissipation.
- μ-Law (HD44272P/CP, HD44274P/CP, HD44278P/CP)
  A-Law (HD44271P/CP, HD44273P/CP, HD44277P/CP)
- Extremely Low Cost for the Digital PBX Terminal or Digital Handset Application.
- Internal Clock Generator.
- Anti-Aliasing Filter (2nd order CR Active Filter).
- Voltage Reference (Internal-Trimmed).
- Input Amplifier with Uncommitted Plus/Minus Terminals.
- Auto-Zero Cancel Circuit without External Component.
- Push/Pull Analog Output.

Type	Comp. Law	Power (Typ.)	Clock			Input Amp	Output Amp	
			Internal clock	Sync/Async Operation	PCM bit clock rate		Type	Min load
HD44271P/CP	A	70mW	PLL Included	Both	64-2048kHz	Fully Uncommited Op-amp	Push-Pull	600Ω
HD44272P/CP	μ	70mW						
HD44273P/CP	A	50mW	Divider Included		1536/1544/2048 kHz		Single Ended	
HD44274P/CP	μ	50mW						
HD44277P/CP	A	50mW	PLL Included		64-2048kHz			
HD44278P/CP	μ	50mW						

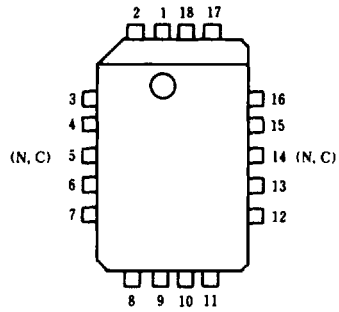
■ PIN ARRANGEMENT

●HD44271P/272P



(Top View)

●HD44271CP/272CP



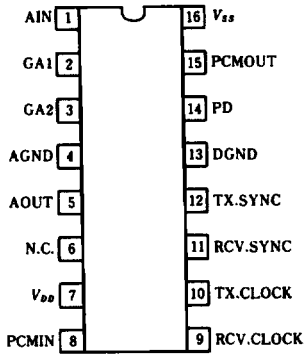
(Top View)

■ PIN DESCRIPTIONS

No. P	No. CP	Symbol	Function	Remarks
1	1	AIN	Analog input	
2	2	GA1	Gain adjust 1	Feed-back input
3	3	GA2	Gain adjust 2	10kΩ < R_L, C_L < 100pF
4	4	AGND	Analog ground	
5	6	AOUT(+)	Analog output	R_L > 600Ω, C_L < 100pF
6	7	AOUT(−)		R_L > 600Ω, C_L < 100pF
7	8	V_{DD}	Positive pow. sup.	5V ± 5%
8	9	PCMIN	PCM data input	(TTL)
9	10	RCV. CLK	PCM bit clock	(TTL)64kHz to
10	11	TX. CLK		2048kHz
11	12	RCV. SYNC	Synchronization	(TTL) 8kHz
12	13	TX. SYNC		
13	15	DGND	Digital ground	
14	16	PD	Power down	(TTL) "0" = down
15	17	PCMOUT	PCM data output	Open drain
16	18	V_{SS}	Negative pow. sup.	−5V ± 5%
—	5, 14	N.C.	—	Open

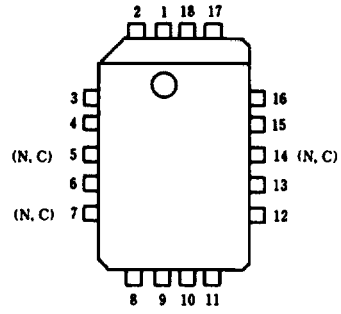
■PIN ARRANGEMENT

● HD44273P/274P



(Top View)

● HD44273CP/274CP



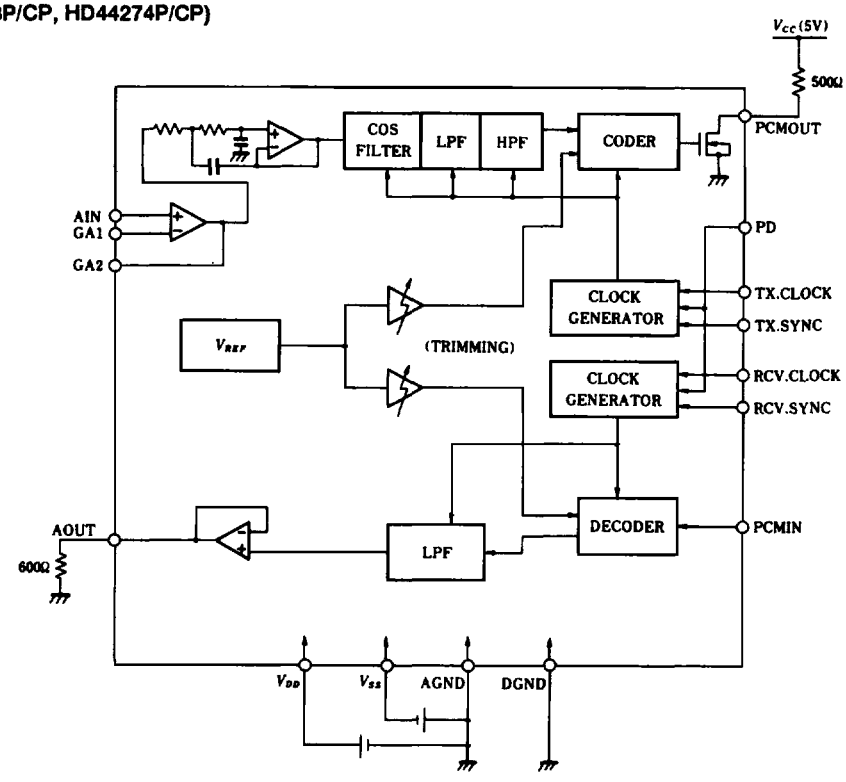
(Top View)

■PIN DESCRIPTIONS

No. P	No. CP	Symbol	Function	Remarks
1	1	AIN	Analog input	
2	2	GA1	Gain adjust 1	Feed-back input
3	3	GA2	Gain adjust 2	10kΩ < R_L C_L < 100pF
4	4	AGND	Analog ground	
5	6	AOUT	Analog output	R_L > 600Ω, C_L < 100pF
7	8	V_{DD}	Positive pow. sup.	5V ± 5%
8	9	PCMIN	PCM data imput	(TTL)
9	10	RCV. CLK	PCM bit clock	(TTL) 2048/1544/ 1536kHz
10	11	TX. CLK		
11	12	RCV. SYNC	Synchronization	(TTL) 8kHz
12	13	TX. SYNC		
13	15	DGND	Digital ground	
14	16	PD	Power down	(TTL) "0" = down
15	17	PCMOUT	PCM data output	Open drain
16	18	V_{SS}	Negative pow. sup.	−5V ± 5%
6	5, 7, 14	N.C.	—	Open

■BLOCK DIAGRAM

(HD44273P/CP, HD44274P/CP)



■PIN/FUNCTION DESCRIPTIONS

HD44271P/CP, HD44272P/CP, HD44277P/CP, HD44278P/CP

Pin	No		Descriptions
	P	CP	
TX. CLOCK RCV. CLOCK	9 10	10 11	Any of 64kHz to 2.048MHz clock can be accepted with the pins. And they are automatically divided down to provide the internal clocks. These TTL compatible inputs shift PCM data out of the coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the TX. SYNC/RCV. SYNC respectively.
TX. SYNC RCV. SYNC	11 12	12 13	These TTL compatible pulse inputs (typ. 8kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the TX.CLOCK/RCV.CLOCK with these positive going edges occurring after the falling edge of the TX.CLOCK/RCV. CLOCK respectively. The width of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.
PCMOUT	15	17	This is a LS-TTL compatible open-drain output. It is active only during transmission of PCM output for 8 bit periods of CLOCK, TX.CLOCK/RCV.CLOCK signal following a positive edge on the SYNC, TX/SYNC. RCV. SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500 Ω pull-up per 8 CODECs is required.
PCMIN	8	8	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of RCV. CLOCK.
AIN GA1 GA2	1 2 3	1 2 3	These three pins are provided for connecting analog signals in the range of $-V_{REF}$ to $+V_{REF}$ to the device The input stage can be connected as a unity gain amplifier, with gain or amplifier with adjustable gain. The adjustable gain configuration will facilitate calibration of the transmit channel. AIN is the input of analog signal of the amplifier. GA2 is the output of the amplifier. GA2 shall be loaded by the resistor above 10k Ω or directly connected to GA1. GA1 is the negative feed back input of the amplifier. C_L should be less than 100 pF.
AOUT(+)	5	6	This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600 Ω. C_L should be less than 100pF.
V_{DD} V_{SS} AGND DGND	7 16 4 13	8 18 4 15	These are power supply pins. V_{DD} and V_{SS} are positive and negative supply pins respectively (typ. +5V, −5V). Analog and digital ground pins are separate for minimizing crosstalk.
PD	14	16	This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect.
AOUT(−)*	6	7	This is the inverted output of pin 5 signal output to drive the 600 Ω transformer as the push-pull operation. $R_L < 600Ω$, $C_L < 100pF$.

*ONLY FOR HD44271, 272P/CP

■PIN/FUNCTION DESCRIPTIONS

HD44273P/CP, HD44274P/CP

Pin	No		Descriptions
	P	CP	
TX. CLOCK RCV. CLOCK	9 10	10 11	One of 1.536, 1.544 and 2.048MHz clock can be accepted with the pins. And they are automatically divided down to provide the internal clocks. These TTL compatible inputs shift PCM data out of the coder on the positive going edges and PCM data into the decoder on the negative going edges after receiving a positive edge on the TX. SYNC/RCV. SYNC respectively.
TX. SYNC RCV. SYNC	11 12	12 13	These TTL compatible pulse inputs (typ. 8kHz) are used for analog sampling and for initiating the PCM output from the coder and initiate clocking of PCM input data into the decoder. They must be synchronized with the TX.CLOCK/RCV.CLOCK with these positive going edges occurring after the falling edge of the TX.CLOCK/RCV. CLOCK respectively. The width of these signals are not critical. An internal bit counter generates the necessary timing for PCM output and input.
PCMOUT	15	17	This is a LS-TTL compatible open-drain output. It is active only during transmisson of PCM output for 8 bit periods of CLOCK, TX.CLOCK/RCV.CLOCK signal following a positive edge on the SYNC, TX/SYNC. RCV. SYNC input. Data is clocked out by the positive edge of the CLOCK. One 500 Ω pull-up per 8 CODECs is required.
PCMIN	8	9	This is a TTL compatible input for supplying PCM input data to the decoder. Data is clocked in by the negative edge of RCV. CLOCK.
AIN GA1 GA2	1 2 3	1 2 3	These three pins are provided for connecting analog signals in the range of $-V_{REF}$ to $+V_{REF}$ to the device. The input stage can be connected as a unity gain amplifier, with gain or amplifier with adjustable gain. The adjustable gain configuration will facilitate calibration of the transmit channel. AIN is the input of analog signal of the amplifier. GA2 is the output of the amplifier. GA2 shall be loaded by the resistor above 10k Ω or directly connected to GA1. GA1 is the negative feed back input of the amplifier. C_L should be less than 100 pF.
AOUT	5	6	This is the buffered output of the recreated analog signal from the received PCM data words. It can drive the impedance of 600 Ω. C_L should be less than 100pF.
V_{DD} V_{SS} AGND DGND	7 16 4 13	8 18 4 15	These are power supply pins. V_{DD} and V_{SS} are positive and negative supply pins respectively (typ. +5V, −5V). Analog and digital ground pins are separate for minimizing crosstalk.
PD	14	16	This TTL compatible input when held low puts the chip into the powered down mode regardless of strobes. The chip will also power down if the strobes stop. The strobes can be high, low or floating, but as long as they are static, the powered down mode is in effect.

■ABSOLUTE MAXIMUM RATINGS

Item	Rating
V_{DD}	−0.3 to +7V
V_{SS}	+0.3 to −7V
Storage temperature	−55°C to +125°C
Power dissipation	0.5W
Digital input/output voltage	$-0.3V < V_{IN} < V_{DD}+0.3V$
Analog input/output voltage	$V_{SS}-0.3V < V_{IN} < V_{DD}+0.3V$

■ELECTRICAL CHARACTERISTICS

●STATIC CHARACTERISTICS ($V_{DD}=5\pm0.25V$, $V_{SS}=-5\pm0.25V$, $V_{CC}=5\pm0.25V$, $T_a=0$ to $+70°C$)

Descriptios	Symbol	P	CP	min	typ	max	Note/condition	Unit
V_{DD} current (ope.)	I_{DD}	7	8	–	8.0	13.5	Note 1 AIN = 0V PCMIN = +0code R_L (GA2) = 10k Ω R_L (AOUT) = 600 Ω	mA
V_{SS} current (ope.)	I_{SS}	16	18	−13.0	−7.5	–		
V_{DD} current (st.by.)	I_{DDST}	7	8	–	0.4	1.0		
V_{SS} current (st.by.)	I_{SSST}	16	18	−0.2	–	–		
Leak current	I_L	1, 2, 8	1, 2, 9	−10.0	–	10.0	V_M = 0.8V	μA
		9, 10	10, 11	−10.0	–	10.0	V_M = 2.0V	μA
		14	16	–	–	10.0	V_{DD} = V_M = 5.25V	μA
Pull up current	I_{PL}	11, 12	12, 13	−100	–	0		μA
Leak current	I_{DL}	15	17	–	–	10.0	V_{DD} = V_M = 5.25V	μA
Analog input cap.	C_{AIN1}	1	1	–	–	10	at 1MHz Vbias = 0	pF
Analog input cap.	C_{AIN2}	2	2	–	–	10	at 1MHz Vbias = 0	pF
Input capacitance	C_{DIN}	8,9,10,11,12,14	9,10,11,12,13,16	–	–	10	at 1MHz Vbias = 0	pF
AOUT resistance	R_{OUTA}	5, (6)	6, (7)	–	1	20		Ω
GA2 resistance	R_{OUTG}	3	3	–	–	50	Note 1	Ω
GA2 output swing	V_{GSW}	3	3	−3.0	–	3.0	R_L = 10kΩ	V
Analog offset input	V_{OFFIN}	1	1	−200	–	200	Note 1	mV
GA2 offset output	V_{OFFG}	3	3	−50	–	50	Note 1	mV
AOUT offset output	V_{OFFA}	5, (6)	6, (7)	−100	–	100	PCMIN = +0 code	mV
PCMOUT capacitance	C_{DOUT}	15	17	–	–	15.0	at 1MHz, Vbias = 0V	pF
PCMOUT low voltage	V_{OL}	15	17	–	–	0.4	R_L = 500Ω, $+I_{OL}$ = 0.8mA	V
PCMOUT high voltage	V_{OH}	15	17	V_{CC} −3.0	–	–	I_{OH} = −150μA	V
Digital input high voltage	V_{IH}	8,9,10,11,12,14	9,10,11,12,13,16	2.0	–	–		V
Digital input low voltage	V_{IL}	8,9,10,11,12,14	9,10,11,12,13,16	–	–	0.8		V

Note 1) Analog input amplifier gain = 0 dB (GA1 is connected to GA2)

( ) : Only for HD44271, 272P/CP

●DYNAMIC-CHARACTERISTICS (V_{DD} = 5 ± 0.25V, V_{SS} = −5 ± 0.25V, V_{CC} = 5 ± 0.25V, T_a = 0 to +70°C)

Descriptions	Symbol	Note	min	typ	max	Unit
Synchronization rate	F_S		–	8	–	kHz
PCM bit clock rate	F_C		64	–	2048	kHz
Clock pulse width	t_{wc}		200	–	–	ns
Sync pulse high width	t_{wSH}		200	–	–	ns
Sync pulse low width	t_{wSL}		8	–	–	ns
Logic input rise time	t_r		5	–	50	ns
Logic input fall time	t_f		5	–	50	ns
Previous clock to Sync delay	t_{hCS}	Note 1	40	–	–	ns
Clock to sync delay	t_{cs}	Note 1, 3	–	–	100	ns
Clock to PCM MSB delay	t_{cdd}	Note 1, 2, 4	–	–	170	ns
Sync to PCM MSB delay	t_{sd}	Note 1, 2, 4	–	–	170	ns
Clock to PCM OUT delay	t_{cd}	Note 1, 2, 5	–	–	180	ns
PCMIN setup time	t_{su}	Note 1	65	–	–	ns
PCMIN hold time	t_{hd}	Note 1	120	–	–	ns

Note 1) t_r, t_f of digital input or clock is assumed 5ns for timing measurement.
2) PCMOUT load condition: 500Ω + 165pF + two LS-TTL Equivalent (I_{IL} = 0.8mA, I_{IH} = −150μA) Threshold level (V_{OH} = 2.4V, V_{OL} = 0.4V)
3) Positive value shows SYNC delay from CLOCK.
4) t_{cdd}, t_{sd} are specified by CLOCK or SYNC which has slower rise time.
5) t_{cd} specification is valid for the data except MSB.

●SYSTEM RELATED CHARACTERISTICS

(V_{DD} = 5 ± 0.25V, V_{SS} = −5 ± 0.25V, V_{CC} = 5 ± 0.25V, T_a = 0 to +70°C, INPUT AMPLIFIER GAIN = 0dB, ANALOG OUT PUT = AOUT(−), GA2 LOAD = 10kΩ, AOUT LOAD = 600Ω, Synchronous operation. **fc** (PCM BIT CLOCK) = 2048kHz)

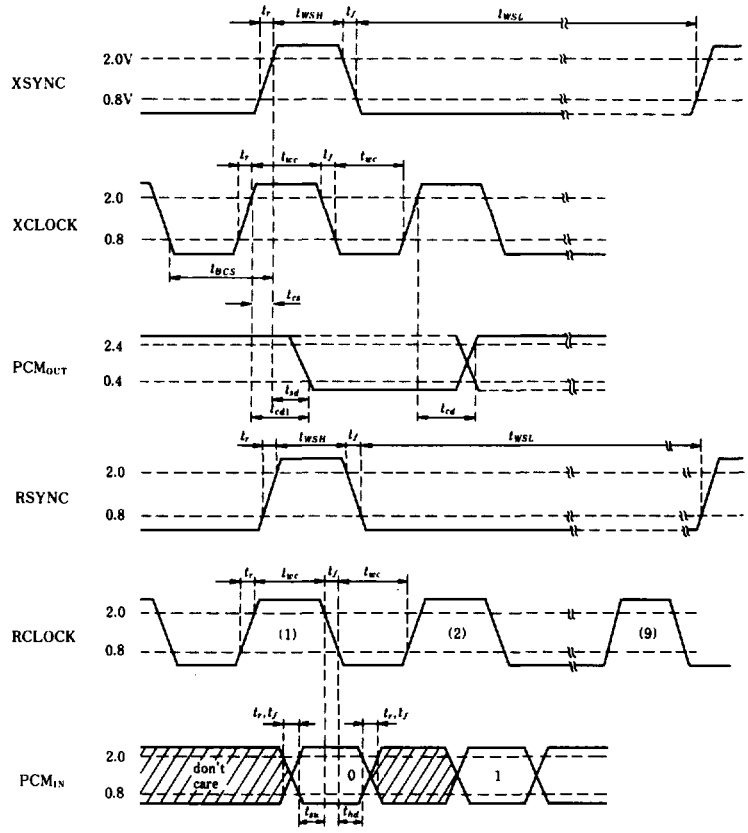
A-law (HD44271P/CP, HD44273P/CP, HD44277P/CP)

Descriptions	Symbol	Test conditions		min	typ	max	Unit	Note
Signal to dist.(A to A)	SDA	820Hz tone	−45dBm0	23	–	–	dB	p-wgt
			−40	28	–	–		
			−30, −20, −10,0	34	–	–		
Gain track. (A to A)	GTA	820Hz tone Relative to −10dBm0	−55dBm0	−1.0	–	1.0	dB	
			−50	−0.5	–	0.5		
			−40, −30, −20, −10,0,3	−0.3	–	0.3		
Freq. response. (A to D)(Loss)	FRX	Relative to 820Hz 0dBm0	0.06kHz	24	–	–	dB	
			0.2	0	–	2.5		
			0.3 to 3	−0.3	–	0.3		
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Freq. response.(D to A)(Loss)	FRR	Relative to 820Hz 0dBm0	0 to 3kHz	−0.3	–	0.3	dB	
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Analog input level variation	AIL	820Hz 0dBm0	Relative to 1.231 Vrms	−0.5	–	0.5	dB	
Analog output level	AOL	820Hz 0dBm0	Relative to 1.231 Vrms	−0.5	–	0.5	dB	
Idle ch. noise	ICNX	A to D	AIN = AGND	–	–	−80	dBm0P	
Idle ch. noise	ICNR	D to A	PCMIN = +0−Code	–	–	−80	dBm0P	
AIN to AOUT crosstalk	XTKA	820Hz	0dBm0	–	–	−65	dB	
PCMIN to PCMOUT	XTKD	820Hz	0dBm0	–	–	−65	dB	
PSRR	PSRR	A to A	0.3 to 50kHz	–	40	–	dB	

μ-law (HD44272P/CP, HD44274P/CP, HD44278P/CP)

Descriptions	Symbol	Test conditions		min	typ	max	Unit	Note
Signal to dist.(A to A)	SDA	1020Hz tone	−45dBm0	23	–	–	dB	c-wgt
			−40	28	–	–		
			−30, −20, −10,0	34	–	–		
Gain Tracking(A to A)	GTA	1020Hz tone relative to −10dBm0	−55dBm0	−1.0	–	1.0	dB	
			−50	−0.5	–	0.5		
			−40, −30, −20, −10,0,3	−0.3	–	0.3		
Freq.Response.(A to D)(Loss)	FRX	Relative to 1020Hz 0dBm0	0.06kHz	24	–	–	dB	
			0.2	0	–	2.5		
			0.3 to 3	−0.3	–	0.3		
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Freq.Response.(D to A)(Loss)	FRR	Relative to 1020Hz 0dBm0	0 to 3kHz	−0.3	–	0.3	dB	
			3.4	0	–	0.8		
			3.78	6.5	–	–		
Analog input level	AIL	1020Hz 0dBm0	Relative to 1.227 Vrms	−0.5	–	0.5	dB	
Analog output level	AOL	1020Hz 0dBm0	Relative to 1.227 Vrms	−0.5	–	0.5	dB	
Idle ch. noise	ICNX	A to D	AIN = AGND	–	–	16	dBrnC0	
Idle ch. noise	ICNR	D to A	PCMIN = +0−code	–	–	10	dBrnC0	
AIN to AOUT crosstalk	XTKA	1020Hz 0dBm0		–	–	−65	dB	
PCMIN to PCMOUT crosstalk	XTKD	1020Hz 0dBm0		–	–	−65	dB	
PSRR	PSRR	A to A	0.3 to 50kHz	–	40	–	dB	

■TIMING CHART



Notes on Using CODEC LSIs

This section discusses protection procedures that should be considered when using CODEC devices.

Latchup Protection: Latchup is a thyristor phenomenon, unique to CMOS structures, caused by parasitic pnp or npn transistors. Since all Hitachi CODEC LSIs employ CMOS structure, general latchup protection is useful.

A CODEC has four power supply pins: AGND, DGND, V_{DD}, and V_{SS}. Power should be applied to these pins in the proper order. Voltage exceeding the absolute maximum ratings may cause damage to the device.

Inserting Boards: Special care should be taken when inserting or replacing a board containing CODECs with the system power on. When the usual slow-starting power supply is turned on, voltages at each part of the board change slowly. Accordingly, a reverse current seldom exceeds the maximum rating. However, when a board is inserted with the power on, a rapid voltage change can occur. This might cause device destruction, thermally dis-connecting V_{DD} or V_{SS} on the device.

In the case of V_{DD} disconnection, substrate bias is derived from I/O pins (because of the substrate's CMOS characteristics) resulting in unstable operation with the S/N ratio reduced. Thus, hot line insertion is not recommended from the standpoint of reliability. If this is unavoidably required, the following must be considered. Hitachi CODEC HD44230 and 240 series incorporate an inverse potential prevention circuit to prevent V_{SS} pin voltage from rising. This circuit can effectively prevent device destruction caused through hot line insertion.

During power up sequence where a +5 V V_{DD} pin is set up first, part of the negative supply current is dissipated to temporarily activate the prevention circuit. Thus, ensure that the current capacity is high enough to set up the transition at power up.

When power must be applied to a large number of lines, the current capacity margin must set up –5 V at the V_{SS} pin. After the power up sequence is complete, the current flowing in the prevention circuit is cut off. Accordingly, the current of the rated input voltage is specified as a supply current in individual data sheets. In Hitachi CODECs, a sufficient current capacity is preserved at the negative power set up by simultaneously setting up two different types of slow-starter power supplies or by first setting up a –5 V V_{SS} pin.

DGND and AGND Connection on a Board: It is usually recommended that bypass capacitors be inserted between DGND and V_{DD} and between AGND and V_{SS}. However, CMOS structure is also formed between DGND and V_{DD}. If DGND and AGND are connected separately on a board, the impedance between V_{DD} and DGND becomes higher, which increases the possibility of latchup generated by noise during power up. The best way to prevent this is to connect the DGND and V_{DD} pins together just before the CODEC. If the two lines are separately traced, they can be connected together just before the socket.

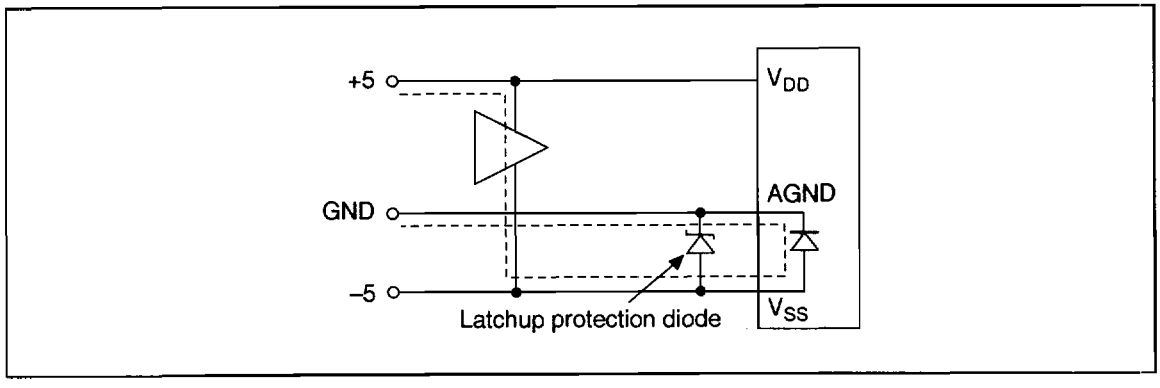


Figure 1 Latchup Protection Diode

Insertion of Diodes against Inverse Voltage: If devices such as resistors and operational amps are inserted between V_{DD} and V_{SS}, current flows in the path of V_{DD} to V_{SS} to AGND/DGND through parasitic diodes in the CODEC (figure 1). To eliminate this current, it is recommended that a diode such as a Schottky diode be placed to suppress the voltage between AGND and V_{SS} to under 0.5 V. The current capacity of the diode should be determined based on the amount of current flowing from external circuits.

Currents Flowing from Other Power Supplies: Power supplies available on the CODEC board include ±12 V, ±15 V, and –4.8 V. These supplies may overdrive the ±5 V CODEC I/O pins. Usually, the current flowing through devices is not large enough to cause latchup, but care should be taken.

Bypass Capacitors: When bypass capacitors are inserted between different power supplies, the potential may be inversed temporarily depending on the order in which the supplies are turned on (figure 2). The following phenomenon can occur:

1. With capacitors placed between the V_{DD}, V_{SS}, and AGND pins, when V_{DD} and GND are powered with V_{SS} open, V_{SS} potential will rise to $V_{DD} \times C1/(C1 + C2)$, which may raise V_{SS} to a positive potential. However, a fairly large capacitance is required for potential inversion.
2. In an application with a bypass capacitor between a –4.8 V power supply and the GND, when –4.8 volts are applied with GND open, the GND potential may be pulled up to –4.8 V and exceed the V_{SS} (–5 V).

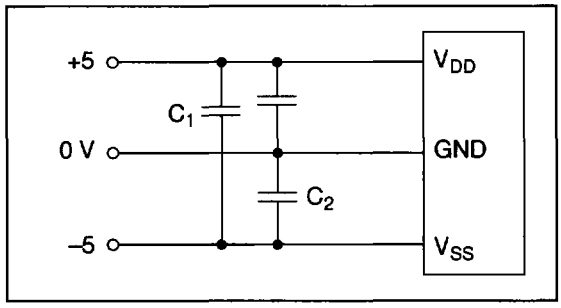


Figure 2 Bypass Capacitors

The more power supplies are used, the more cases of inverse potential should be considered. Inverse potential can be prevented by providing larger bypass capacitors between V_{DD} and GND (including AGND and DGND) and between GND and V_{SS}.

Inserting the CODEC into a Socket: Power should be turned off before the CODEC is inserted into a socket. Insertion with power on may destroy the CODEC because the bypass capacitors have no effect.

Connecting to a Transformer or Coil: Special care should be taken when connecting a transformer for a audio circuit with the CODEC. A voltage beyond the power supply voltage may be applied to the inputs when:

- Rush currents are caused by intermittent currents through a telephone circuit
- Lightning surge leakage exists between coils
- Substrate potential has risen

The circuit in figure 3 can effectively prevent this problem. The peak voltage can be suppressed by a

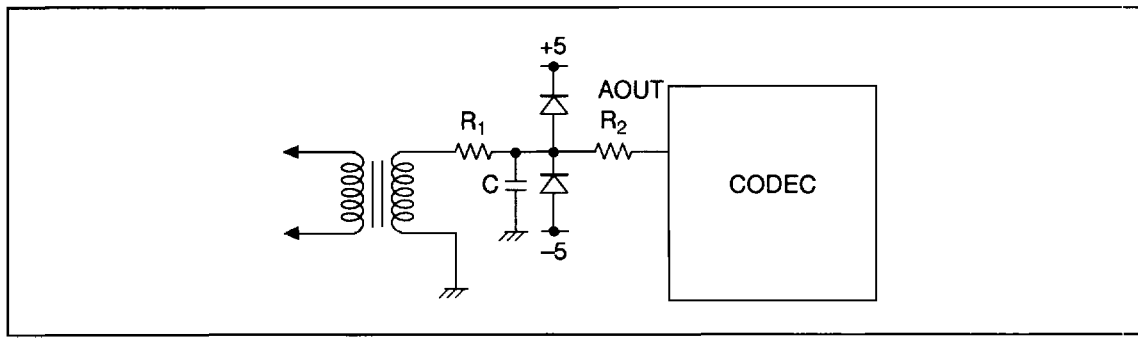


Figure 3 Surge Prevention Circuit

filter consisting of R1 and C (floating capacitance only is sufficient) and clamped by diodes. This prevents AOUT or AIN from being overdriven. Most cases do not require R2.

When long lines are connected to CODEC pins, such as a microphone input and earphone output, these pins should be protected from noise such as external spikes. When piezo elements are used for the microphone and earphone pins, these pins should also be protected from the piezo effect when stress is applied.

Digital Output: Digital output pins employ open drain structure, but the substrate (well) is connected to DGND. Accordingly, voltages below DGND (0 V) at these pins may cause latchup. Additionally, loading capacitance and transmission reflection effects should be considered. Since a diode is provided between V_{DD} and digital outputs, pull-up voltage must not exceed V_{DD}.