Datasheet

1. Features

- **Dual ADC with 8-bit Resolution**
- **1 Gsps Sampling Rate per Channel, 2 Gsps in Interleaved Mode**
- **Single or 1:2 Demultiplexed Output**
- **LVDS Output Format (100Ω)**
- **500 mVpp Analog Input (Differential Only)**
- **Differential or Single-ended 50Ω PECL/LVDS Compatible Clock Inputs**
- **Power Supply: 3.3V (Analog), 3.3V (Digital), 2.25V (Output)**
- **LQFP144 or LQFP-ep 144L Green Packages**
- **Temperature Range:**
  - **0°C < T_{amb} < 70°C (Commercial Grade)**
  - **–40°C < T_{amb} < 85°C (Industrial Grade)**
- **3-wire Serial Interface**
  - **16-bit Data, 3-bit Address**
  - **1:2 or 1:1 Output Demultiplexer Ratio Selection**
  - **Full or Partial Standby Mode**
  - **Analog Gain (± 1.5 dB) Digital Control**
  - **Input Clock Selection**
  - **Analog Input Switch Selection**
  - **Synchronous Data Ready Reset**
  - **Data Ready Delay Adjustable on Both Channels**
  - **Interleaving Functions:**
    - **Offset and Gain (Channel to Channel) Calibration**
    - **Digital Fine SDA (Fine Sampling Delay Adjust) on One Channel**
  - **Internal Static or Dynamic Built-In Test (BIT)**

2. Performance

- **Low Power Consumption: 0.75W Per Channel**
- **Power Consumption in Standby Mode: 120 mW**
- **1.5 GHz Full Power Input Bandwidth (–3 dB)**
- **Flat ENOB (DC to 1 GHz)**
- **SNR = 45 dB Typ (7.2 bit ENOB), THD = –51 dBc, SFDR = –54 dBc at Fs = 1 Gsps Fin = 500 MHz**
- **2-tone IMD3: –54 dBc (499 MHz, 501 MHz) at 1 Gsps**
- **DNL = 0.25 LSB, INL = 0.5 LSB**
- **Low Bit Error Rate (10^{-13}) at 1 Gsps**

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AT84AD001C

3. Application

- **Digital Oscilloscopes**
- **Communication Receivers (I/Q)**
- **Direct RF Down Conversion**
- **High Speed Data Acquisition**

4. Description

The AT84AD001C is a monolithic dual 8-bit analog-to-digital converter, offering low 1.56W power consumption and excellent digitizing accuracy. It integrates dual on-chip track/holds that provide an enhanced dynamic performance with a sampling rate of up to 1 Gsps and an input frequency bandwidth of over 1.5 GHz. The dual concept, the integrated demultiplexer and the easy interleaving mode make this device user-friendly for all dual channel applications, such as direct RF conversion or data acquisition. The *smart* function of the 3-wire serial interface eliminates the need for external components, which are usually necessary for gain and offset tuning and setting of other parameters, leading to space and power reduction as well as system flexibility.

5. Functional Description

The AT84AD001C is a dual 8-bit 1 Gsps ADC based on advanced high-speed BiCMOS technology.

Each ADC includes a front-end analog multiplexer followed by a Sample and Hold (S/H), and an 8-bit flash-like architecture core analog-to-digital converter. The output data is followed by a switchable 1:1 or 1:2 demultiplexer and LVDS output buffers (100Ω).

Two over-range bits are provided for adjustment of the external gain control on each channel.

A 3-wire serial interface (3-bit address and 16-bit data) is included to provide several adjustments:

- Analog input range adjustment (±1.5 dB) with 8-bit data control using a 3-wire bus interface (steps of 0.011 dB)
- Analog input switch: both ADCs can convert the same analog input signal I or Q
- Output format: DMUX 1:1 or 1:2 with control of the output frequency on the data ready output signal
- Partial or full standby on channel I or channel Q
- Clock selection:
    - Two independent clocks: CLKI and CLKQ
    - One master clock (CLKI) with the same phase for channel I and channel Q
    - One master clock but with two phases (CLKI for channel I and CLKIB for channel Q)
- ISA: Internal Settling Adjustment on channel I and channel Q
- FiSDA: Fine Sampling Delay Adjustment on channel Q (in interleaving mode)
- Adjustable Data Ready Output Delay on both channels
- Test mode: decimation mode (by 16), Built-In Test

A calibration phase is provided to set the two DC offsets of channel I and channel Q close to code 127.5 and calibrate the two gains. This calibration might be launched several times before the optimum is reached. The offset and gain error can also be set externally via the 3-wire serial interface.

The AT84AD001C operates in fully differential mode from the analog inputs up to the digital outputs. The AT84AD001C features a full-power input bandwidth of 1.5 GHz.

Figure 5-1. Simplified Block Diagram

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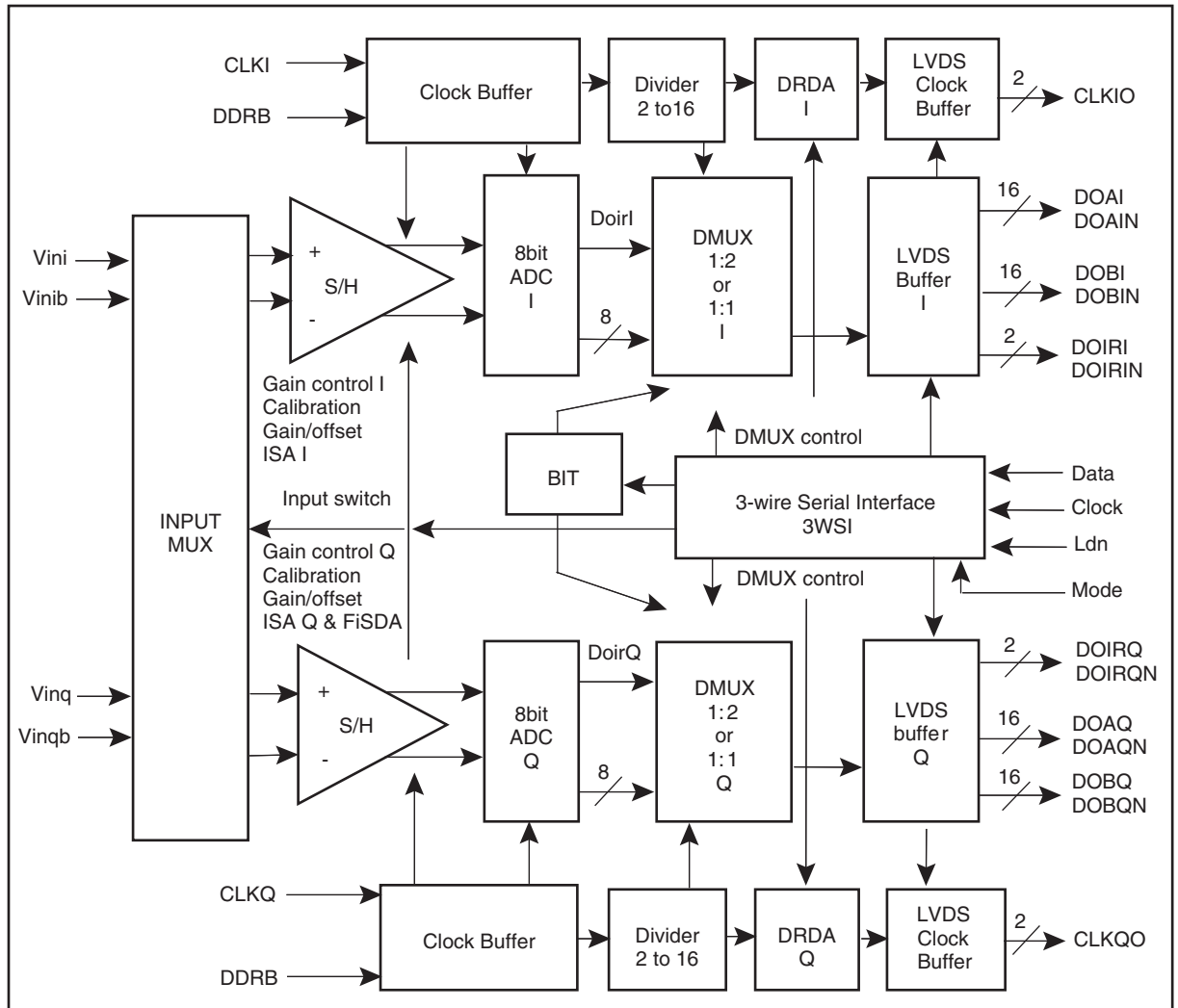
6. Typical Applications

Figure 6-1. Satellite Receiver Application
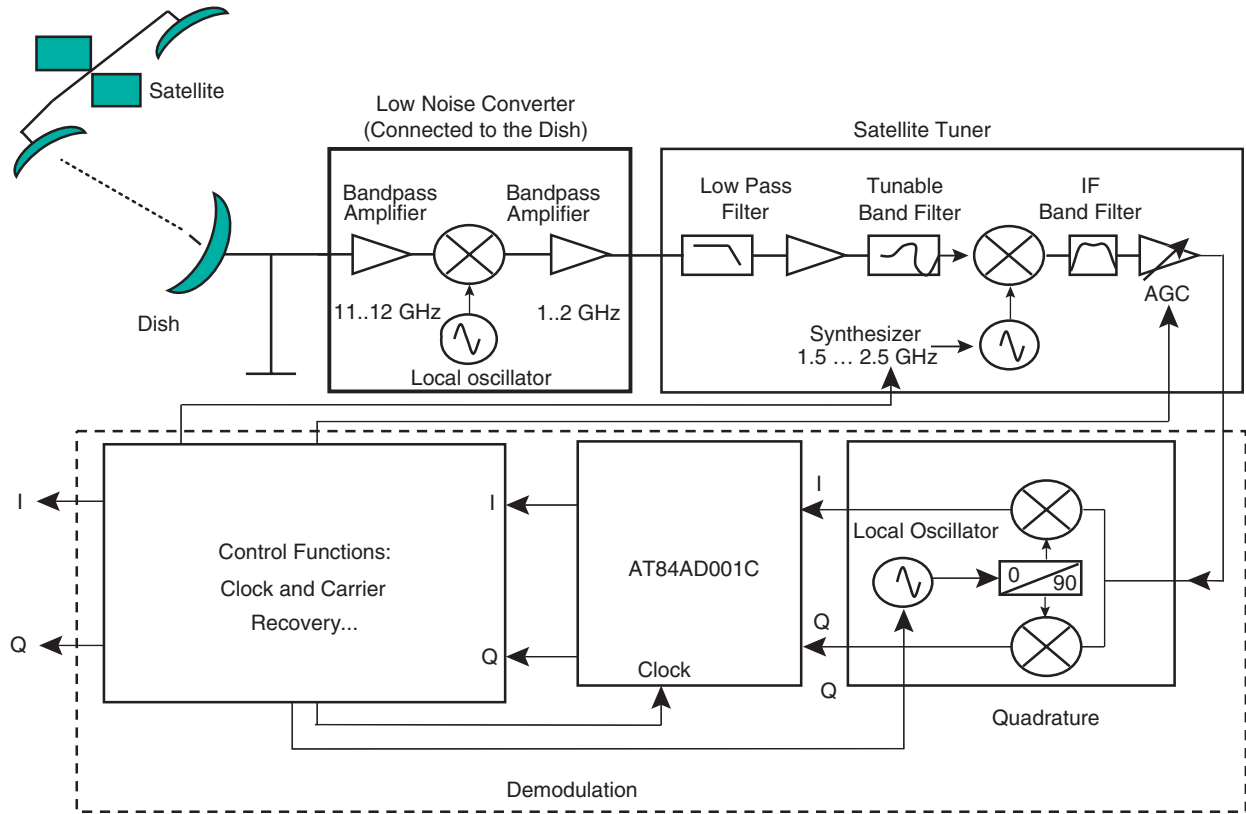
Figure 6-2. Dual Channel Digital Oscilloscope Application

AT84AD001C
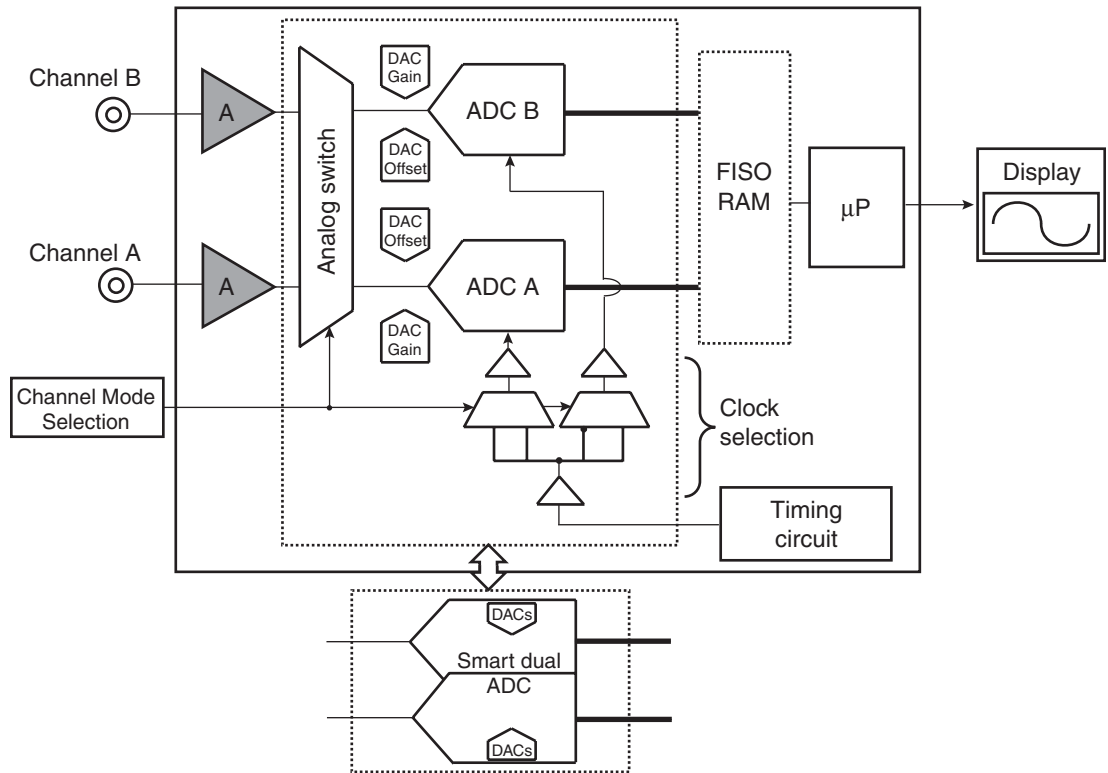
Table 6-1. Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Analog positive supply voltage	V_{CCA}	3.6	V
Digital positive supply voltage	V_{CCD}	3.6	V
Output supply voltage	V_{CCO}	3.6	V
Maximum difference between V_{CCA} and V_{CCD}	V_{CCA} to V_{CCD}	± 0.8	V
Minimum V_{CCO}	V_{CCO}	1.6	V
Analog input voltage	V_{INI} or V_{INIB} V_{INQ} or V_{INQB}	1/–1	V
Digital input voltage	V_D	–0.4 to V_{CCD} + 0.4	V
Clock input voltage	V_{CLK} or VC_{LKB}	–0.4 to V_{CCD} + 0.4	V
Maximum difference between V_{CLK} and V_{CLKB}	$V_{CLK} - V_{CLKB}$	–2 to 2	V
Maximum junction temperature	T_J	125	°C
Storage temperature	T_{stg}	–55 to 150	°C
Lead temperature (soldering 10s)	T_{leads}	300	°C

Note: Absolute maximum ratings are limiting values (referenced to GND = 0V), to be applied individually, while other parameters are within specified operating conditions. Long exposure to maximum ratings may affect device reliability.

Table 6-2. Recommended Conditions of Use

Parameter	Symbol	Comments	Recommended Value	Unit
Analog supply voltage	V_{CCA}		3.3	V
Digital supply voltage	V_{CCD}		3.3	V
Output supply voltage	V_{CCO}		2.25	V
Differential analog input voltage (full-scale)	$V_{INi} - V_{IniB}$ or $V_{INQ} - V_{INQB}$		500	mVpp
Differential clock input level	Vinclk		600	mVpp
Internal Settling Adjustment (ISA) with a 3-wire serial interface for channel I and channel Q	ISA	1:1 DMUX	0	ps
		1:2 DMUX	–100	ps
Operating temperature range	$T_{Ambient}$	Commercial grade Industrial grade	$0 < T_{amb} < 70$ $-40 < T_{amb} < 85$	°C

7. Electrical Operating Characteristics

Unless otherwise specified:

- V_{CCA} = 3.3V; V_{CCD} = 3.3V; V_{CCO} = 2.25V
- $V_{INI} - V_{INB}$ or $V_{INQ} - V_{INQB}$ = 500 mVpp full-scale differential input
- LVDS digital outputs (100Ω)
- T_{amb} (typical) = 25°C
- Full temperature range: 0°C < T_{amb} < 70°C (commercial grade)

Table 7-1. Electrical Operating Characteristics in Nominal Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Resolution			8		Bits
Coding			Binary		
Power Requirements					

Positive supply voltage
    - Analog
    - Digital
    -Output digital (LVDS) and serial interface
	V_{CCA}
	V_{CCD}
	V_{CCO}
		3.15
		3.15
		2.0
			3.3
			3.3
			2.25
				3.45
				3.45
				2.5
					V
					V
					V

Supply current (1:1 DMUX mode, 1 clock)
    - Analog
    - Digital
    - Output
	I_{CCA}
	I_{CCD}
	I_{CCO}
			145
			248
			88
				179
				274
				119
					mA
					mA
					mA

Supply current (1:2 DMUX mode, 2 clocks)
    - Analog
    - Digital
    - Output
	I_{CCA}
	I_{CCD}
	I_{CCO}
			145
			296
			158
				179
				349
				214
					mA
					mA
					mA

Supply current (1:2 DMUX mode, 1 clock)
    - Analog
    - Digital
    - Output
	I_{CCA}
	I_{CCD}
	I_{CCO}
			145
			272
			154
				179
				309
				209
					mA
					mA
					mA

Supply current (1:1 DMUX mode, partial standby)
    - Analog
    - Digital
    - Output
	I_{CCA}
	I_{CCD}
	I_{CCO}
			79
			170
			48
				94
				189
				64
					mA
					mA
					mA

Supply current (1:2 DMUX mode, partial standby)
    - Analog
    - Digital
    - Output
	I_{CCA}
	I_{CCD}
	I_{CCO}
			79
			157
			81
				94
				204
				109
					mA
					mA
					mA

Supply current (Full Standby)
    - Analog
    - Digital
    - Output
	I_{CCA}
	I_{CCD}
	I_{CCO}
			14
			20
			4.3
				19
				38
				6.5
					mA
					mA
					mA

Nominal dissipation (1 clock, 1:1 DMUX mode, 2 channels)	P_D		1.5		W
Nominal dissipation (full standby mode)	stbpd		120		mW
Nominal Power dissipation (1 clock, 1:2 DMUX)	P_D		1.7		W

Table 7-1. Electrical Operating Characteristics in Nominal Conditions (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Analog Inputs					
Full-scale differential analog input voltage to obtain full scale with no gain adjust (mode 0)[1]	V_{Dp-p}	450	500	550	mV
Analog input common mode			0		V
Analog input capacitance I and Q	C_{IN}			2	pF
Full power input bandwidth (–3 dB)	FPBW		1.5		GHz
Gain flatness (–0.5 dB)			500		MHz
Clock Input					
Logic compatibility for clock inputs and DDRB reset (pins 124,125,126,127,128,129) in AC coupling mode		PECL/ECL/LVDS			
PECL/LVDS clock inputs and DDRB input voltages ($V_{CLKI/IN}$ or $V_{CLKQ/QN}$) Differential logical level	$V_{IL} - V_{IH}$		600		mV
Clock input and DDRB input power level		–9	0	6	dBm
Clock input capacitance			2		pF
Digital Outputs (including DOIRI, DOIRIN, DOIRQ and DOIRQN signals)					
Logic driving compatibility for digital outputs (depending on the value of V_{CCO})		LVDS			
Differential output voltage swings (assuming V_{CCO} = 2.25V)	V_{OD}	220	270	350	mV
Output levels (assuming V_{CCO} = 2.25V) 100Ω differentially terminated Logic 0 voltage Logic 1 voltage	V_{OL} V_{OH}	1.0 1.25	1.1 1.35	1.2 1.48	V V
Output offset voltage (assuming V_{CCO} = 2.25V) 100Ω differentially terminated	V_{OS}	1125	1250	1340	mV
Output impedance	R_O		50		Ω
Output current (shorted output)				12	mA
Output current (grounded output)			30		mA
Output level drift with temperature			1.3		mV/°C
Digital Input (Serial Interface)					
Maximum clock frequency (input clk)	Fclk			50	MHz
Input logical level 0 (clk, mode, data, ldn)		–0.4	0	0.4	V
Input logical level 1 (clk, mode, data, ldn)		V_{CCO} – 0.4	V_{CCO}	V_{CCO} + 0.4	V
Output logical level 0 (cal)		–0.4	0	0.4	V
Output logical level 1 (cal)		V_{CCO} – 0.4	V_{CCO}	V_{CCO} + 0.4	V
Maximum output load (cal)				15	pF

Notes: 1.   See Figure 7-1 on page 13 for more information.
         2.   The gain setting is 0 dB, one clock input, no standby mode [full power mode], 1:1 DMUX, calibration off.

Table 7-2. Electrical Operating Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
DC Accuracy					
No missing code		Guaranteed over specified temperature range			
Differential non-linearity (peak +/-)	DNL		0.25	0.78	LSB
Integral non-linearity (peak +/-)	INL		0.5	1	LSB
Gain error (single channel I or Q) with calibration		−2	0	2	%
Input offset matching (single channel I or Q) with calibration		−2	0	2	LSB
Gain error drift against temperature Gain error drift against V_{CCA}			0.062 0.064		LSB/°C LSB/mV
Mean output offset code with calibration		126	127.5	129	LSB
Transient Performance					
Bit Error Rate Fs = 1 GHz Fin = 250 MHz	BER[1]		10^{-13}		Error/sample
ADC settling time channel I or Q (between 10% – 90% of output response) $V_{Ini} – V_{iniB}$ = 500 mVpp	TS		170		ps

Notes: 1. BER with sinewave at −1 dBFS at Fin = 250 MHz.

2. Gain setting is 0 dB, two clock inputs, no standby mode [full power mode], 1:2 DMUX, calibration on.

Table 7-3. AC Performances

Parameter	Symbol	Min	Typ	Max	Unit
AC Performance					
Signal-to-noise Ratio					
Fs = 1 Gsps Fin = 20 MHz	SNR	42	45		dBc
Fs = 1 Gsps Fin = 500 MHz		40	45		dBc
Fs = 1 Gsps Fin = 1 GHz			43		dBc
Effective Number of Bits					
Fs = 1 Gsps Fin = 20 MHz	ENOB	7	7.3		Bits
Fs = 1 Gsps Fin = 500 MHz		6.5	7.2		Bits
Fs = 1 Gsps Fin = 1 GHz			7		Bits
Total Harmonic Distortion (First 9 Harmonics)					
Fs = 1 Gsps Fin = 20 MHz	|THD|	48	55		dBc
Fs = 1 Gsps Fin = 500 MHz		45	51		dBc
Fs = 1 Gsps Fin = 1 GHz			45		dBc
Spurious Free Dynamic Range					
Fs = 1 Gsps Fin = 20 MHz	|SFDR|	50	56		dBc
Fs = 1 Gsps Fin = 500 MHz		48	54		dBc
Fs = 1 Gsps Fin = 1 GHz			50		dBc
Two-tone Inter-modulation Distortion (Single Channel)					
F_{IN1} = 499 MHz, F_{IN2} = 501 MHz at Fs = 1 Gsps	IMD		–54		dBc
Band flatness from DC up to 600 MHz			±0.5		dB
Phase matching using auto-calibration and FiSDA in interleaved mode (channel I and Q) Fin = 250 MHz Fs = 1 Gsps	dφ	–0.7	0	0.7	°
Crosstalk channel I versus channel Q Fin = 250 MHz, Fs = 1 Gsps[2]	Cr		–65		dB

Notes: 1. Differential input [–1 dBFS analog input level], gain setting is 0 dB, two input clock signals, no standby mode,
1:1 DMUX, ISA = 0 ps.

2. Measured on the AT84AD001TD-EB Evaluation Board.

Table 7-4. AC Performances over Full Industrial Temperature Range (–40°C < T_{amb} < 85°C)

Parameter	Symbol	Min	Typ	Max	Unit
AC Performance					
Signal-to-noise Ratio					
Fs = 1 Gsps Fin = 500 MHz		39	45		dBc
Effective Number of Bits					
Fs = 1 Gsps Fin = 500 MHz		6.0	7.2		Bits
Total Harmonic Distortion (First 9 Harmonics)					
Fs = 1 Gsps Fin = 500 MHz		39	51		dBc
Spurious Free Dynamic Range					
Fs = 1 Gsps Fin = 500 MHz		42	54		dBc

Table 7-5. AC Performances in Interleaved Mode

Parameter	Symbol	Min	Typ	Max	Unit
Interleaved Mode					
Maximum equivalent clock frequency Fint = 2 × Fs Where Fs = external clock frequency	F_{int}	2			Gsps
Minimum clock frequency	F_{int}		20		Msps
Differential non-linearity in Interleaved mode	intDNL		0.25		LSB
Integral non-linearity in Interleaved mode	intINL		0.5		LSB
Signal-to-noise Ratio in Interleaved Mode					
Fint = 2 Gsps Fin= 20 MHz	iSNR		42		dBc
Fint = 2 Gsps Fin = 250 MHz			40		dBc
Effective Number of Bits in Interleaved Mode					
Fint = 2 Gsps Fin = 20 MHz	iENOB		7.1		Bits
Fint = 2 Gsps Fin = 250 MHz			6.8		Bits
Total Harmonic Distortion in Interleaved Mode					
Fint = 2 Gsps Fin = 20 MHz	IiTHDI		52		dBc
Fint = 2 Gsps Fin = 250 MHz			49		dBc
Spurious Free Dynamic Range in Interleaved Mode					
Fint = 2 Gsps Fin = 20 MHz	IiSFDRI		54		dBc
Fint = 2 Gsps Fin = 250 MHz			52		dBc
Two-tone Inter-modulation Distortion (Single Channel) in Interleaved Mode					
F_{IN1} = 249 MHz , F_{IN2} = 251 MHz at F_{int} = 2 Gsps	iIMD		–54		dBc

Note: One analog input on both cores, clock I samples the analog input on the rising and falling edges. The calibration phase is necessary. The gain setting is 0 dB, one input clock I, no standby mode, 1:1 DMUX, FiSDA adjustment.

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Table 7-6. Switching Performances

Parameter	Symbol	Min	Typ	Max	Unit
Switching Performance and Characteristics – See "Timing Diagrams" on page 13.					
Maximum operating clock frequency	F_S	1			Gsps
Maximum operating clock frequency in BIT and decimation modes	F_S (BIT, DEC)			1	Gsps
Minimum clock frequency (no transparent mode)	F_S		10		Msps
Minimum clock frequency (with transparent mode)			1		Ksps
Minimum clock pulse width [high] (No transparent mode)	TC1	0.4	0.5	50	ns
Minimum clock pulse width [low] (No transparent mode)	TC2	0.4	0.5	50	ns
Aperture delay: nominal mode with ISA & FiSDA	TA		0.8		ns
Aperture uncertainty	Jitter		0.4		ps (rms)
Data output delay between input clock and data	TDO		2.8		ns
Data Ready Output Delay	TDR		3		ns
Data Ready Reset to Data Ready	TRDR			2 clock cycles	
Data Ready (CLKO) Delay Adjust (85 ps steps)	Tdrda range		–340 to 255		ps
Output skew		50		100	ps
Output rise/fall time for DATA (20% – 80%)	TR/TF	300	350	500	ps
Output rise/fall time for DATA READY (20% – 80%)	TR/TF	300	350	500	ps
Data pipeline delay (nominal mode) DMUX 1:1	TPD	Port A: 5			Clock cycles
Data pipeline delay (nominal mode) DMUX 1:2		Port A: 5.5 Port B: 4.5			
Data pipeline delay in S/H transparent mode DMUX 1:1		Port A: 4.5			
Data pipeline delay in S/H transparent mode DMUX 1:2		Port A: 5.0 Port B: 4.0			
DDRB recommended pulse width		2 clock cycles			

Notes: 1. All timing characteristics are specified at ambient temperature but also apply to the specified temperature range (the variation over the specified temperature range is negligible).
2. Data Ready signal is centered on Data by TOD-TDR ns.

Figure 7-1. Differential Inputs Voltage Span (Full-scale)
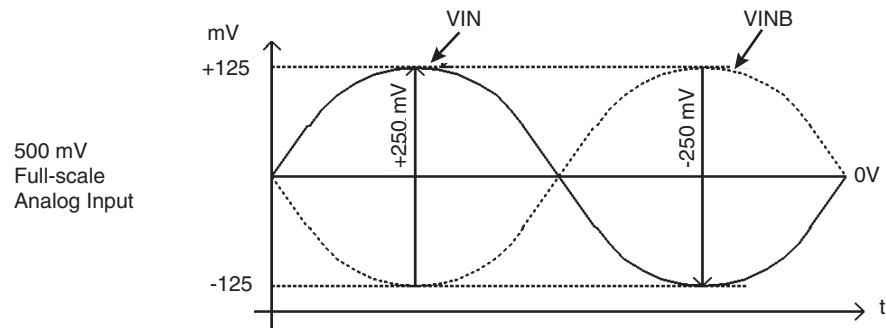
The analog input full-scale range is 0.5V peak-to-peak (Vpp), or –2 dBm into the 50Ω (100Ω differential) termination resistor. In differential mode input configuration, this means 0.25V on each input, or ±125 mV around common mode voltage.

7.1 Timing Diagrams

**Figure 7-2.** 1:1 DMUX Mode, Clock I → ADC I, Clock Q → ADC Q
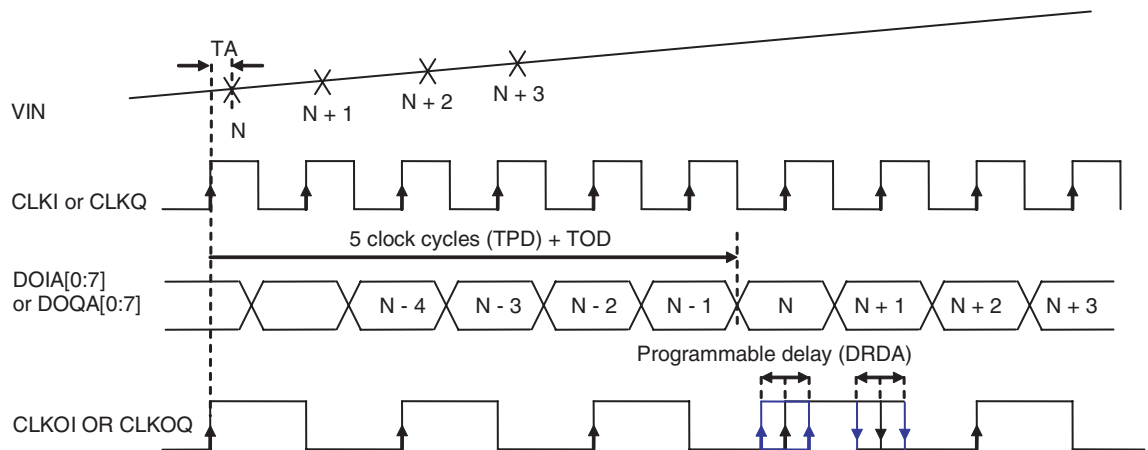
Notes: 1. VIN = VINI or VINQ depending on setting of bits D4 and D5 of 3WSI control register at address 000

2. Programmable delay is controlled via the 3WSI at address 111 (DRDA), refer to section 10 of the 0817G datasheet.

3. DOIB[0:7] and DOQB[0:7] are high impedance.

4. 3WSI Setting at address '000':

| D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	0	1	1	X	X	0	1	0	0

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Figure 7-3. 1:1 DMUX Mode, Clock I → ADC I, Clock I → ADC Q, analog I → ADC I, Analog Q → ADC Q
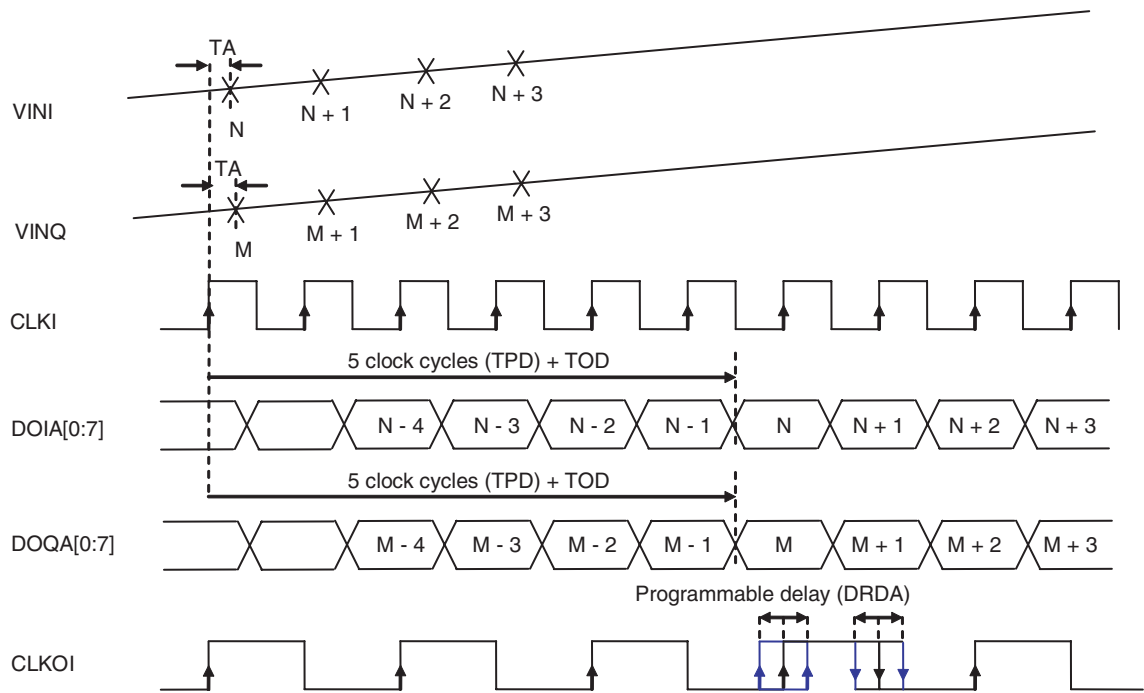
Notes: 1. CLKOQ is high impedance.

2. DOIB[0:7] and DOQB[0:7] are high impedance.

3. Programmable delay is controlled via the 3WSI at address 111 (DRDA), refer to section 10 of the 0817G datasheet.

4. 3WSI Setting at address '000':

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	0	1	0	1	1	0	1	0	0

5. In the case of the following settings:

– Analog I → ADC I, analog I → ADC Q, 3WSI setting at address '000' is

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	0	1	0	1	0	0	1	0	0

Then, DOQA[0:7] will output the same data as DOIA[0:7], ie data N, N+1, N+2… synchronously.

– Analog Q → ADC I, analog Q → ADC Q, 3WSI setting at address '000' is

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	0	1	0	0	X	0	1	0	0

Then, DOQA[0:7] will output the same data as DOIA[0:7], ie data M, M+1, M+2… synchronously.

Figure 7-4. 1:1 DMUX Mode, Clock I → ADC I, Clock IN → ADC Q, Analog I → ADC I, Analog Q → ADC Q
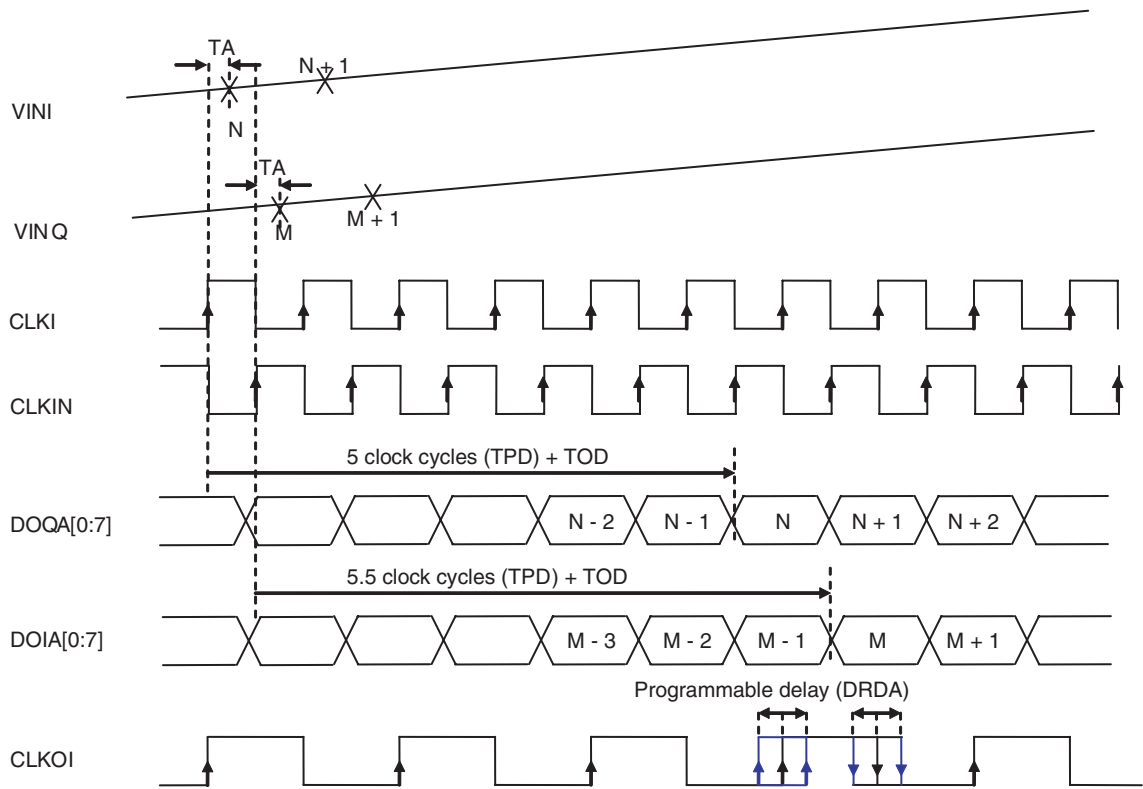
Notes: 1. CLKOQ is high impedance.

2. DOIB[0:7] and DOQB[0:7] are high impedance.

3. Programmable delay is controlled via the 3WSI at address 111 (DRDA), refer to section 10 of the 0817G datasheet.

4. 3WSI Setting at address '000':

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	0	1	0	1	1	0	1	0	0

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Figure 7-5. 1:1 DMUX Mode, Clock I → ADC I, Clock IN → ADC Q
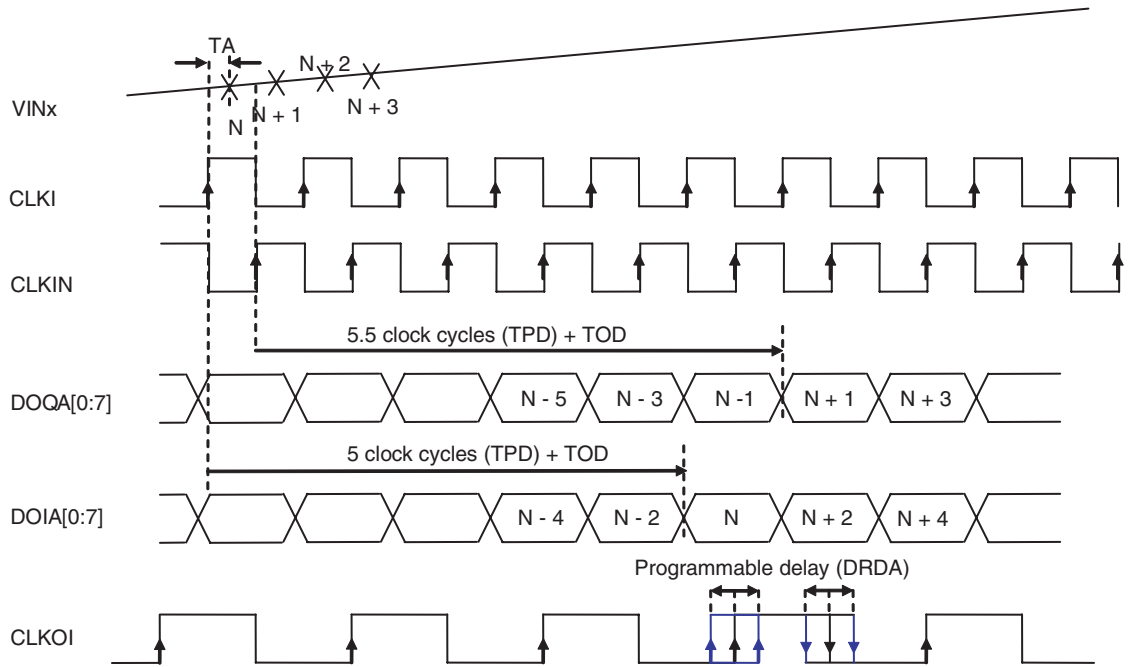

Notes: 1. CLKOQ is high impedance.

2. DOIB[0:7] and DOQB[0:7] are high impedance.

3. Programmable delay is controlled via the 3WSI at address 111 (DRDA), refer to section 10 of the 0817G datasheet.

4. VINx = VINI or VINQ with the following 3WSI settings:

– VINx = VINI, then, Analog I → ADC I, analog I → ADC Q, 3WSI setting at address '000' is

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	0	1	0	1	0	0	1	0	0

– VINx = VINQ, then, Analog Q → ADC I, analog Q → ADC Q, 3WSI setting at address '000' is

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	0	1	0	0	X	0	1	0	0

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Figure 7-6. 1:2 DMUX Mode, Clock I → ADC I, Clock Q → ADC Q
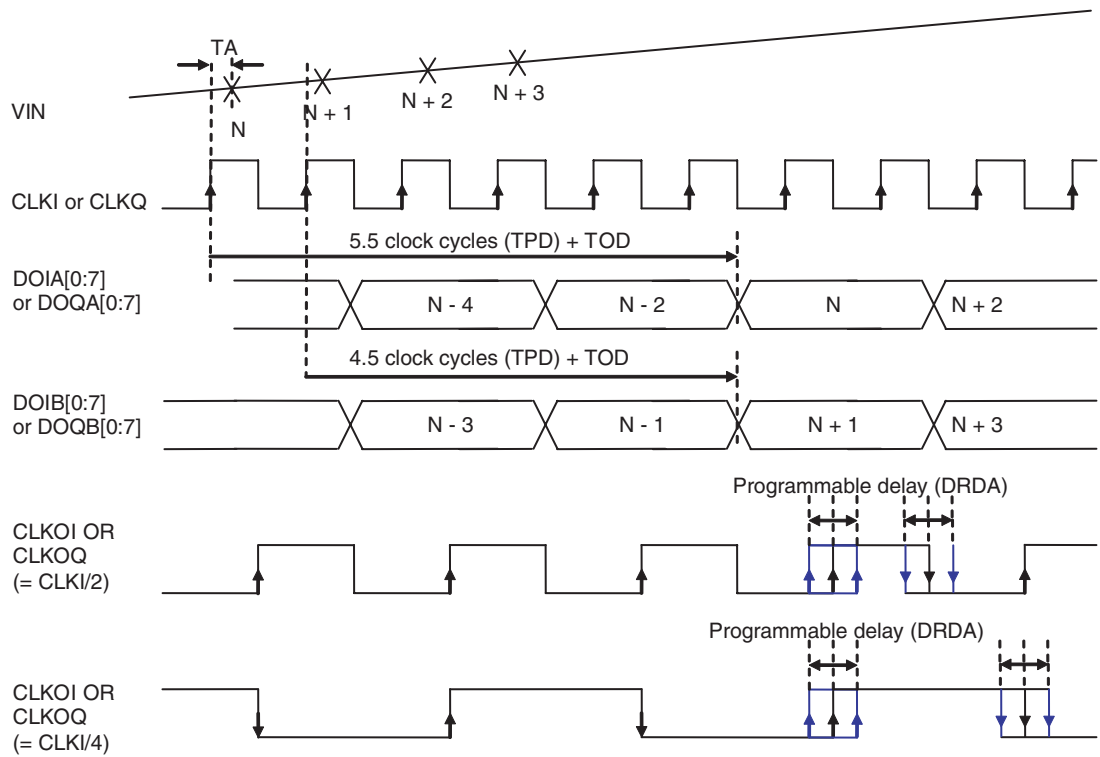
Notes: 1. Programmable delay is controlled via the 3WSI at address 111 (DRDA), refer to Section 10. "Test and Control Features" on page 32.

2. 3WSI Setting at address '000':

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	0	1	1	X	X	1	1	0	0

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Figure 7-7. 1:2 DMUX Mode, Clock I → ADC 1, Clock I → ADC Q
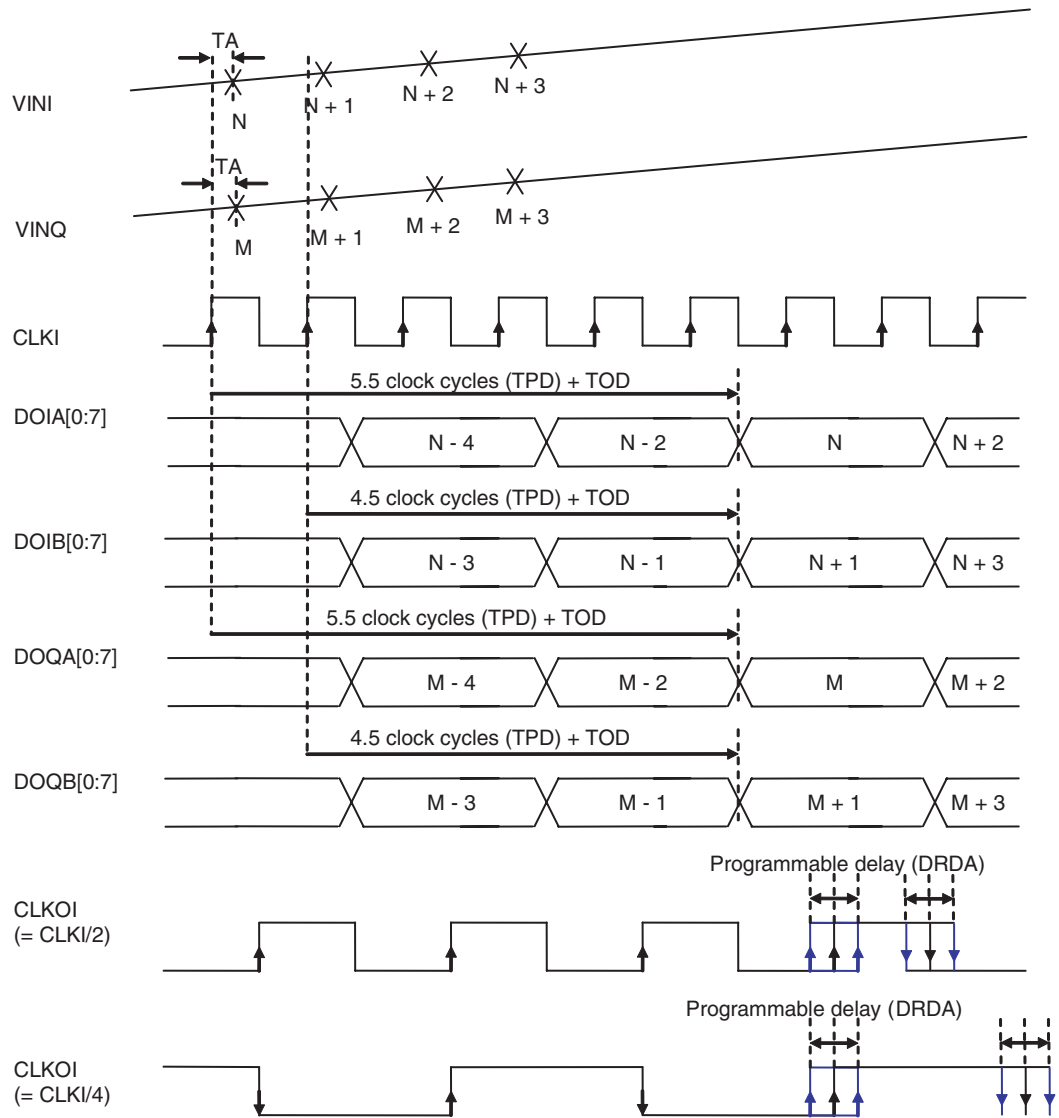
Notes: 1. Programmable delay is controlled via the 3WSI at address 111 (DRDA), refer to section 10 of the 0817G datasheet.
   2. CLKOQ is high impedance.
   3. 3WSI Setting at address '000':

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	0	1	0	1	1	1	1	0	0

4. In the case of the following settings:

– Analog I → ADC I, analog I → ADC Q, 3WSI setting at address '000' is:

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	0	1	0	1	0	0	1	0	0

Then, DOQx[0:7] will output the same data as DOIx[0:7], with x = A or B

– Analog Q → ADC I, analog Q → ADC Q, 3WSI setting at address '000' is

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	0	1	0	0	X	0	1	0	0

Then, DOQx[0:7] will output the same data as DOIx[0:7], with x = A or B

Figure 7-8. 1:2 DMUX Mode, Clock I → ADC I, Clock IN → ADC Q, Analog I → ADC I, Analog Q → ADC Q
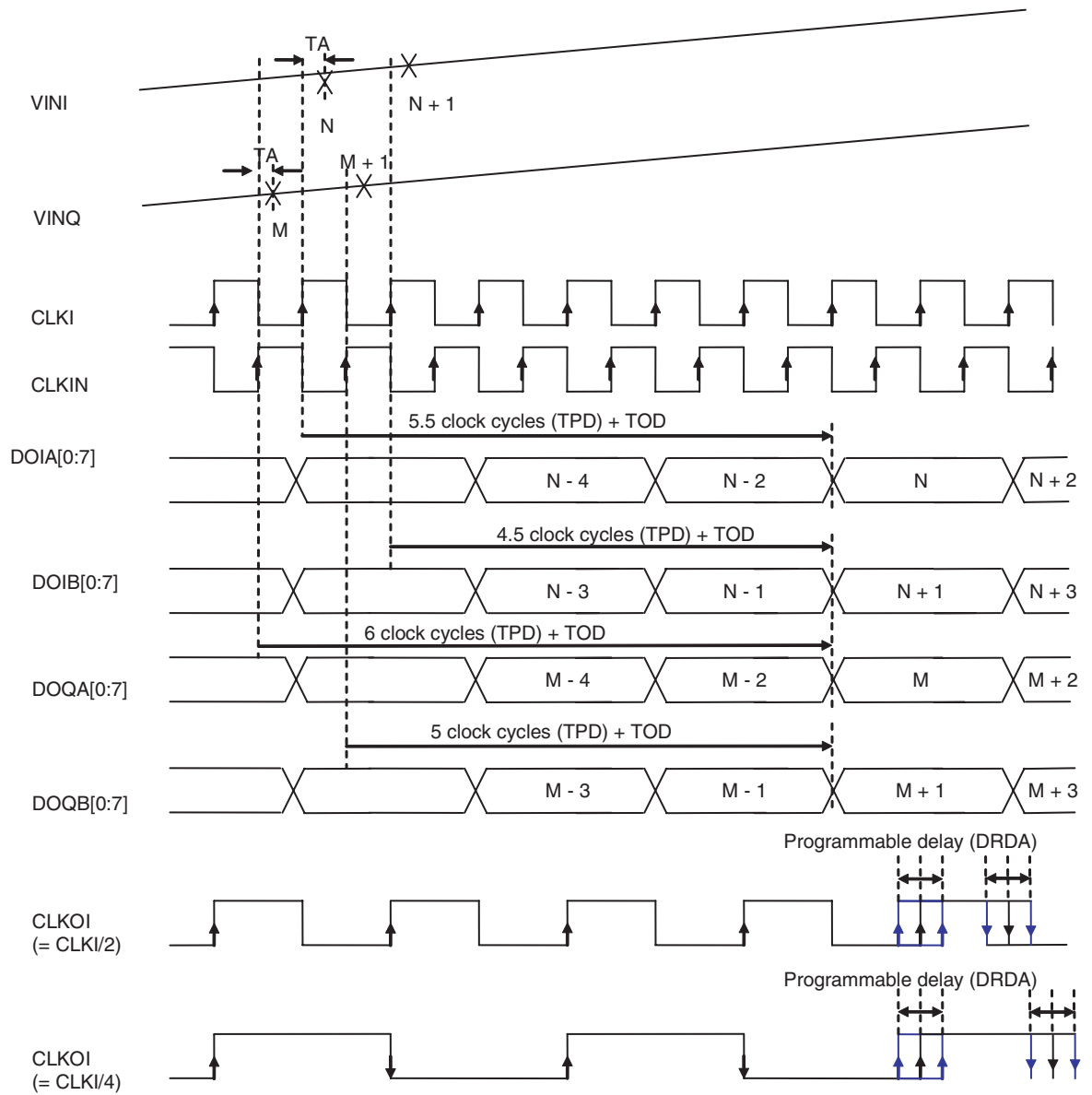
Notes: 1. Programmable delay is controlled via the 3WSI at address 111 (DRDA), refer to section 10 of the 0817G datasheet.
2. CLKOQ is high impedance.
3. 3WSI Setting at address '000':

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	0	1	0	1	1	1	1	0	0

Figure 7-9. 1:2 DMUX Mode, Clock I → ADC I, Clock IN → ADC Q
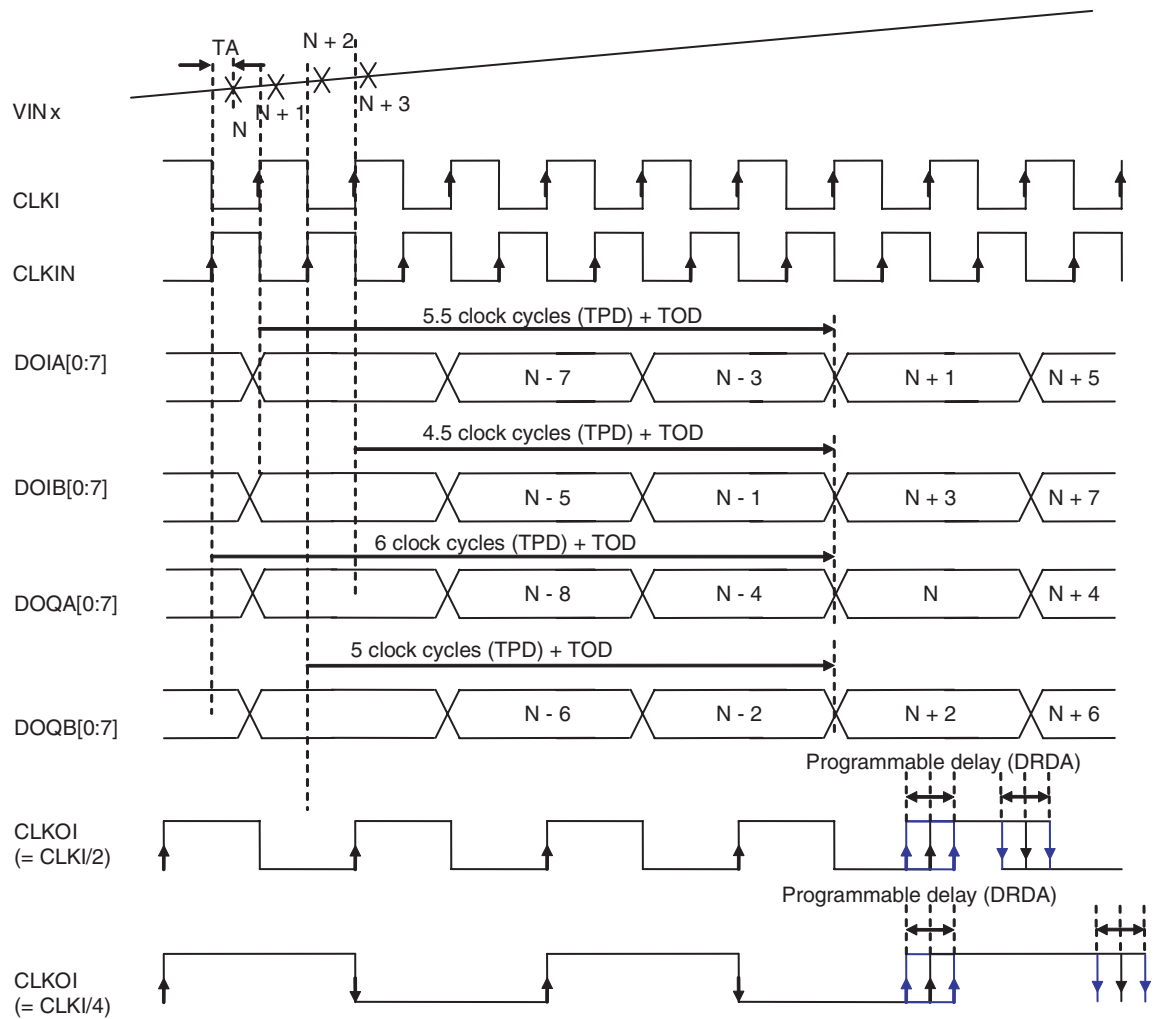
Notes: 1. Programmable delay is controlled via the 3WSI at address 111 (DRDA), refer to section 10 of the 0817G datasheet.

2. CLKOQ is high impedance.

3. VINx = VINI or VINQ with the following 3WSI settings:

– VINx = VINI, then, Analog I → ADC I, analog I → ADC Q, 3WSI setting at address '000' is

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	0	1	0	1	0	0	1	0	0

– VINx = VINQ, then, Analog Q → ADC I, analog Q → ADC Q, 3WSI setting at address '000' is

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	0	1	0	0	X	0	1	0	0

Figure 7-10. 1:1 DMUX Mode, Decimation Mode Test (1:16 Factor)

DOIB[0:7] and DOQB[0:7] are high impedance
CLKOQ is high impedance
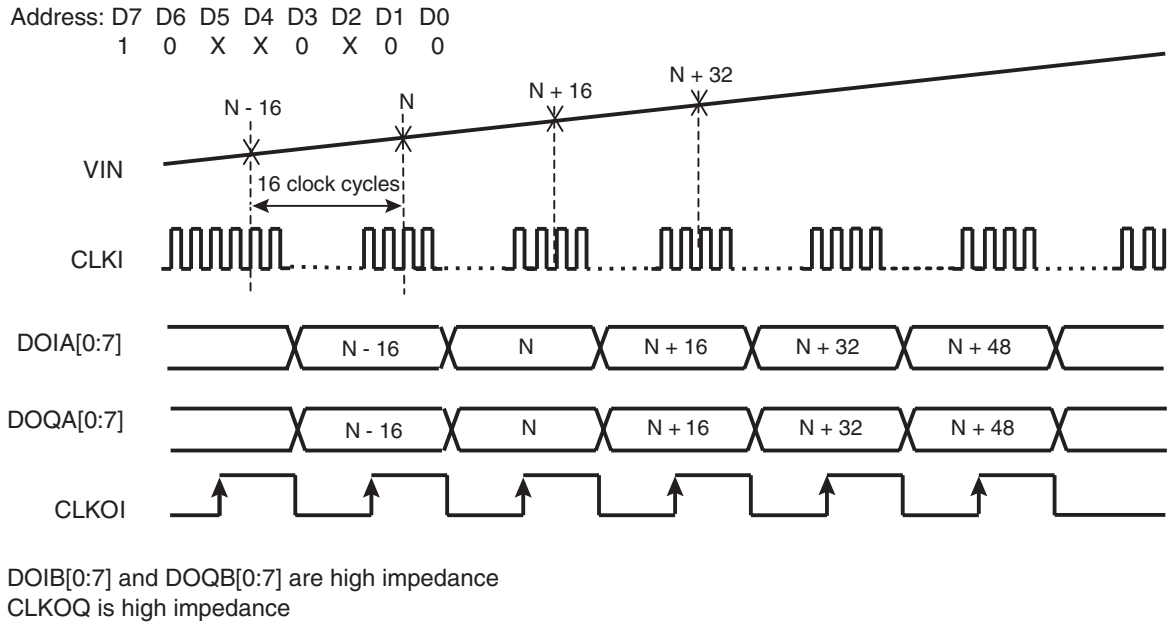
Notes: 1. The maximum clock input frequency in decimation mode is 750 Msps.

2. Frequency(CLKOI) = Frequency(Data) = Frequency(CLKI)/16.

Figure 7-11. Data Ready Reset
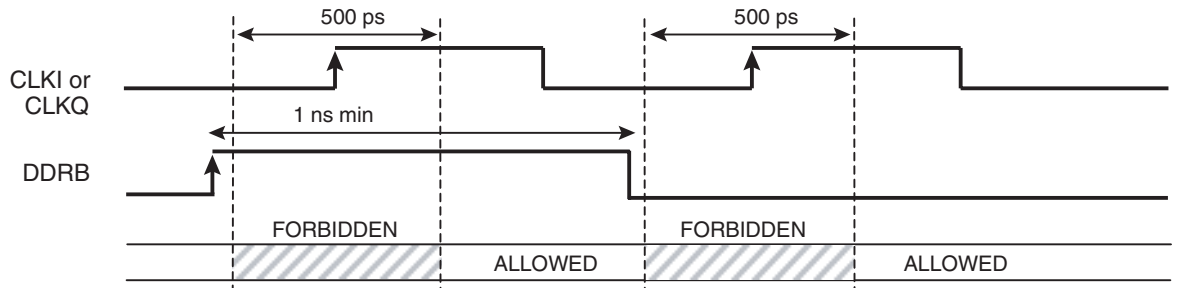
Figure 7-12. Data Ready Reset 1:1 DMUX Mode
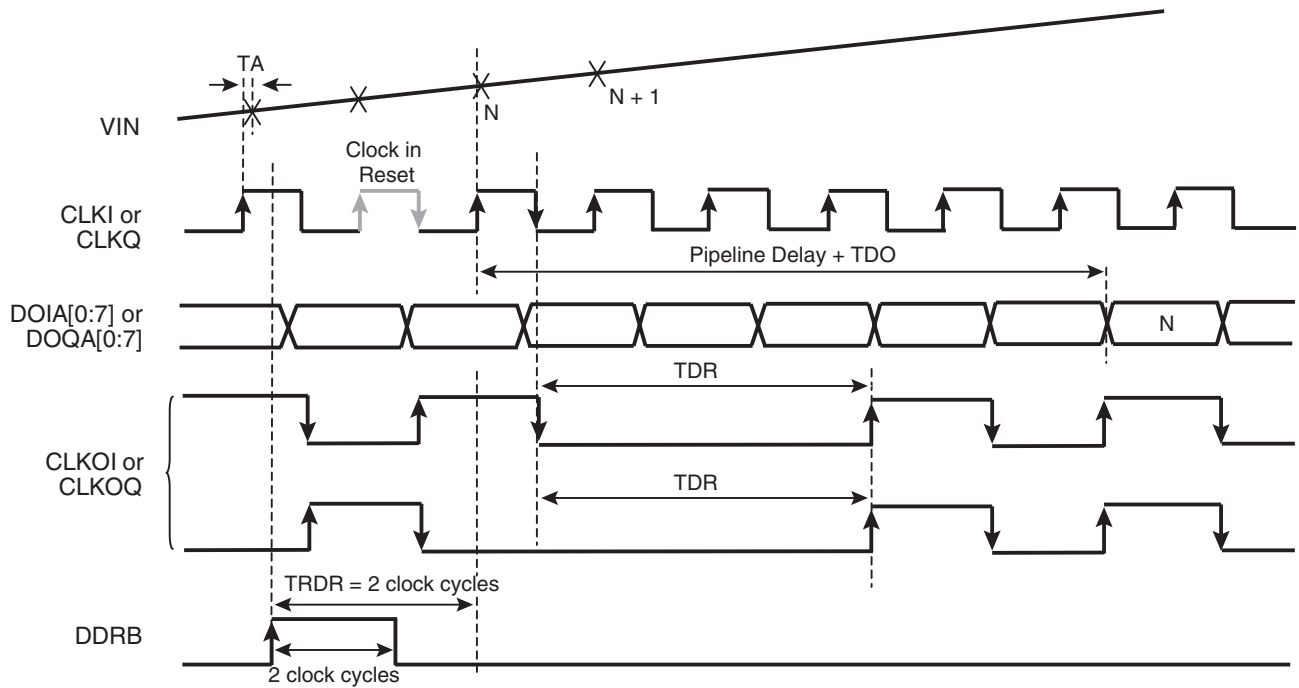
Notes: 1. The Data Ready Reset is taken into account only 2 ns after it is asserted. The output clock first completes its cycle (if the reset occurs when it is high, it goes low only when its half cycle is complete; if the reset occurs when it is low, it remains low) and then only, remains in reset state (frozen to a low level in 1:1 DMUX mode). The next falling edge of the input clock after reset makes the output clock return to normal mode (after TDR).

2. DDRB reset is needed whenever the following functions are changed: DMUX mode, FS/2 - FS/4 function, clock frequency. BIT function (Test mode) in DMUX 1:2.

Figure 7-13. Data Ready Reset 1:2 DMUX Mode
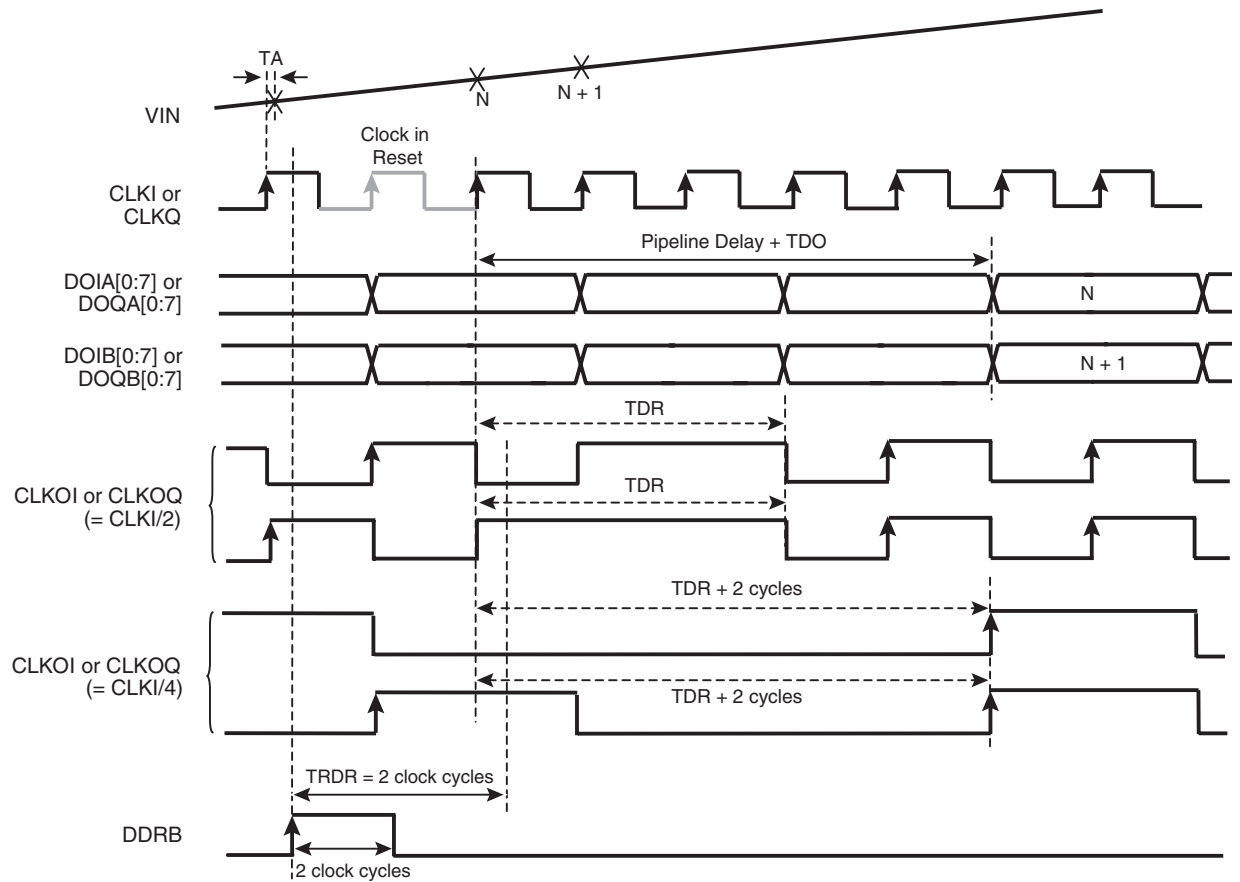
Notes: 1. In 1:2 DMUX, Fs/2 mode:
The Data Ready Reset is taken into account only 2 ns after it is asserted. The output clock first completes its cycle (if the reset occurs when it is low, it goes high only when its half cycle is complete; if the reset occurs when it is high, it remains high) and then only, remains in reset state (frozen to a high level in 1:2 DMUX Fs/2 mode). The next rising edge of the input clock after reset makes the output clock return to normal mode (after TDR).

2. In 1:2 DMUX, Fs/4 mode:
The Data Ready Reset is taken into account only 2 ns after it is asserted. The output clock first completes its cycle (if the reset occurs when it is high, it goes low only when its half cycle is complete; if the reset occurs when it is low, it remains low) and then only, remains in reset state (frozen to a low level in 1:2 DMUX Fs/4 mode). The next rising edge of the input clock after reset makes the output clock return to normal mode (after TDR).

If you don't respect the RESET forbidden zone, The output Data and Data Ready have an uncertainty.If you interleave several ADC, you are not sure that all ADC outputs are synchronized.

Figure 7-14. Data Ready Reset with bad Timings
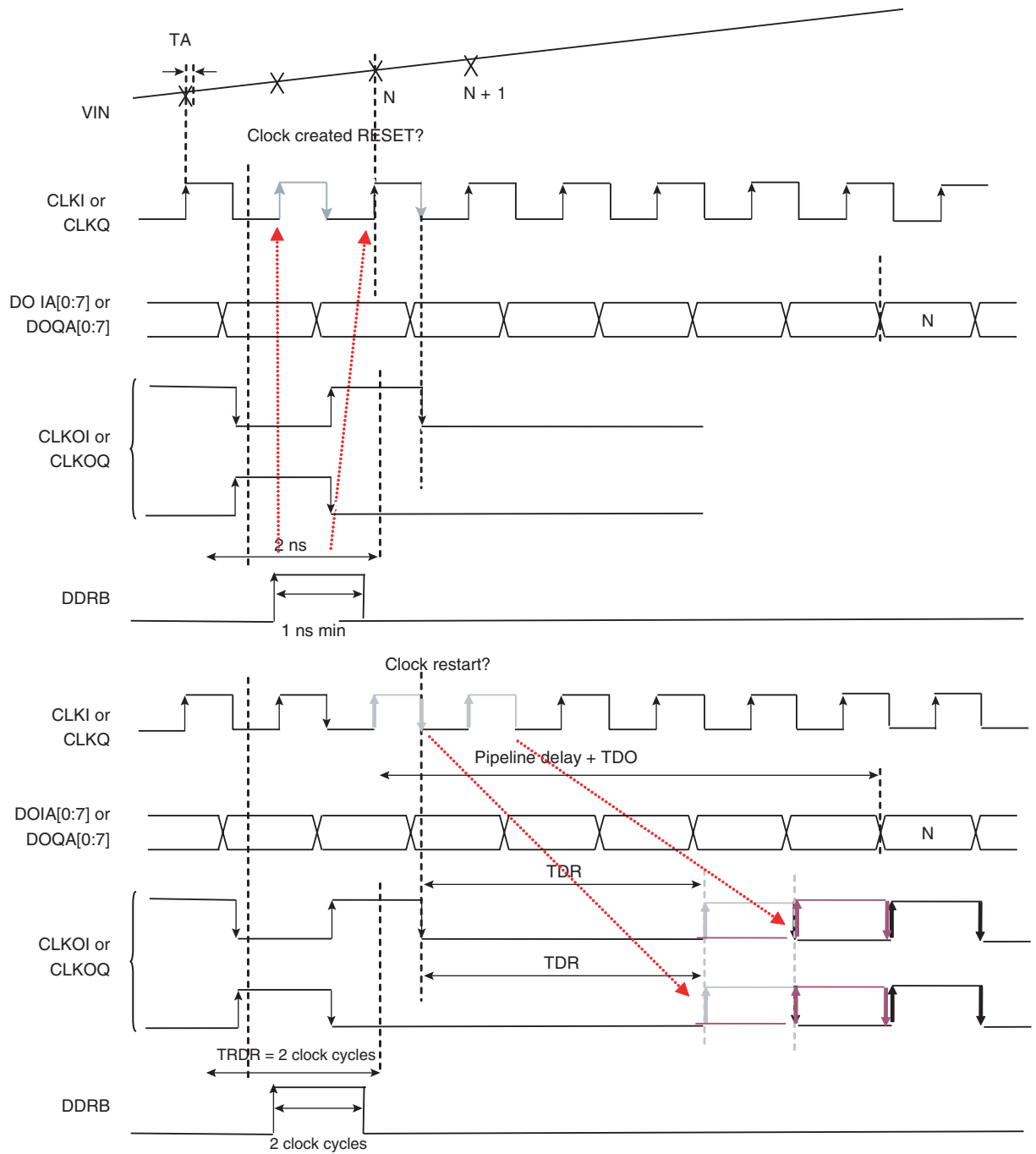
Note: You don't know exactly the clock in RESET edge and the clock in RESTART edge. For the clock CLKOI and
         CLKOQ, you are not sure that this two output clocks start at the same time. Maybe CLKOI starts with the
         first clock in edge and CLKOQ starts with the second clock in edge. The CLKOI and CLKOQ are in opposite
         phase (in same condition before the reset).

7.2 Functions Description

Table 7-7. Description of Functions

Name	Function
V_{CCA}	Positive analog power supply
V_{CCD}	Positive digital power supply
V_{CCO}	Positive output power supply
GNDA	Analog ground
GNDD	Digital ground
GNDO	Output ground
V_{INI}, V_{INIB}	Differential analog inputs I
V_{INQ}, V_{INQB}	Differential analog inputs Q
CLKOI, CLKOIN, CLKOQ, CLKOQN	Differential output data ready I and Q
CLKI, CLKIN, CLKQ, CLKQN	Differential clock inputs I and Q
DDRB, DDRBN	Synchronous data ready reset I and Q
Mode	Bit selection for 3-wire bus or nominal setting
Clk	Input clock for 3-wire bus interface
Data	Input data for 3-wire bus
Ldn	Beginning and end of register line for 3-wire bus interface
<D0AI0:DOAI7> <D0AI0N:DOAI7N> <D0BI0:DOBI7> <D0BI0N:DOBI7N>	Differential output data port channel I
<D0AQ0:DOAQ7> <D0AQ0N:DOAQ7N> <D0BQ0:DOBQ7> <D0BQ0N:DOBQ7N>	Differential output data port channel Q

DOIRI, DOIRIN DOIRQ, DOIRQN	Differential output IN range data I and Q
VtestQ	Test voltage output for ADC Q (to be left open)
VtestI	Test voltage output for ADC I (to be left open)
Cal	Output bit status internal calibration or Test Chip version indicator
Vdiode	Test diode voltage for T_J measurement

7.3 Digital Output Coding (Nominal Settings)

Table 7-8. Digital Output Coding (Nominal Setting, MSB = bit 7 and LSB = bit 0)

Differential Analog Input	Voltage Level	Digital Output I or Q (Binary Coding)	Out-of-range Bit
> 250 mV	> Positive full-scale + 1/2 LSB	1 1 1 1 1 1 1 1	1
250 mV 248 mV	Positive full-scale + 1/2 LSB Positive full-scale − 1/2 LSB	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 0	0 0
1 mV −1 mV	Bipolar zero + 1/2 LSB Bipolar zero − 1/2 LSB	1 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1	0 0
−248 mV −250 mV	Negative full-scale + 1/2 LSB Negative full-scale − 1/2 LSB	0 0 0 0 0 0 0 1 0 0 0 0 0 0 0 0	0 0
< −250 mV	< Negative full-scale − 1/2 LSB	0 0 0 0 0 0 0 0	1

8. Pin Description

Table 8-1.   AT84AD001C Pin Description

Symbol	Pin number	Function
GNDA, GNDD, GNDO	10, 12, 22, 24, 36, 38, 40, 42, 44, 46, 51, 54, 59, 61, 63, 65, 67, 69, 85, 87, 97, 99, 109, 111, 130, 142, 144	Ground pins. To be connected to external ground plane
V_{CCA}	41, 43, 45, 60, 62, 64	Analog positive supply: 3.3V typical
V_{CCD}	9, 21, 37, 39, 66, 68, 88, 100, 112, 123, 141	3.3V digital supply
V_{CCO}	11, 23, 86, 98, 110, 143	2.25V output and 3-wire serial interface supply
V_{INI}	57, 58	In-phase (+) analog input signal of the sample & hold differential preamplifier channel I
V_{INIB}	55, 56	Inverted phase (–) of analog input signal (V_{INI})
V_{INQ}	47, 48	In-phase (+) analog input signal of the sample & hold differential preamplifier channel Q
V_{INQB}	49, 50	Inverted phase (–) of analog input signal (V_{INQ})
CLKI	124	In-phase (+) clock input signal
CLKIN	125	Inverted phase (–) clock input signal (CLKI)
CLKQ	129	In-phase (+) clock input signal
CLKQN	128	Inverted phase (–) clock input signal (CLKQ)
DDRB	126	Synchronous data ready reset I and Q
DDRBN	127	Inverted phase (–) of input signal (DDRB)
DOAI0, DOAI1, DOAI2, DOAI3, DOAI4, DOAI5, DOAI6, DOAI7	117, 113, 105, 101, 93, 89, 81, 77	In-phase (+) digital outputs first phase demultiplexer (channel I) DOAI0 is the LSB. D0AI7 is the MSB
DOAI0N, DOAI1N, DOAI2N, DOAI3N, DOAI4N, DOAI5N, DOAI6N, DOAI7N,	118, 114, 106, 102, 94, 90, 82, 78	Inverted phase (–) digital outputs first phase demultiplexer (channel I) DOAI0N is the LSB. D0AI7N is the MSB
DOBI0, DOBI1, DOBI2, DOBI3, DOBI4, DOBI5, DOBI6, DOBI7	119, 115, 107, 103, 95, 91, 83, 79	In-phase (+) digital outputs second phase demultiplexer (channel I) DOBI0 is the LSB. D0BI7 is the MSB
DOBI0N, DOBI1N, DOBI2N, DOBI3N, DOBI4N, DOBI5N, DOBI6N, DOBI7N	120, 116, 108, 104, 96, 92, 84, 80	Inverted phase (–) digital outputs second phase demultiplexer (channel I) DOBI0N is the LSB. D0BI7N is the MSB
DOAQ0, DOAQ1, DOAQ2, DOAQ3, DOAQ4, DOAQ5, DOAQ6, DOAQ7	136, 140, 4, 8, 16, 20, 28, 32	In-phase (+) digital outputs first phase demultiplexer (channel Q) DOAI0 is the LSB. D0AQ7 is the MSB
DOAQ0N, DOAQ1N, DOAQ2N, DOAQ3N, DOAQ4N, DOAQ5N, DOAQ6N, DOAQ7N	135, 139, 3, 7, 15, 19, 27, 31	Inverted phase (–) digital outputs first phase demultiplexer (channel Q) DOAI0N is the LSB. D0AQ7N is the MSB
DOBQ0, DOBQ1, DOBQ2, DOBQ3, DOBQ4, DOBQ5, DOBQ6, DOBQ7	134, 138, 2, 6, 14, 18, 26, 30	In-phase (+) digital outputs second phase demultiplexer (channel Q) DOBQ0 is the LSB. D0BQ7 is the MSB
DOBQ0N, DOBQ1N, DOBQ2N, DOBQ3N, DOBQ4N, DOBQ5N, DOBQ6N, DOBQ7N	133, 137, 1 ,5, 13, 17, 25, 29	Inverted phase (–) digital outputs second phase demultiplexer (channel Q) DOBQ0N is the LSB. D0BQ7N is the MSB

Table 8-1. AT84AD001C Pin Description (Continued)

Symbol	Pin number	Function
DOIRI	75	In-phase (+) out-of-range bit input (I phase) combined demultiplexer out-of-range is high on the leading edge of code 0 and code 256
DOIRIN	76	Inverted phase of output signal DOIRI
DOIRQ	34	In-phase (+) out-of-range bit input (Q phase) combined demultiplexer out-of-range is high on the leading edge of code 0 and code 256
DOIRQN	33	Inverted phase of output signal DOIRQ
MODE	74	Bit selection for 3-wire bus interface or nominal setting
CLK	73	Input clock for 3-wire bus interface
DATA	72	Input data for 3-wire bus
LND	71	Beginning and end of register line for 3- wire bus interface
CLKOI	121	Output clock in-phase (+) channel I
CLKOIN	122	Inverted phase (–) output clock channel I
CLKOQ	132	Output clock in-phase (+) channel Q, 1/2 input clock frequency
CLKOQN	131	Inverted phase (–) output clock channel Q
VtestQ, VtestI	52, 53	Pins for internal test (to be left open)
Cal	70	Calibration output bit status or Test Chip version indicator
Vdiode	35	Positive node of diode used for die junction temperature measurements

Figure 8-1. AT84AD001C Pinout (Top View)

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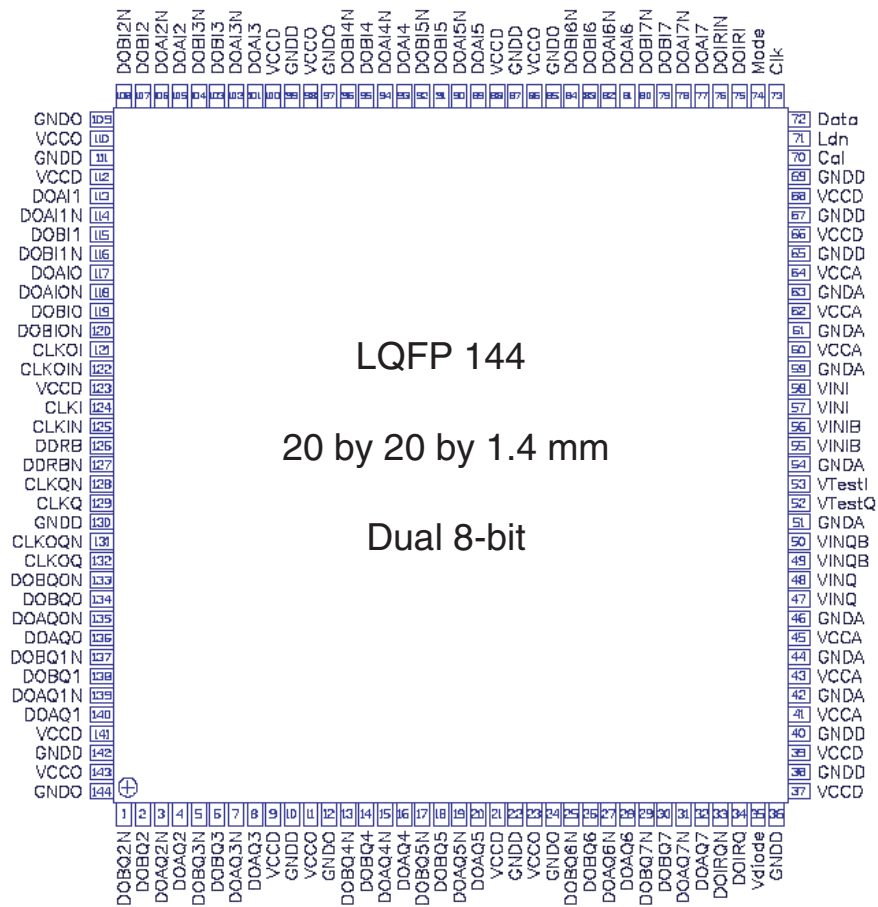
9. Typical Characterization Results

Nominal conditions (unless otherwise specified):

- V_{CCA} = 3.3V; V_{CCD} = 3.3V; V_{CCO} = 2.25V
- V_{INI} – V_{INB} or V_{INQ} to V_{INQB} = 500 mVpp full-scale differential input
- LVDS digital outputs (100Ω)
- TA (typical) = 25°C
- Full temperature range: 0°C < TA < 70°C (commercial grade) or –40°C < TA < 85°C (industrial grade)

9.1 Typical Full Power Input Bandwidth

- Fs = 500 Msps
- Pclock = 0 dBm
- Pin = –1 dBFS
- Gain flatness (±0.5 dB) from DC to > 500 MHz
- Full power input bandwidth at –3 dB > 1.5 GHz

Figure 9-1. Full Power Input Bandwidth
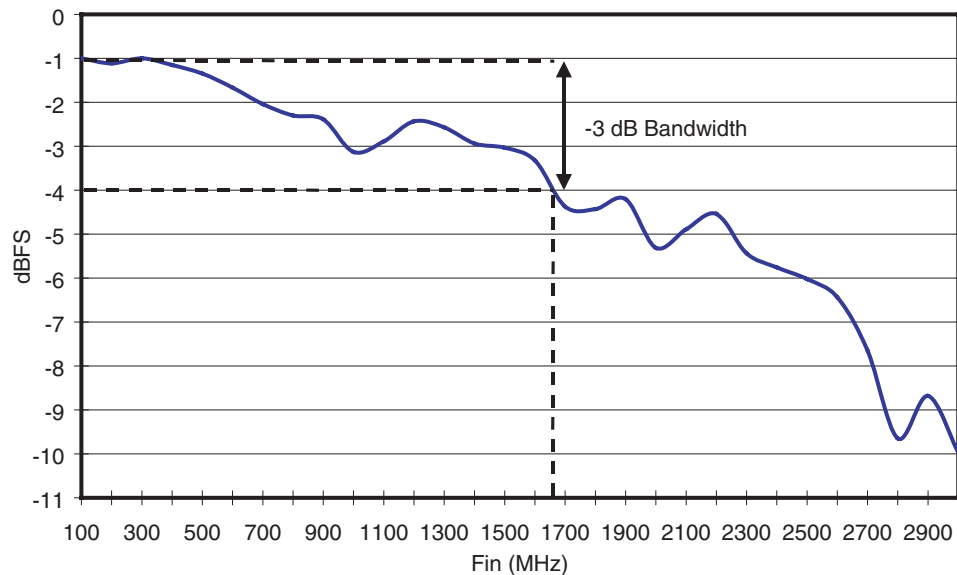
9.2 Typical DC, INL and DNL Patterns

1:2 DMUX mode, Fs/4 DR type

Figure 9-2. Typical INL (Fs = 50 Msps, Fin = 1 MHz, Saturated Input)
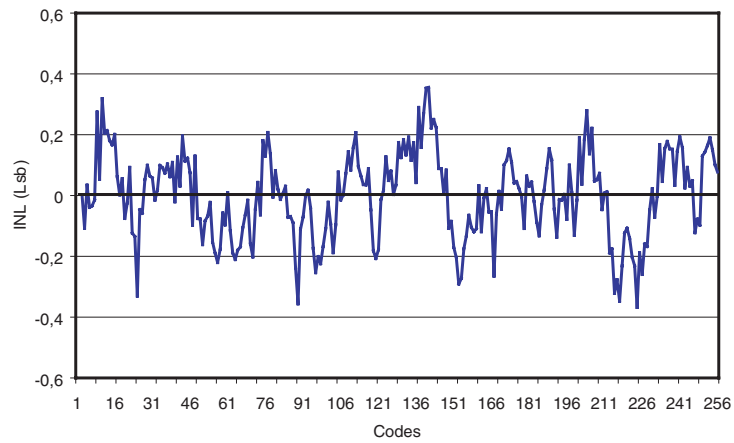
Figure 9-3. Typical DNL (Fs = 50 Msps, Fin = 1 MHz, Saturated Input)
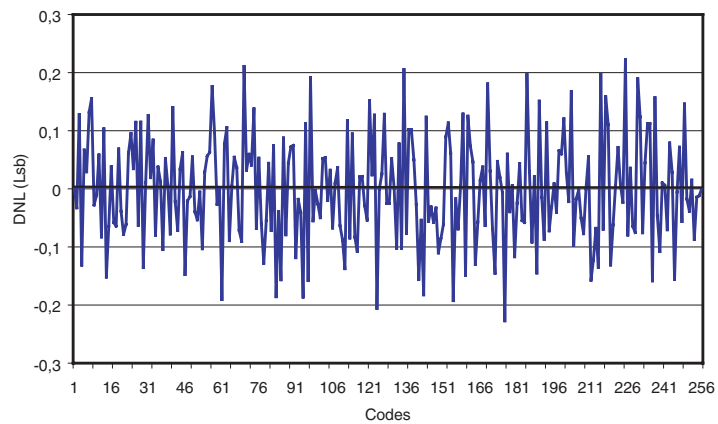
10. Test and Control Features

10.1 3-wire Serial Interface Control Setting

Table 10-1.   3-wire Serial Interface Control Settings

Mode	Characteristics
Mode = 1 (2.25V)	3-wire serial bus interface activated

Mode = 0 (0V)	3-wire serial bus interface deactivated
	Nominal setting:
	    Dual channel I and Q activated
	    One clock I
	    0 dB gain
	    DMUX mode 1:1
	    DRDA I & Q = 0 ps
	    ISA I & Q = 0 ps
	    FiSDA Q = 0 ps
	    Cal = 0
	    Decimation test mode OFF
	    Calibration setting OFF
	    Data Ready = Fs/4

Note: In the AT84AD001C, the default setting is Fs/4 mode for DMUX 1:2 mode (it was Fs/2 in previous versions of the device AT84AD001Bxxx series).

10.1.1 3-wire Serial Interface and Data Description

The 3-wire bus is activated with the control bit mode set to 1. The length of the word is 19 bits: 16 for the data and 3 for the address. The maximum clock frequency is 50 MHz.

Table 10-2.   3-wire Serial Interface Address Setting Description

Address	Setting
000	**Standby** Chip version indicator 1:1 or 1:2 DMUX mode Analog input MUX Clock selection Auto-calibration Decimation test mode Data Ready Delay Adjust
001	**Analog gain adjustment** Data7 to Data0: gain channel I Data15 to Data8: gain channel Q Code 00000000: −1.5 dB Code 10000000: 0 dB Code 11111111: 1.5 dB Steps: 0.011 dB
010	**Offset compensation** Data7 to Data0: offset channel I Data15 to Data8: offset channel Q Data7 and Data15: sign bits Code 11111111b: 31.75 LSB Code 10000000b: 0 LSB Code 00000000b: 0 LSB Code 01111111b: −31.75 LSB Steps: 0.25 LSB Maximum correction: ±31.75 LSB
011	**Gain compensation** Data6 to Data0: channel I/Q (Q is matched to I for interleaving adjustment) Code 11111111b: −0.315 dB Code 10000000b: 0 dB Code 0000000b: 0 dB Code 0111111b: 0.315 dB Steps: 0.005 dB Data6: sign bit Data15 to Data7 = XXX
100	**Internal Settling Adjustment (ISA)** Data2 to Data0: channel I Data5 to Data3: channel Q Data15 to Data6: 1000010000 Code 000 = −200 ps Code 100 = 0 ps Code 111 = 150 ps DMUX 1:1 recommended value code 100 = 0 ps DMUX 1:2 recommended value code 010 = −100 ps

Table 10-2. 3-wire Serial Interface Address Setting Description (Continued)

Address	Setting
101	**Testability** Data3 to Data0 = 0000 Mode S/H transparent OFF: Data4 = 0 ON: Data4 = 1 Data7 = 0 Data8 = 0 Data5 to Data6 = XXX Data15 to Data9 = XXX

110	**Built-In Test (BIT)**
	Data0 = 0 BIT Inactive Data0 = 1 BIT Active
	Data1 = 0 Static BIT Data1 = 1 Dynamic BIT
	If Data1 = 1, then Ports BI & BQ = Rising Ramp
	                        Ports AI & AQ = Decreasing Ramp
	If Data1 = 0, then Data2 to Data9 = Static Data for BIT
	                        Ports BI & BQ = Data2 to Data9
	                        Ports AI & AQ = NOT (Data2 to Data9)
	
	Data15 to Data10 = XXX

111	**Data Ready Delay Adjust (DRDA)** Data2 to Data0: clock I Data5 to Data3: clock Q Steps: 85 ps 000: –340 ps 100: 0 ps 111: +255 ps **Fine Sampling Delay Adjustment (FiSDA) on channel Q** Data10 to Data6: channel Q Steps: 4 ps Data4: sign bit 11000: –60 ps Code 10000: 0 ps Code 00000: 0 ps Code 01111: +60 ps Data15 to Data11 = XXX

Notes: 1. The Internal Settling Adjustment could change independently of the two analog sampling times (TA channels I and Q) of the sample/hold (with a fixed digital sampling time) with steps of ±50 ps:
Nominal mode will be given by Data2…Data0 = 100 or Data5…Data3 = 100.
Data5…Data3 = 000 or Data2…Data0 = 000: sampling time is –200 ps compared to nominal.
Data2…Data0 = 111 or Data5…Data3 = 111: sampling time is 150 ps compared to nominal.
We recommend setting the ISA to 0 ps in 1:1 DMUX mode and to –100 ps in 1:2 DMUX mode to optimize the ADC's dynamic performance.

2. The Fine Sampling Delay Adjustment enables you to change the sampling time (steps of 4 ps) on channel Q more precisely, particularly in the interleaved mode.

3. A Built-In Test (BIT) function is available to rapidly test the device's I/O by either applying a defined static pattern to the dual ADC or by generating a dynamic ramp at the output of the dual ADC. This function is controlled via the 3-wire bus interface at the address 110. The maximum clock frequency in dynamic BIT mode is 1 Gsps.
Please refer to "Built-In Test (BIT)" on page 41 for more information about this function. Dynamic BIT works on channel I when Clock I is applied and on channel Q when clock Q is applied.

4. The decimation mode enables you to lower the output bit rate (including the output clock rate) by a factor of 16, while the internal clock frequency remains unchanged. The maximum clock frequency in decimation mode is 1 Gsps.

5. The "S/H transparent" mode (address 101, Data4) enables bypassing of the ADC's track/hold. This function optimizes the ADC's performances at very low input frequencies (Fin < 50 MHz) with an increase of 2 dB in SNR.

6. If bit D2 "Chip version Test bit" is set to "0", the output bit Cal should change to high level when the ADC corresponds to AT84AD001C version (this function is not implemented in previous AT84AD001 and AT84AD001B versions).

7. With DRDA adjustment, you can shift the Output clock signal (shift the falling and rising edges) from –200 to +150 ps around its default value.

8. DDRB reset is needed whenever the following functions are changed: DMUX mode, FS/2 - FS/4 function, clock frequency. BIT function (Test mode) in DMUX 1:2.

Table 10-3. 3-wire Serial Interface Data Setting Description

Setting for Address: 000	D15	D14	D13	D12	D11	D10	D9[1]	D8	D7	D6	D5	D4	D3	D2	D1	D0
Full standby mode	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1	1
Standby channel I[2]	X	X	X	X	X	X	0	X	X	X	X	X	X	X	0	1
Standby channel Q[3]	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1	0
No standby mode	X	X	X	X	X	X	0	X	X	X	X	X	X	X	0	0
Chip Version Test bit inactivated[7]	X	X	X	X	X	X	0	X	X	X	X	X	X	1	X	X
Chip Version Test bit activated[7]	X	X	X	X	X	X	0	X	X	X	X	X	X	0	X	X
DMUX 1:2 mode	X	X	X	X	X	X	0	X	X	X	X	X	1	X	X	X
DMUX 1:1 mode	X	X	X	X	X	X	0	X	X	X	X	X	0	X	X	X
Analog selection mode Input I →ADC I Input Q → ADC Q	X	X	X	X	X	X	0	X	X	X	1	1	X	X	X	X
Analog selection mode Input I →ADC I Input I → ADC Q	X	X	X	X	X	X	0	X	X	X	1	0	X	X	X	X
Analog selection mode Input Q →ADC I Input Q → ADC Q	X	X	X	X	X	X	0	X	X	X	0	X	X	X	X	X
Clock Selection mode CLKI →ADC I CLKQ → ADC Q	X	X	X	X	X	X	0	X	1	1	X	X	X	X	X	X
Clock selection mode CLKI →ADC I CLKI → ADC Q	X	X	X	X	X	X	0	X	1	0	X	X	X	X	X	X
Clock selection mode CLKI →ADC I CLKIN → ADC Q	X	X	X	X	X	X	0	X	0	X	X	X	X	X	X	X
Decimation OFF mode	X	X	X	X	X	X	0	0	X	X	X	X	X	X	X	X
Decimation ON mode	X	X	X	X	X	X	0	1	X	X	X	X	X	X	X	X
Keep last calibration calculated value[4] No calibration phase	X	X	X	X	0	1	0	X	X	X	X	X	X	X	X	X
No calibration phase[5] No calibration value	X	X	X	X	0	0	0	X	X	X	X	X	X	X	X	X
Start a new calibration phase	X	X	X	X	1	1	0	X	X	X	X	X	X	X	X	X

Table 10-3. 3-wire Serial Interface Data Setting Description (Continued)

Setting for Address: 000	D15	D14	D13	D12	D11	D10	D9[1]	D8	D7	D6	D5	D4	D3	D2	D1	D0
Control wait bit calibration[6]	X	X	a	b	X	X	0	X	X	X	X	X	X	X	X	X
In 1:2 DMUX FDataReady I & Q = Fs/4 [9]	X	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X
In 1:2 DMUX FDataReady I & Q = Fs/2 [9]	X	1	X	X	X	X	0	X	X	X	X	X	X	X	X	X

Notes: 1. D9 must be set to "0"

2. Mode standby channel I: use analog input I Vini, Vinib and Clocki.

3. Mode standby channel Q: use analog input Q Vinq, Vinqb and Clockq.

4. Keep last calibration calculated value – no calibration phase: D11 = 0 and D10 = 1. No new calibration is required. The values taken into account for the gain and offset are either from the last calibration phase or are default values (reset values).

5. No calibration phase – no calibration value: D11 = 0 and D10 = 0. No new calibration phase is required. The gain and offset compensation functions can be accessed externally by writing in the registers at address 010 for the offset compensation and at address 011 for the gain compensation.

6. The control wait bit gives the possibility to change the internal setting for the auto-calibration phase:
For high clock rates (> 500 Msps) use a = b = 1.
For clock rates > 250 Msps and < 500 Msps use a = 1 and b = 0.
For clock rates > 125 Msps and < 250 Msps use a = 0 and b = 1.
For low clock rates < 125 Msps use a = 0 and b = 0.

7. If bit D2 "Chip version Test bit" is set to "0", the output bit Cal should change to high level when the ADC corresponds to AT84AD001C version (this function is not implemented in previous AT84AD001 and AT84AD001B versions).

8. When Channel I is in standby (D1 = 0, D0 = 1), the following modes are forbidden:
Clock I → I & Q (D7 = 1, D6 = 0)
Clock I → I & Clock IN → Q (D7 = 0, D6 = X)

9. Default mode for AT84AD001C is now Fs/4 (previously Fs/2 for AT84AD001Bxxx series).

10.1.2 3-wire Serial Interface Timing Description

The 3-wire serial interface is a synchronous write-only serial interface made of three wires:

- sclk: serial clock input
- sldn: serial load enable input
- sdata: serial data input

The 3-wire serial interface gives write-only access to as many as 8 different internal registers of up to 16 bits each. The input format is always fixed with 3 bits of register address followed by 16 bits of data. The data and address are entered with the Most Significant Bit (MSB) first.

The write procedure is fully synchronous with the rising clock edge of "sclk" and described in the write chronogram ().

- "sldn" and "sdata" are sampled on each rising clock edge of "sclk" (clock cycle).
- "sldn" must be set to 1 when no write procedure is performed.
- A minimum of one rising clock edge (clock cycle) with "sldn" at 1 is required for a correct start of the write procedure.
- A write starts on the first clock cycle with "sldn" at 0. "sldn" must stay at 0 during the complete write procedure.

- During the first 3 clock cycles with "sldn" at 0, 3 bits of the register address from MSB (a[2]) to LSB (a[0]) are entered.
- During the next 16 clock cycles with "sldn" at 0, 16 bits of data from MSB (d[15]) to LSB (d[0]) are entered.
- An additional clock cycle with "sldn" at 0 is required for parallel transfer of the serial data d[15:0] into the addressed register with address a[2:0]. This yields 20 clock cycles with "sldn" at 0 for a normal write procedure.
- A minimum of one clock cycle with "sldn" returned at 1 is requested to close the write procedure and make the interface ready for a new write procedure. Any clock cycle where "sldn" is at 1 *before* the write procedure is completed interrupts this procedure and no further data transfer to the internal registers is performed.
- Additional clock cycles with "sldn" at 0 *after* the parallel data transfer to the register (done at the 20th consecutive clock cycle with "sldn" at 0) do not affect the write procedure and are ignored.

It is possible to have only one clock cycle with "sldn" at 1 between two following write procedures.

- 16 bits of data must always be entered even if the internal addressed register has less than 16 bits. Unused bits (usually MSBs) are ignored. Bit signification and bit positions for the internal registers are detailed in Table 10-2 on page 33.

To reset the registers, the Pin mode can be used as a reset pin for chip initialization, even when the 3-wire serial interface is used.

Figure 10-1. Write Chronogram
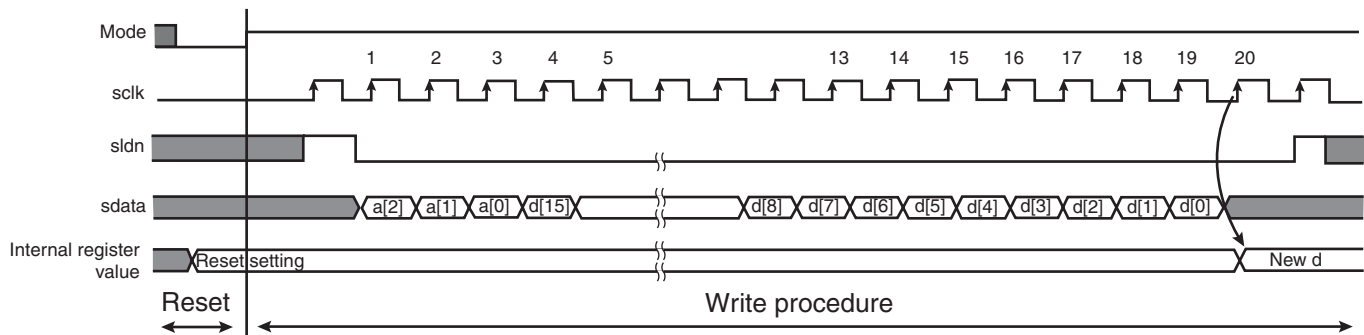
Figure 10-2. Timing Definition
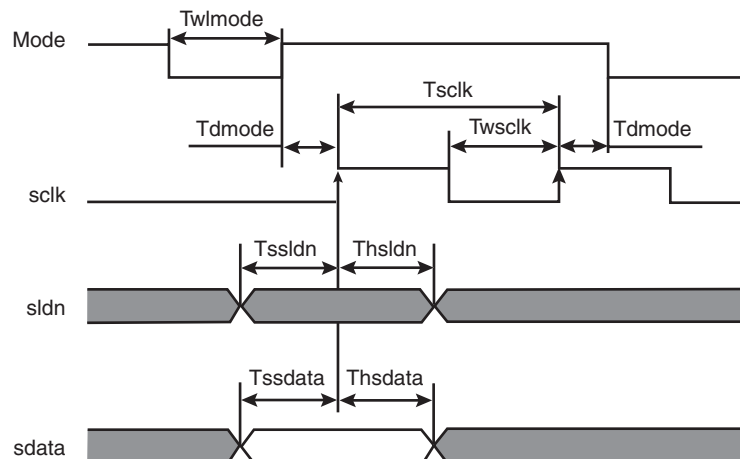
Table 10-4. Timing Description

Name	Parameter	Value			Unit
		Min	Typ	Max	
Tsclk	Sclk period	20			ns
Twsclk	High or low time of sclk	5			ns
Tssldn	Setup time of sldn before rising edge of sclk	4			ns
Thsldn	Hold time of sldn after rising edge of sclk	2			ns
Tssdata	Setup time of sdata before rising edge of sclk	4			ns
Thsdata	Hold time of sdata after rising edge of sclk	2			ns
Twlmode	Minimum low pulse width of mode	5			ns
Tdmode	Minimum delay between an edge of mode and the rising edge of sclk	10			ns

10.1.3 Calibration Description

The AT84AD001C offers the possibility of reducing offset and gain matching between the two ADC cores. An internal digital calibration may start right after the 3-wire serial interface has been loaded (using data D12 of the 3-wire serial interface with address 000). This calibration might be launched several times before the optimum is reached.

The beginning of calibration disables the two ADCs and a standard data acquisition is performed. The output bit CAL goes to a high level during the entire calibration phase. When this bit returns to a low level, the two ADCs are calibrated with offset and gain and can be used again for a standard data acquisition.

If only one channel is selected (I or Q) the offset calibration duration is divided by two and no gain calibration between the two channels is necessary.

Figure 10-3. Internal Timing Calibration
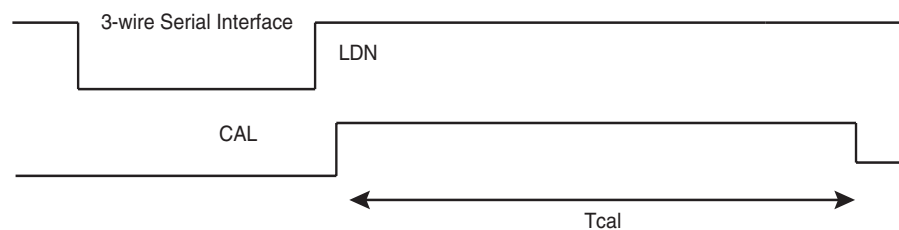
The Tcal duration is a multiple of the clock frequency ClockI (master clock). Even if a dual clock scheme is used during calibration, ClockQ will not be used.

The control wait bits (D13 and D14) give the possibility of changing the calibration's setting depending on the clock's frequency:

- For high clock rates (> 500 Msps) use a = b = 1, Tcal = 10112 clock I periods.
- For clock rates > 250 Msps and < 500 Msps use a = 1, b = 0, Tcal = 6016 clock I periods.
- For clock rates > 125 Msps and < 250 Msps use a = 0, b = 1 ,Tcal = 3968 clock I periods.
- For low clock rates (< 125 Msps) use a = 0, b = 0 , Tcal = 2944 clock I periods.

The calibration phase is necessary when using the AT84AD001C in Interleaved mode, where one analog input is sampled at both ADC cores on the common input clock's rising and falling edges. This operation is equivalent to converting the analog signal at twice the clock frequency.

Table 10-5. Matching Between Channels

Parameter	Value			Unit
	Min	Typ	Max	
Gain error (single channel I or Q) without calibration		0		%
Gain error (single channel I or Q) with calibration	−2	0	2	%
Offset error (single channel I or Q) without calibration		0		LSB
Offset error (single channel I or Q) with calibration	−2	0	2	LSB
Mean offset code without calibration (single channel I or Q)		127.5		
Mean offset code with calibration (single channel I or Q)	126	127.5	129	

During the ADC's auto-calibration phase, the dual ADC is set with the following:

• Decimation mode ON

• 1:1 DMUX mode

• Binary mode

Any external action applied to any signal of the ADC's registers is inhibited during the calibration phase.

10.1.4 Gain and Offset Compensation Functions

It is also possible for the user to have external access to the ADC's gain and offset compensation functions:

• Offset compensation between I and Q channels (at address 010)

• Gain compensation between I and Q channels (at address 011)

To obtain manual access to these two functions, which are used to set the offset to middle code 127.5 and to match the gain of channel Q with that of channel I (if only one channel is used, the gain compensation does not apply), it is necessary to set the ADC to "manual" mode by writing 0 at bits D11 and D10 of address 000.

10.1.5 Built-In Test (BIT)

A Built-In Test (BIT) function is available to allow rapid testing of the device's I/O by either applying a defined static pattern to the ADC or by generating a dynamic ramp at the ADC's output. The dynamic ramp can be used with a clock frequency of up to 1 Gsps. This function is controlled via the 3-wire bus interface at address 101.

- The BIT is active when Data0 = 1 at address 110.

- The BIT is inactive when Data0 = 0 at address 110.

- The Data1 bit allows choosing between static mode (Data1 = 0) and dynamic mode (Data1 = 1).

When the static BIT is selected (Data1 = 0), it is possible to write any 8-bit pattern by defining the Data9 to Data2 bits. Port B then outputs an 8-bit pattern equal to *Data9 ... Data2,* and Port A outputs an 8-bit pattern equal to *NOT (Data9 ... Data2)*.

Note: In 1:1 DMUX mode, the ramp test mode works with the same output rate as in 1:2 DMUX mode, ie. The change stays at the same code during 2 clock cycles instead of 1"

Example:

Address = 110

Data =

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	0	1	0	1	0	1	0	1	0	1

One should then obtain 01010101 on Port B and 10101010 on Port A.

When the dynamic mode is chosen (Data1 = 1) port B outputs a rising ramp while Port A outputs a decreasing one.

Note: In dynamic mode, use the DRDA function to align the edges of CLKO with the middle of the data.

Dynamic BIT works on channel I when Clock I is applied and on channel Q when clock Q is applied.

10.1.6 Decimation Mode

The decimation mode can be used with a clock frequency of up to 1 Gsps. In decimation mode, one data out of 16 is output, thus leading to a maximum output rate of 62.5 Msps.

Note: Frequency (CLKO) = frequency (Data) = Frequency (CLKI)/16.

10.2   Die Junction Temperature Monitoring Function

A die junction temperature measurement setting is included on the board for junction temperature monitoring.

The measurement method forces a 1 mA current into a diode-mounted transistor.

Caution should be given to respecting the polarity of the current.

In any case, one should make sure the maximum voltage compliance of the current source is limited to a maximum of 1V or use a resistor serial-mounted with the current source to avoid damaging the transistor device (this may occur if the current source is reverse-connected).

The measurement setup is illustrated in Figure 10-5 on page 42.

Figure 10-4.   Die Junction Temperature Monitoring Setup
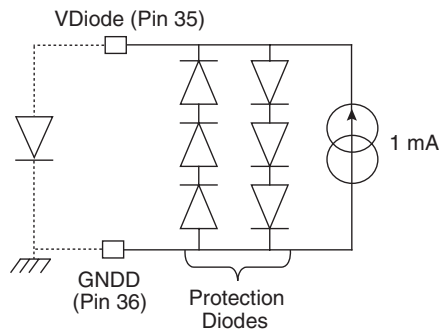
The VBE diode's forward voltage in relation to the junction temperature (in steady-state conditions) is shown in Figure 11-1.

Figure 10-5.   Diode Characteristics Versus T_J
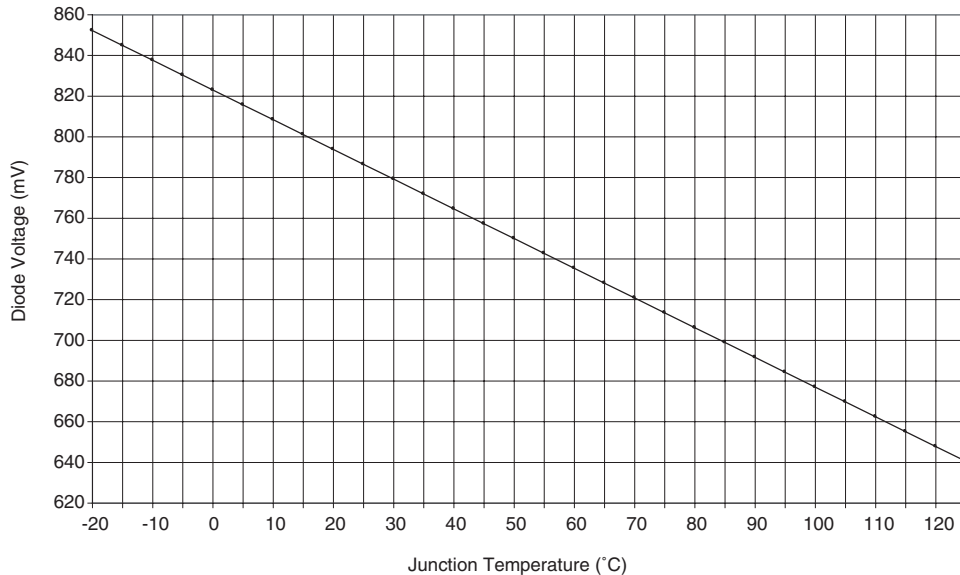
10.3   VtestI, VtestQ

VtestI and VtestQ pins are for internal test use only. These two signals must be left open.

11. Equivalent Input/Output Schematics

Figure 11-1. Simplified Input Clock Model
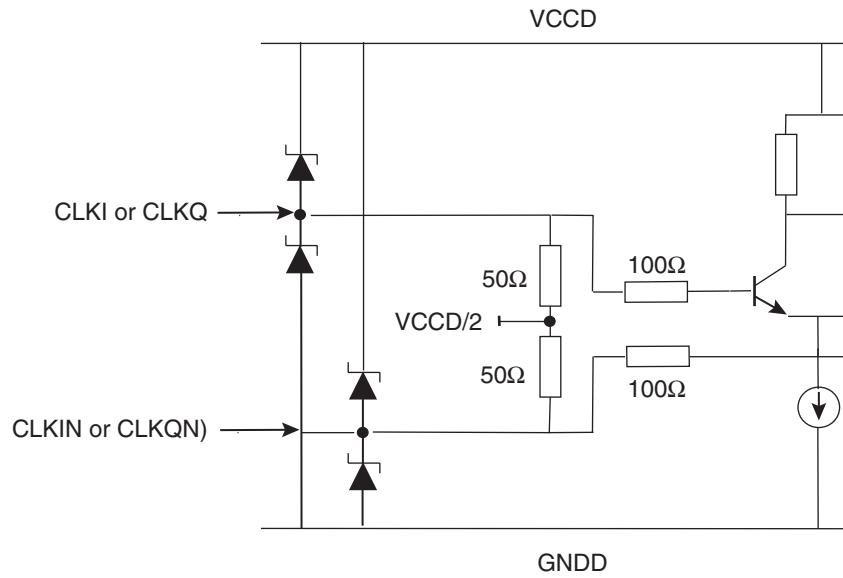
Figure 11-2. Simplified Data Ready Reset Buffer Model
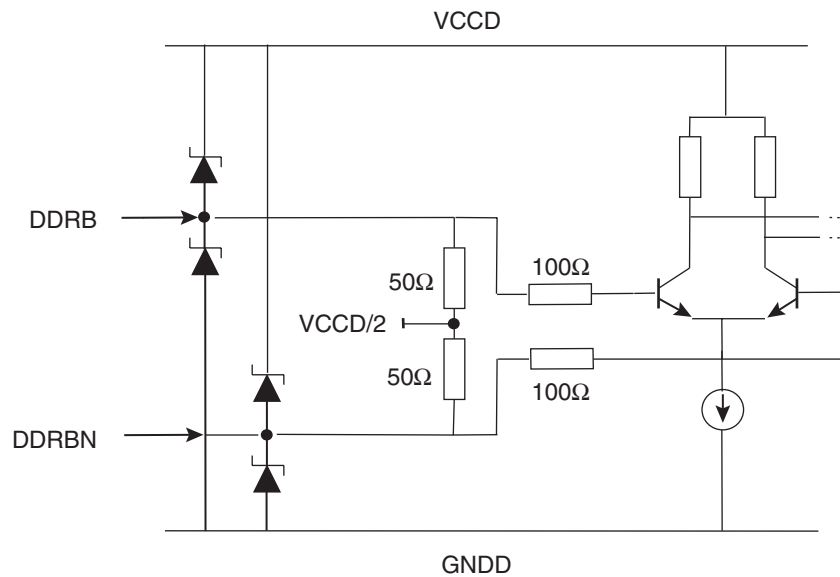
Figure 11-3. Analog Input Model
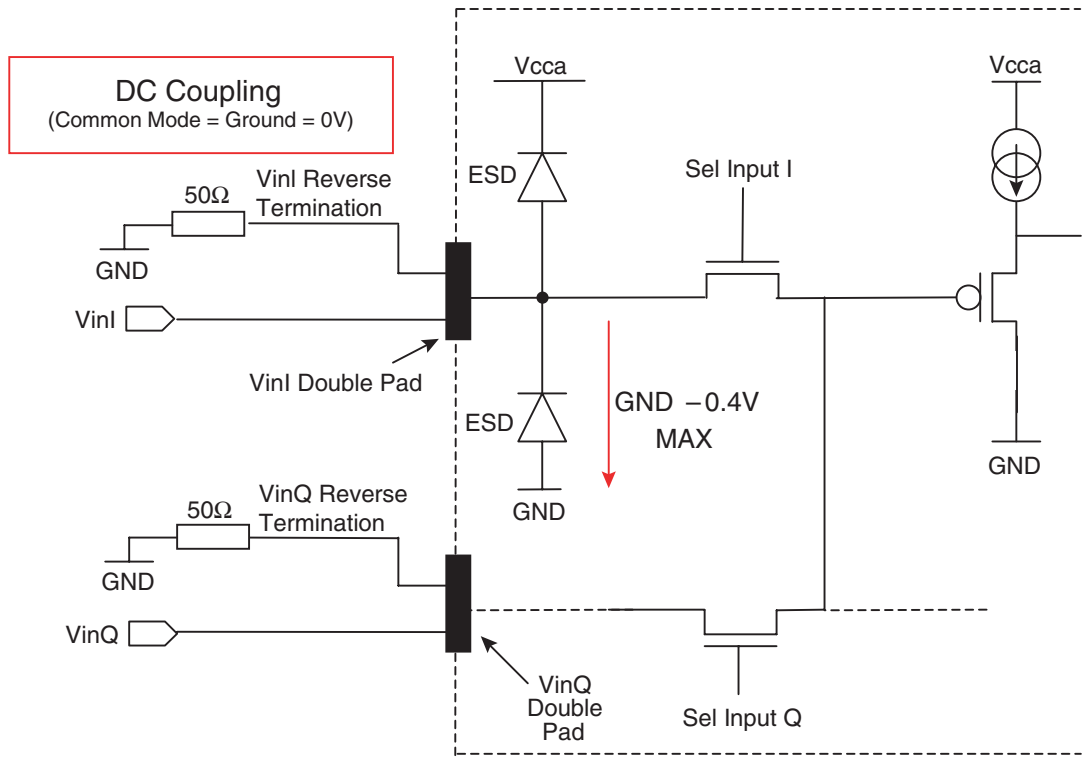
Figure 11-4. Data Output Buffer Model
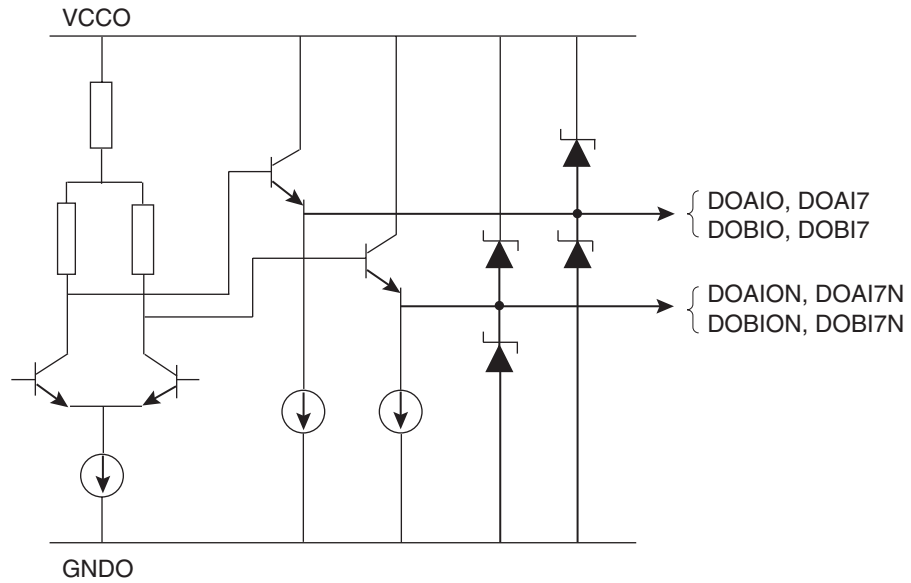
12. Definitions of Terms

Table 12-1. Definitions of Terms

Abbreviation	Definition	Description
BER	Bit Error Rate	The probability of an error occurring on the output at a maximum sampling rate.
DNL	Differential Non-Linearity	The differential non-linearity for an output code i is the difference between the measured step size of code i and the ideal LSB step size. DNL (i) is expressed in LSBs. DNL is the maximum value of all DNL (i). A DNL error specification of less than 1 LSB guarantees that there are no missing output codes and that the transfer function is monotonic
ENOB	Effective Number of Bits	$ENOB = \dfrac{SINAD - 1,76 + 20\ \log\left[\dfrac{A}{Fs/2}\right]}{6,02}$ Where A is the actual input amplitude and Fs is the full scale range of the ADC under test
FPBW	Full Power Input Bandwidth	The analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at full-scale −1 dB (−1 dBFS)
IMD	Inter-Modulation Distortion	The two tones intermodulation distortion (IMD) rejection is the ratio of either of the two input tones to the worst third order intermodulation products
INL	Integral Non-Linearity	The integral non-linearity for an output code i is the difference between the measured input voltage at which the transition occurs and the ideal value of this transition. INL (i) is expressed in LSBs and is the maximum value of all |INL (i)|
JITTER	Aperture uncertainty	The sample-to-sample variation in aperture delay. The voltage error due to jitters depends on the slew rate of the signal at the sampling point
NPR	Noise Power Ratio	The NPR is measured to characterize the ADC's performance in response to broad bandwidth signals. When applying a notch-filtered broadband white noise signal as the input to the ADC under test, the Noise Power Ratio is defined as the ratio of the average out-of-notch to the average in-notch power spectral density magnitudes for the FFT spectrum of the ADC output sample test
ORT	Overvoltage Recovery Time	The time to recover a 0.2% accuracy at the output, after a 150% full-scale step applied on the input is reduced to midscale
PSRR	Power Supply Rejection Ratio	The ratio of input offset variation to a change in power supply voltage
SFDR	Spurious Free Dynamic Range	The ratio expressed in dB of the RMS signal amplitude, set at 1 dB below full-scale, to the RMS value of the highest spectral component (peak spurious spectral component). The peak spurious component may or may not be a harmonic. It may be reported in dB (related to the converter −1 dB full-scale) or in dBc (related to the input signal level)
SINAD	Signal to Noise and Distortion Ratio	The ratio expressed in dB of the RMS signal amplitude, set to 1 dB below full-scale (−1 dBFS) to the RMS sum of all other spectral components including the harmonics, except DC
SNR	Signal to Noise Ratio	The ratio expressed in dB of the RMS signal amplitude, set to 1 dB below full-scale, to the RMS sum of all other spectral components excluding the first 9 harmonics
SSBW	Small Signal Input Bandwidth	The analog input frequency at which the fundamental component in the digitally reconstructed output waveform has fallen by 3 dB with respect to its low frequency value (determined by FFT analysis) for input at full-scale −10 dB (−10 dBFS)
TA	Aperture delay	The delay between the rising edge of the differential clock inputs (CLKI, CLKIN) [zero crossing point] and the time at which VIN and VINB are sampled
TC	Encoding Clock period	TC1 = minimum clock pulse width (high) TC = TC1 + TC2 TC2 = minimum clock pulse width (low)
TD1	Time delay data to clock	Time delay between Data transition (Port A or B) channel I or Q to Output Clock CLKXO (channel I or Q) If Output Clock CLKXO is in the middle to data TD1 = Tdata/2
TD2	Time delay clock to data	Time delay between Output Clock CLKXO (channel I or Q) to Data transition (Port A or B) channel I or Q If Output Clock CLKXO is in the middle to data TD2 = Tdata/2

**Table 12-1.** Definitions of Terms (Continued)

Abbreviation	Definition	Description
TD1-TD2		This difference TD1-TD2 gives an information if Output Clock CLKXO (channel I or Q) is centered on the output data If Output Clock CLKXO is in the middle to data TD2=TD1=Tdata/2
TDO	Digital Data Output Delay	The delay from the rising edge of the differential clock inputs (CLKI, CLKIN) [zero crossing point] to the next point of change in the differential output data (zero crossing) with a specified load
TDR	Data Ready Output Delay	The delay from the falling edge of the differential clock inputs (CLKI, CLKIN) [zero crossing point] to the next point of change in the differential output data (zero crossing) with a specified load
TF	Fall Time	The time delay for the output data signals to fall from 20% to 80% of delta between the low and high levels
THD	Total Harmonic Distortion	The ratio expressed in dB of the RMS sum of the first 9 harmonic components to the RMS input signal amplitude, set at 1 dB below full-scale. It may be reported in dB (related to the converter –1 dB full-scale) or in dBc (related to the input signal level)
TPD	Pipeline Delay	The number of clock cycles between the sampling edge of an input data and the associated output data made available (not taking into account the TDO)
TR	Rise Time	The time delay for the output data signals to rise from 20% to 80% of delta between the low and high levels
TRDR	Data Ready Reset Delay	The delay between the falling edge of the Data Ready output asynchronous reset signal (DDRB) and the reset to digital zero transition of the Data Ready output signal (DR)
TS	Settling Time	The time delay to rise from 10% to 90% of the converter output when a full-scale step function is applied to the differential analog input
VSWR	Voltage Standing Wave Ratio	The VSWR corresponds to the ADC input insertion loss due to input power reflection. For example, a VSWR of 1.2 corresponds to a 20 dB return loss (99% power transmitted and 1% reflected)

13. Using the AT84AD001C Dual 8-bit 1 Gsps ADC

13.1 Decoupling, Bypassing and Grounding of Power Supplies

The following figures show the recommended bypassing, decoupling and grounding schemes for the dual 8-bit 1 Gsps ADC power supplies.

Figure 13-1. V_{CCD} and V_{CCA} Bypassing and Grounding Scheme
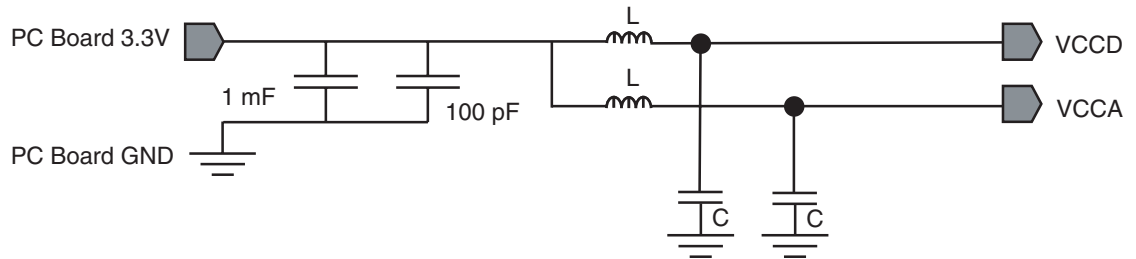
Figure 13-2. V_{CCO} Bypassing and Grounding Scheme
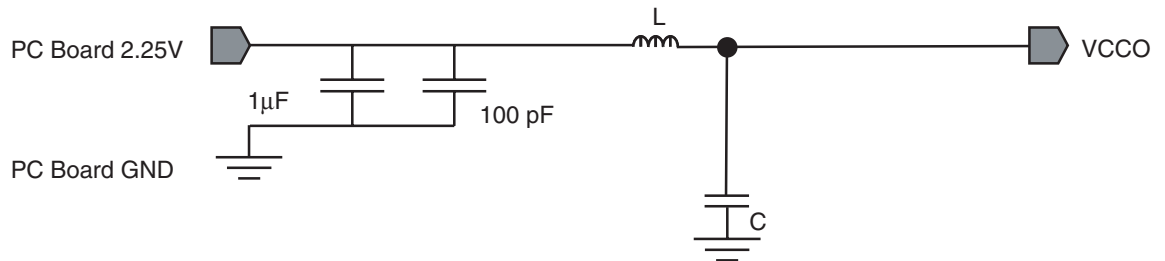
Note: L and C values must be chosen in accordance with the operation frequency of the application.

Figure 13-3. Power Supplies Decoupling Scheme
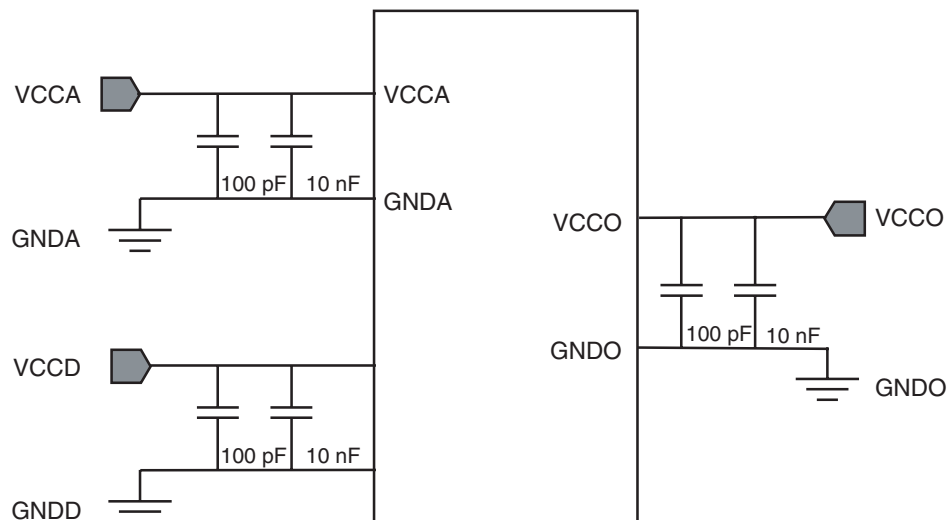
Note: The bypassing capacitors (1 μF and 100 pF) should be placed as close as possible to the board connectors, whereas the decoupling capacitors (100 pF and 10 nF) should be placed as close as possible to the device.

13.2 Analog Input Implementation

The analog inputs of the dual ADC have been designed with a double pad implementation as illustrated in Figure 13-5 on page 49. The reverse pad for each input should be tied to ground via a 50Ω resistor.

The analog inputs must be used in differential mode only.

Figure 13-4. Termination Method for the ADC Analog Inputs in DC Coupling Mode
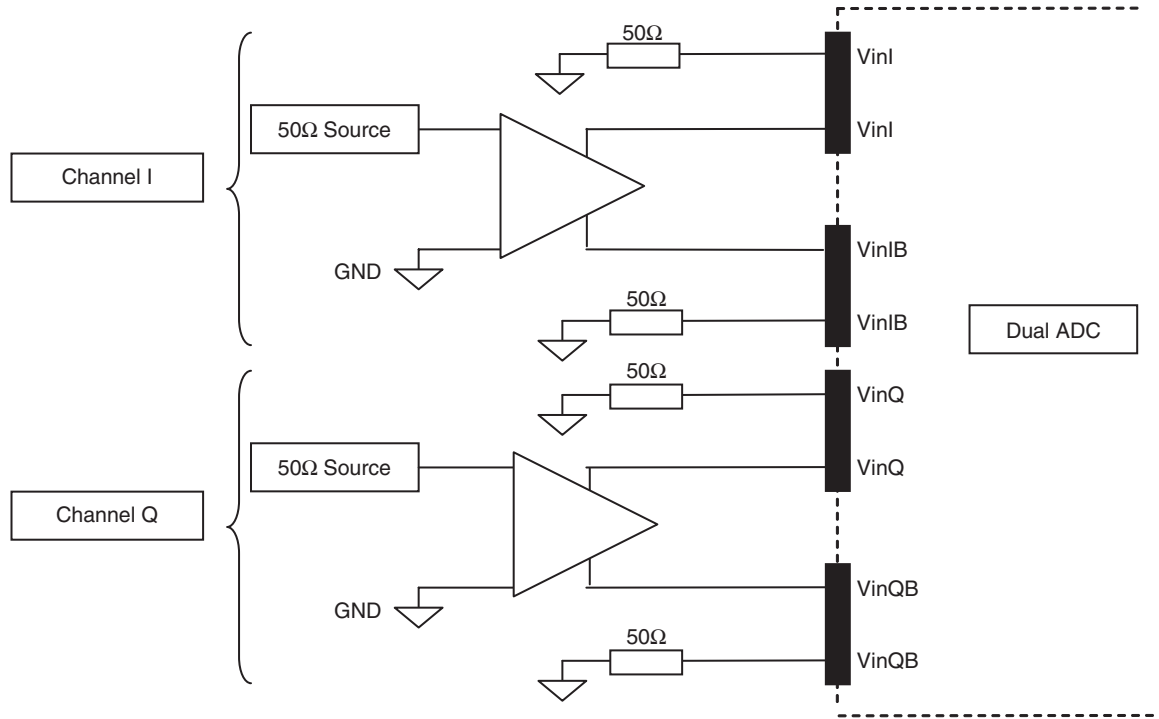
Figure 13-5. Termination Method for the ADC Analog Inputs in AC Coupling Mode
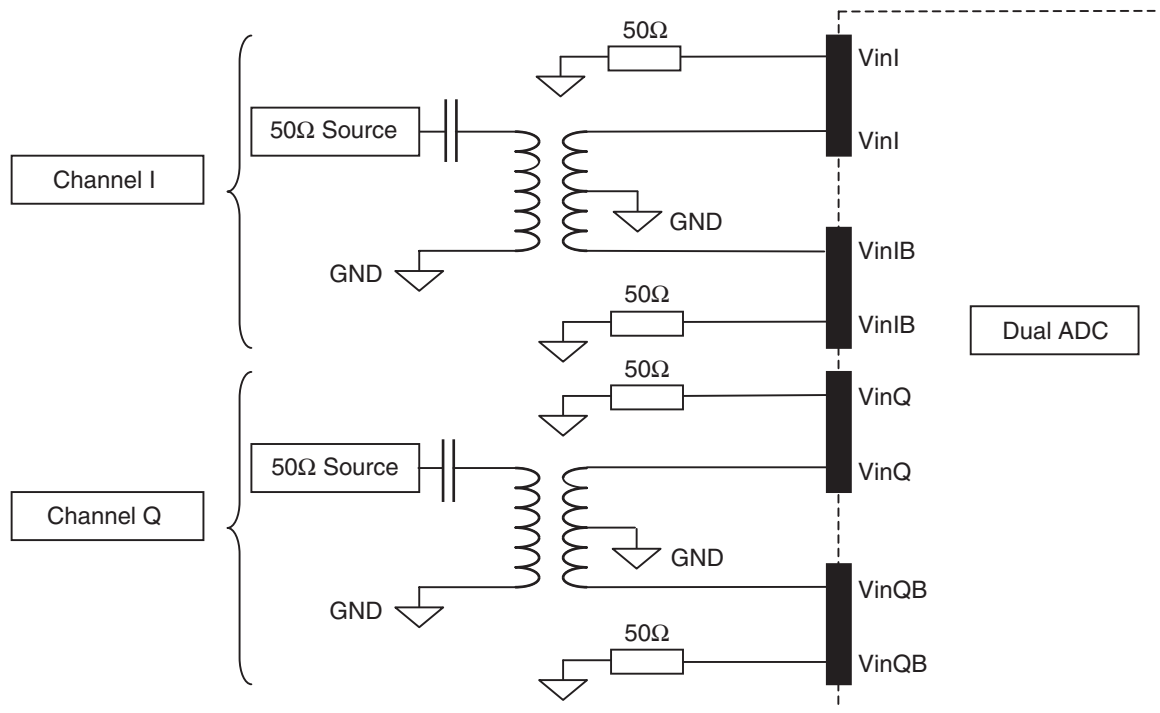
13.3 Clock Implementation

The ADC features two different clocks (I or Q) that must be implemented as shown in Figure 13-6. Each path must be AC coupled with a 100 nF capacitor.

Figure 13-6. Differential Termination Method for Clock I or Clock Q
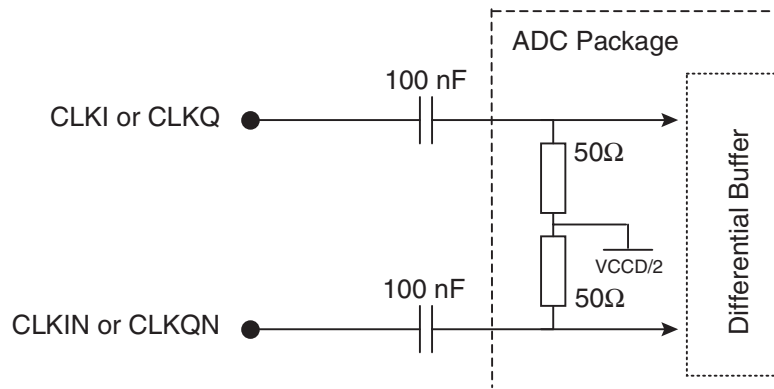
Note: When only clock I is used, it is not necessary to add the capacitors on the CLKQ and CLKQN signal paths; they may be left floating.

Figure 13-7. Single-ended Termination Method for Clock I or Clock Q
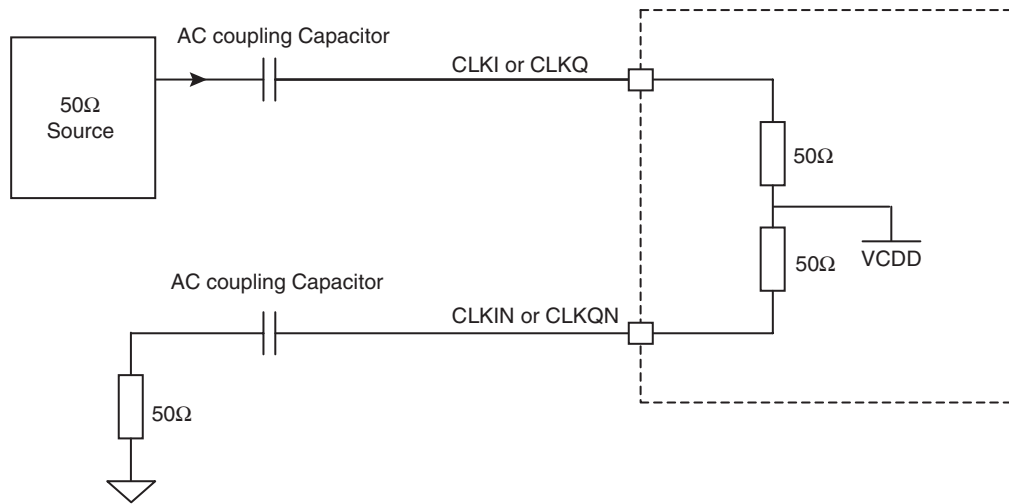
13.4 Reset Implementation

DDRB may be implemented as described in the following figure. A pull-up resistor is implemented to maintain the DDRB signal inactive in normal mode. The Data Ready Reset command (it might be a pulse) is active on the high level.

Figure 13-8. Reset Implementation
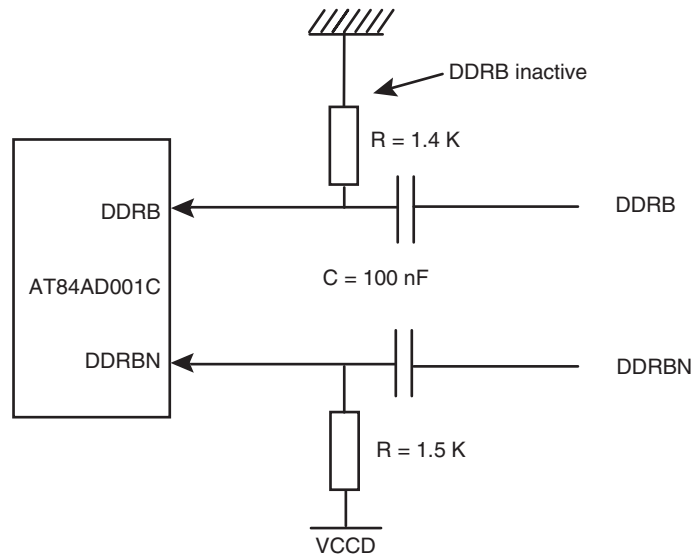
Note: The external pull and pull down resistors are needed to bias the differential pair in AC coupling. They are of no use in DC coupling (when used with an LVDS driver).

13.5 Output Termination in 1:1 Ratio

When using the integrated DMUX in 1:1 ratio, the valid port is port A. Port B remains unused.

Port A functions in LVDS mode and the corresponding outputs (DOAI or DOAQ) have to be 100Ω differentially terminated as shown in Figure 13-9.

The pins corresponding to Port B (DOBI or DOBQ pins) must be left floating (in high impedance state).

Figure 13-9 shows the example of a 1:1 ratio of the integrated DMUX for channel I (the same applies to channel Q).

Figure 13-9. Example of Termination for Channel I Used in DMUX 1:1 Ratio (Port B Unused)
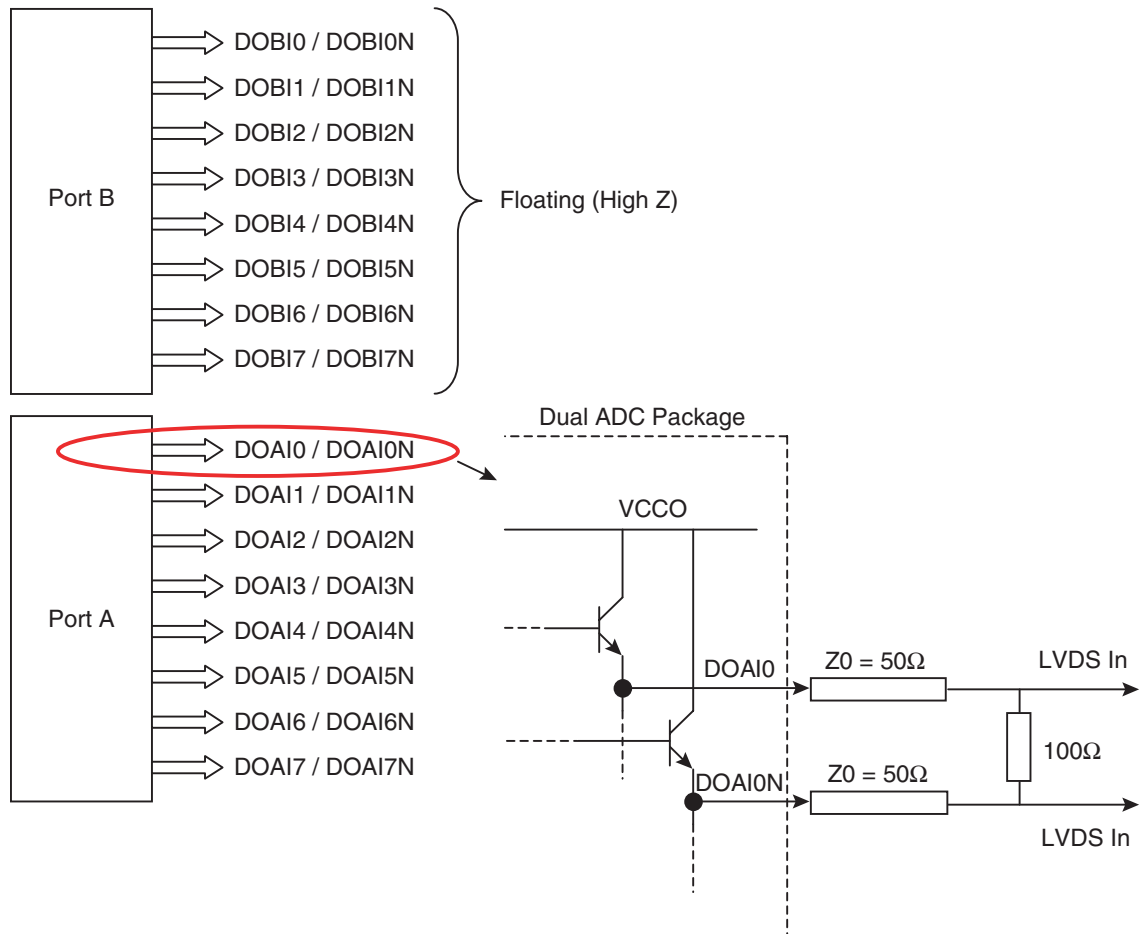
Note: If the outputs are to be used in single-ended mode, it is recommended that the true and false signals be terminated with a 50Ω resistor.

13.6 Using the Dual ADC With and ASIC/FPGA Load

Figure 13-10 illustrates the configuration of the dual ADC (1:2 DMUX mode, independent I and Q clocks) driving an LVDS system (ASIC/FPGA) with potential additional DMUXes used to halve the speed of the dual ADC outputs.

Figure 13-10. Dual ADC and ASIC/FPGA Load Block Diagram
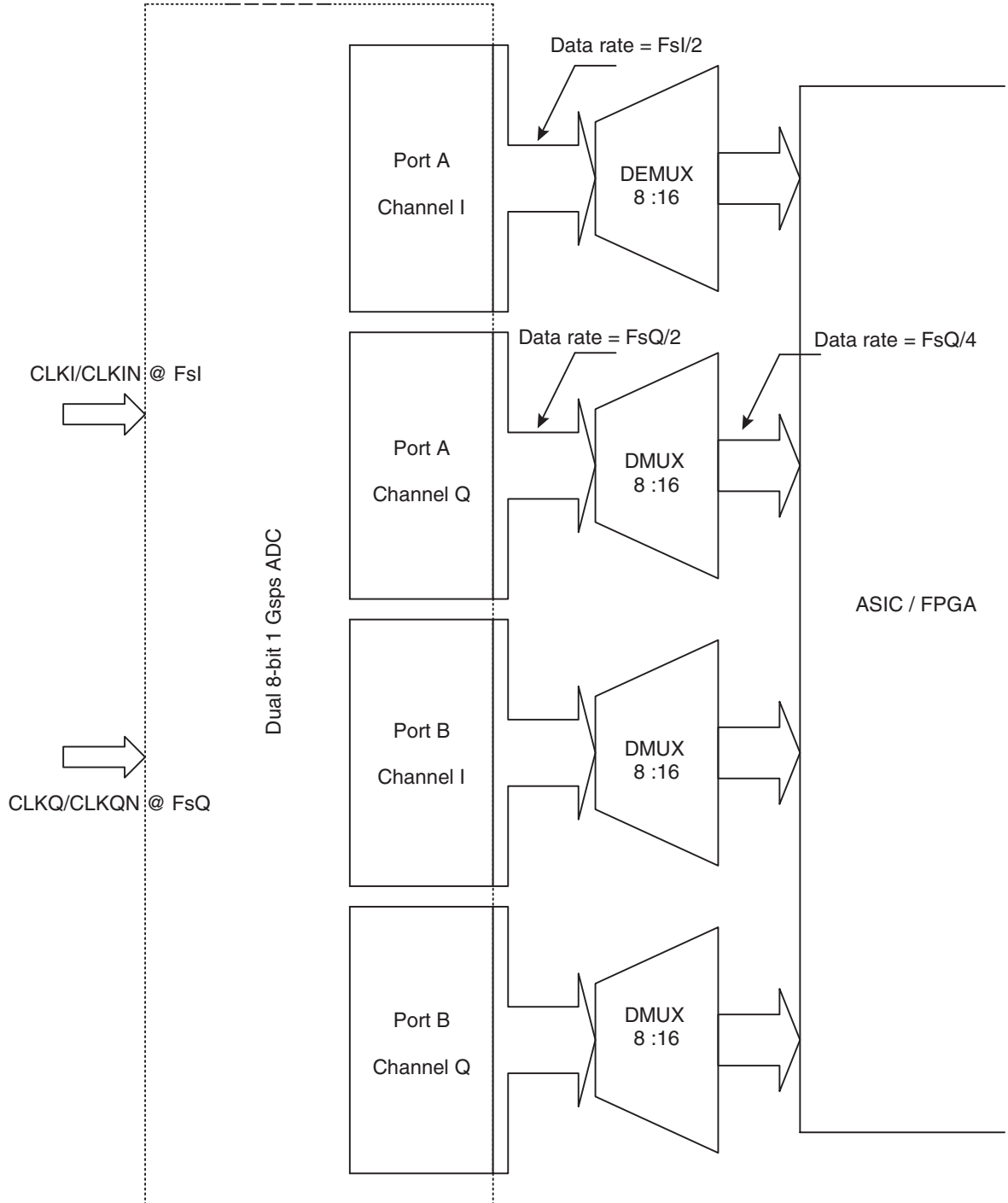
Note: The demultiplexers may be internal to the ASIC/FPGA system.

14. Thermal Characteristics

14.1 Simplified Thermal Model for LQFP 144 20 × 20 × 1.4 mm

The following model has been extracted from the ANSYS FEM simulations.

Assumptions: no air, no convection and no board.

Figure 14-1. Simplified Thermal Model for LQFP Package
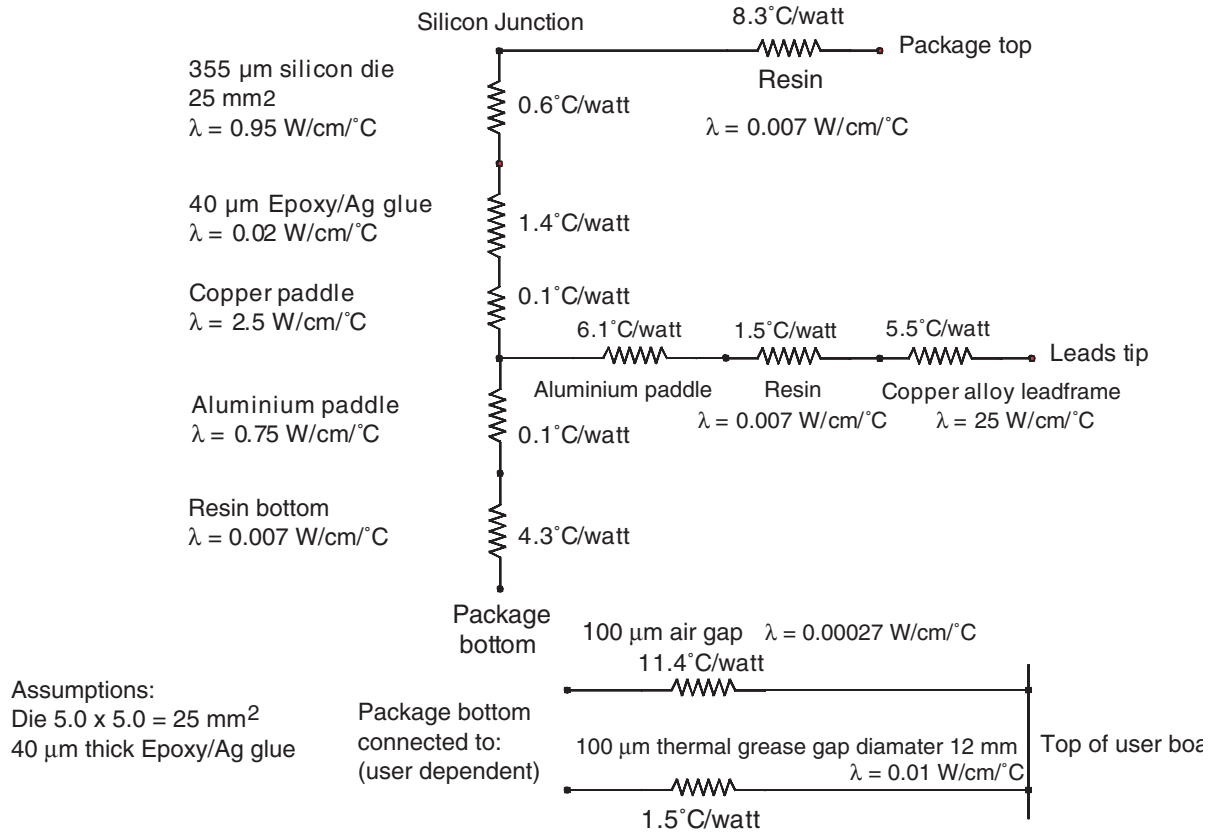
Note: The above are typical values with an assumption of uniform power dissipation over 2.5 × 2.5 mm^2 of the top surface of the die.

14.1.0.1 *Thermal Resistance from Junction to Bottom of Leads*

Assumptions: no air, no convection and no board.

The thermal resistance from the junction to the bottom of the leads is 15.2°C/W typical.

14.1.0.2 *Thermal Resistance from Junction to Top of Case*

Assumptions: no air, no convection and no board.

The thermal resistance from the junction to the top of the case is 8.3°C/W typical.

14.1.0.3 *Thermal Resistance from Junction to Bottom of Case*

Assumptions: no air, no convection and no board.

The thermal resistance from the junction to the bottom of the case is 6.4°C/W typical.

14.1.0.4 *Thermal Resistance from Junction to Bottom of Air Gap*

The thermal resistance from the junction to the bottom of the air gap (bottom of package) is 17.9°C/W typical.

14.1.0.5 *Thermal Resistance from Junction to Ambient*

The thermal resistance from the junction to ambient is 25.2°C/W typical.

Note: In order to keep the ambient temperature of the die within the specified limits of the device grade (that is T_{amb} max = 70°C in commercial grade and 85°C in industrial grade) and the die junction temperature below the maximum allowed junction temperature of 105°C, it is necessary to operate the dual ADC in air flow conditions (1m/s recommended).

In still air conditions, the junction temperature is indeed greater than the maximum allowed T_J.
- T_J = 25.2 °C/W × 1.4W + T_{amb} = 35.28 + 70 = 105.28 °C for commercial grade devices
- T_J = 25.2 °C/W × 1.4W + T_{amb} = 35.28 + 85 = 125.28 °C for industrial grade devices

14.1.0.6 *Thermal Resistance from Junction to Board*

The thermal resistance from the junction to the board is 13°C/W typical.

14.2 LQFP-ep 144L Green Package Thermal Characteristics

14.2.1 Thermal Resistance from Junction to Ambient

Simulations (JEDEC JESD51 standard) were held with the following assumptions:

• Board with 76.2 mm x 114.3 mm dimensions

• Still air

• Exposed pad (5.8 x 5.8 mm) soldered to the board

The thermal resistance from the junction to ambient is 25.0 °C/W.

Note: when the exposed pad is not soldered to the board, the Rthj-a becomes 58.8°C/W.

14.2.2 Exposed pad Board layout recommendation

This recommendation is done for the AT84AD001CXEPW (LQFP-ep 144L green package).

Electrical contact of the part to the Printed Circuit Board (PCB) is made by soldering the leads on the bottom surface of the package to the PCB. Hence; special attention is require to the heat transfer below the package to provide a good thermal bond to the PCB.

A Copper (Cu) fill is to be designed into PCB as a thermal pad under the package. Heat from devices, is conducted to the PCB at the thermal pad. It is then conducted from the thermal pad to the PCB inner ground plane by a 6.5 array of via. The LQFP metal died paddle must be soldered to the PCB's thermal pad.

Solder mask is placed on the board top side **over each via** to resist solder flow into the via.

The diameter of solder Mask needs to be higher than diameter of via (**diameter of via+ 0.2 mm**)

The diameter of solder Mask is 0.3 mm + 0.1 mm + 0.1 mm = 0.5 mm)

The Solder Paste template needs to de designed to allow at least **50% solder coverage**.

The Solder Paste is place between the balls (diamond area) and not covers all the copper.
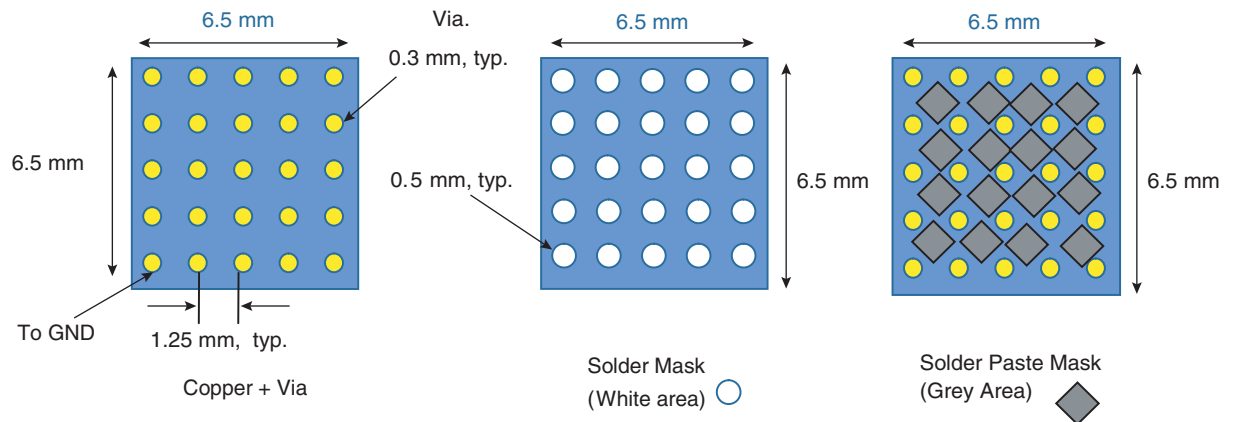
The thermal via is connected to inner layer (GND layer) with **complete connection**.
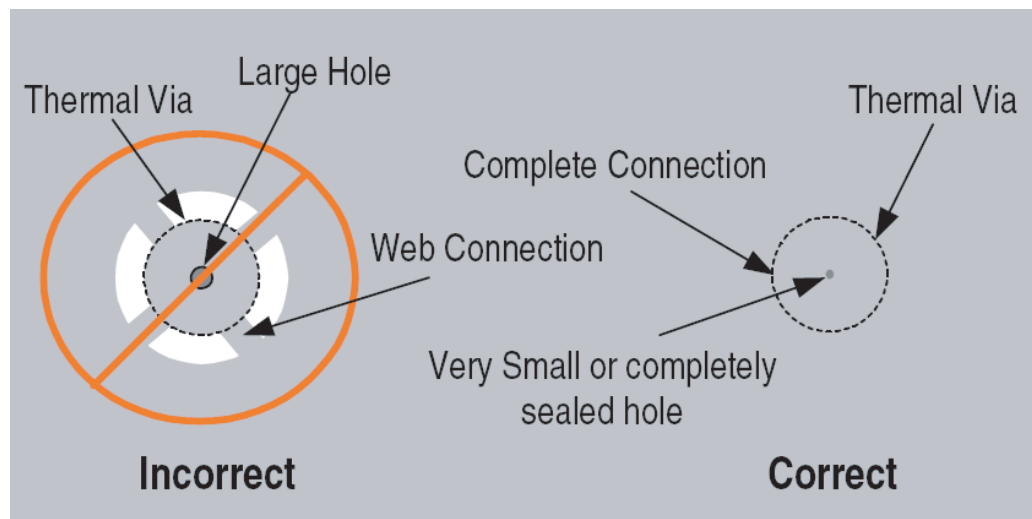
15. Ordering Information

Table 15-1. Ordering Information

Part Number	Package	Temperature Range	Screening	Comments
AT84AD001CCTD	LQFP 144	C grade $0°C < T_{amb} < 70°C$	Standard	Please contact your local sales office
AT84AD001CVTD	LQFP 144	V grade $-40°C < T_{amb} < 85°C$	Standard	Please contact your local sales office
AT84XAD001CEPW	LQFP-ep 144L green (RoHS compliant)	Ambient	Prototype	
AT84AD001CCEPW	LQFP-ep 144L green (RoHS compliant)	C grade $0°C < T_{amb} < 70°C$	Standard	
AT84AD001CVEPW	LQFP-ep 144L green (RoHS compliant)	V grade $-40°C < T_{amb} < 85°C$	Standard	
AT84AD001TD-EB	LQFP 144	Ambient	Prototype	Evaluation Kit

16. Packaging Information

Figure 16-1. LQFP 144 Package
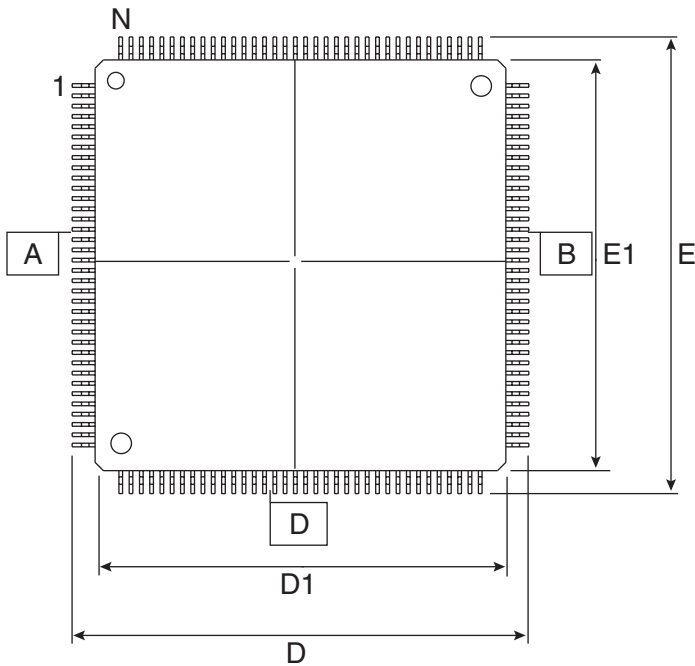
Body +2.00 mm footprint		
Dims.	Tols. Leads	144L
A	max.	1.60
A1		0.05 min./0.15 max.
A2	+/- 0.05	1.40
D	+/-0.20	22.00
D1	+/-0.10	20.00
E	+/-0.20	22.00
E1	+/-0.10	20.00
L	+0.15/-0.10	0.60
e	basic	0.50
b	+/-0.05	0.22
ddd		0.08
ccc	max.	0.08
o		$0°- 5°$

Notes: 1. All dimensions are in millimeters
2. Dimensions shown are nominal with tolerances as indicated
3. L/F: eftec 64T copper or equivalent
4. Foot length: "L" is measured at gauge plane
   at 0.25 mm above the seating plane
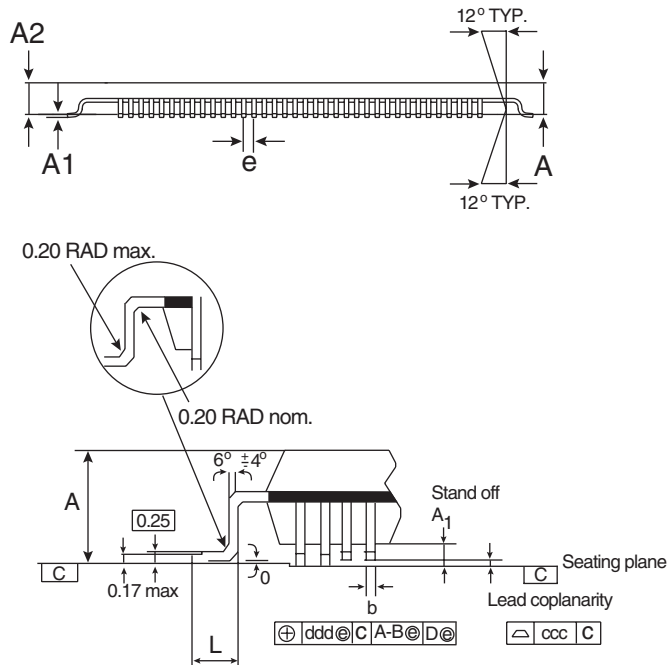
Note: Thermally enhanced package: LQFP 144, 20 × 20 × 1.4 mm.

Figure 16-2. LQFP-ep 144L Green Package
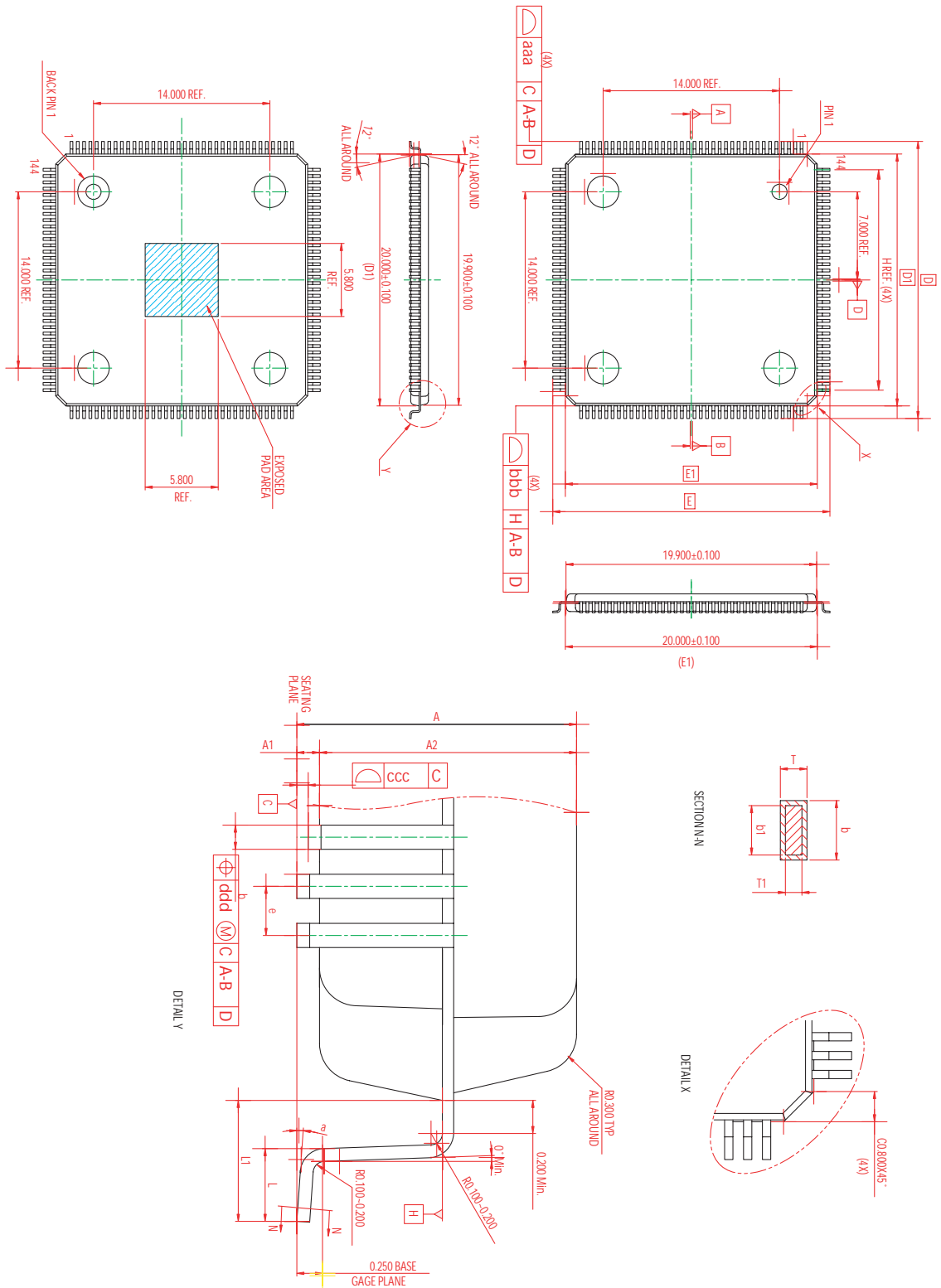
Figure 16-3. Dimensions

DIMENSION LIST (FOOTPRINT: 2.00)

S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 1.600	OVERALL HEIGHT
2	A1	0.100±0.050	STANDOFF
3	A2	1.400±0.050	PKG THICKNESS
4	D	22.000±0.200	LEAD TIP TO TIP
5	D1	20.000±0.100	PKG LENGTH
6	E	22.000±0.200	LEAD TIP TO TIP
7	E1	20.000±0.100	PKG WIDTH
8	L	0.600±0.150	FOOT LENGTH
9	L1	1.000 REF.	LEAD LENGTH
10	T	$0.150^{+0.050}_{-0.060}$	LEAD THICKNESS
11	T1	0.127±0.030	LEAD BASE METAL THICKNESS
12	a	0˚~7˚	FOOT ANGLE
13	b	0.220±0.050	LEAD WIDTH
14	b1	0.200±0.030	LEAD BASE METAL WIDTH
15	e	0.500 BASE	LEAD PITCH
16	H (REF.)	(17.500)	CUM. LEAD PITCH
17	aaa	0.200	PROFILE OF LEAD TIPS
18	bbb	0.200	PROFILE OF MOLD SURFACE
19	ccc	0.080	FOOT COPLANARITY
20	ddd	0.080	FOOT POSITION

NOTES :

S/N	DESCRIPTION		SPECIFICATION
1	GENERAL TOLERANCE.	DISTANCE	±0.100
		ANGLE	±2.5˚
2	MATTE FINISH ON PACKAGE BODY SURFACE EXCEPT EJECTION AND PIN 1 MARKING.		Ra0.8~2.0 um
3	ALL MOLDED BODY SHARP CORNER RADII UNLESS OTHERWISE SPECIFIED.		MAX. R0.200
4	PACKAGE/LEADFRAME MISALIGNMENT (X, Y):		MAX. 0.127
5	TOP/BTM PACKAGE MISALIGNMENT (X, Y):		MAX. 0.127
6	DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OR CUTTING BURR.		
7	COMPLIANT TO JEDEC STANDARD: MS-026		

FOR HIGH DENSITY STRIP LAYOUT

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