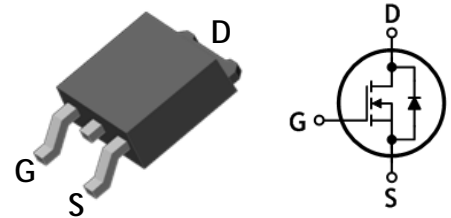


HIGH SPEED SWITCHING APPLICATION

Features

- Low drain-source On resistance: $R_{DS(on)}=1.23\Omega$ (Typ.)
- Low gate charge: $Q_g=10.5nC$ (Typ.)
- Low reverse transfer capacitance: $C_{rss}=2pF$ (Typ.)
- Halogen free device and RoHS compliant device
- 100% avalanche tested

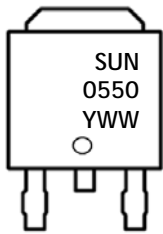


Ordering Information

Part Number	Marking	Package
SUN0550D	SUN0550	TO-252

TO-252

Marking Information



Column 1, 2: Device Code
 Column 3: Production Information
 e.g.) YWW
 -. Y: Year Code
 -. WW: Week Code

Absolute maximum ratings ($T_c=25^\circ C$ unless otherwise noted)

Characteristic	Symbol	Rating	Unit	
Drain-source voltage	V_{DSS}	500	V	
Gate-source voltage	V_{GSS}	± 30	V	
Drain current (DC) *	I_D	$T_c=25^\circ C$	4.5	A
		$T_c=100^\circ C$	2.85	A
Drain current (Pulsed) *	I_{DM}	18	A	
Single pulsed avalanche energy ^(Note 2)	E_{AS}	281	mJ	
Repetitive avalanche current ^(Note 1)	I_{AR}	4.5	A	
Repetitive avalanche energy ^(Note 1)	E_{AR}	4.8	mJ	
Power dissipation	P_D	48	W	
Junction temperature	T_J	150	$^\circ C$	
Storage temperature range	T_{stg}	-55-150	$^\circ C$	

* Limited only maximum junction temperature

Thermal Characteristics

Characteristic	Symbol	Rating	Unit
Thermal resistance, junction to case	$R_{th(j-c)}$	Max. 2.6	°C/W
Thermal resistance, junction to ambient	$R_{th(j-a)}$	Max. 62.5	

Electrical Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	BV_{DSS}	$I_D=250\mu\text{A}$, $V_{GS}=0$	500	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$I_D=250\mu\text{A}$, $V_{DS}=V_{GS}$	3	-	5	V
Drain-source cut-off current	I_{DSS}	$V_{DS}=500\text{V}$, $V_{GS}=0\text{V}$	-	-	1	μA
		$V_{DS}=400\text{V}$, $T_C=125^\circ\text{C}$	-	-	10	μA
Gate leakage current	I_{GSS}	$V_{DS}=0\text{V}$, $V_{GS}=\pm 30\text{V}$	-	-	± 100	nA
Drain-source on-resistance	$R_{DS(ON)}$	$V_{GS}=10\text{V}$, $I_D=2.25\text{A}$	-	1.23	1.5	Ω
Forward transfer conductance (Note 3)	g_{fs}	$V_{DS}=10\text{V}$, $I_D=2.25\text{A}$	-	4.5	-	S
Input capacitance	C_{iss}	$V_{DS}=25\text{V}$, $V_{GS}=0\text{V}$, $f=1.0\text{MHz}$	-	760	-	pF
Output capacitance	C_{oss}		-	65	-	
Reverse transfer capacitance	C_{rss}		-	2	-	
Turn-on delay time (Note 3,4)	$t_{d(on)}$	$V_{DD}=250\text{V}$, $I_D=4.5\text{A}$, $R_G=25\Omega$	-	35	-	ns
Rise time (Note 3,4)	t_r		-	26	-	
Turn-off delay time (Note 3,4)	$t_{d(off)}$		-	80	-	
Fall time (Note 3,4)	t_f		-	19	-	
Total gate charge (Note 3,4)	Q_g	$V_{DS}=400\text{V}$, $V_{GS}=10\text{V}$, $I_D=4.5\text{A}$	-	10.5	15	nC
Gate-source charge (Note 3,4)	Q_{gs}		-	4	-	
Gate-drain charge (Note 3,4)	Q_{gd}		-	2	-	

Source-Drain Diode Ratings and Characteristics ($T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	I_S	Integral reverse diode in the MOSFET	-	-	4.5	A
Source current (Pulsed)	I_{SM}		-	-	18	A
Forward voltage	V_{SD}	$V_{GS}=0\text{V}$, $I_S=4.5\text{A}$	-	-	1.4	V
Reverse recovery time (Note 3,4)	t_{rr}	$I_S=4.5\text{A}$, $V_{GS}=0\text{V}$ $dI_F/dt=100\text{A}/\mu\text{s}$	-	330	-	ns
Reverse recovery charge (Note 3,4)	Q_{rr}		-	1.15	-	μC

Note:

1. Repeated rating: Pulse width limited by safe operating area
2. $L=25\text{mH}$, $I_{AS}=4.5\text{A}$, $V_{DD}=50\text{V}$, $R_G=25\Omega$, Starting $T_J=25^\circ\text{C}$
3. Pulse test: Pulse width $\leq 300\mu\text{s}$, Duty cycle $\leq 2\%$
4. Essentially independent of operating temperature typical characteristics

Electrical Characteristics Curves

Fig. 1 Typical Output Characteristics

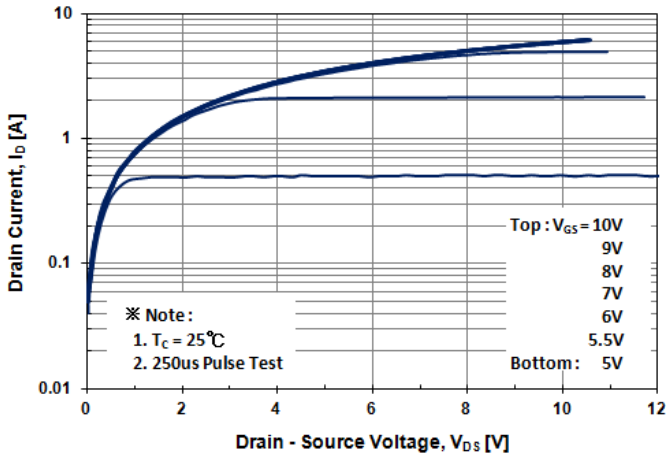


Fig. 2 Typical Output Characteristics

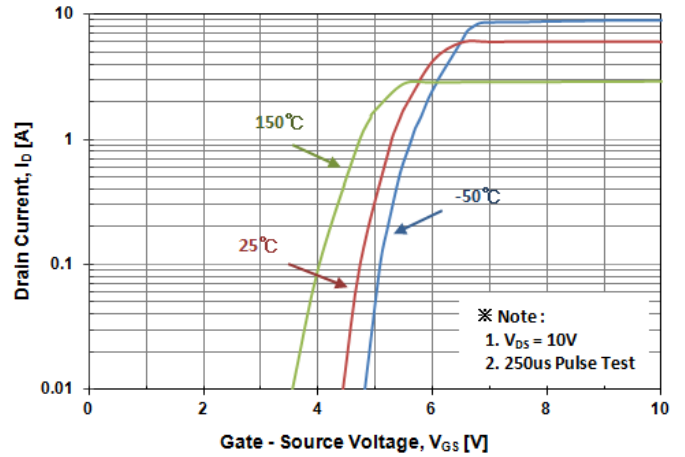


Fig.3 On-Resistance Variation with Drain Current and Gate Voltage

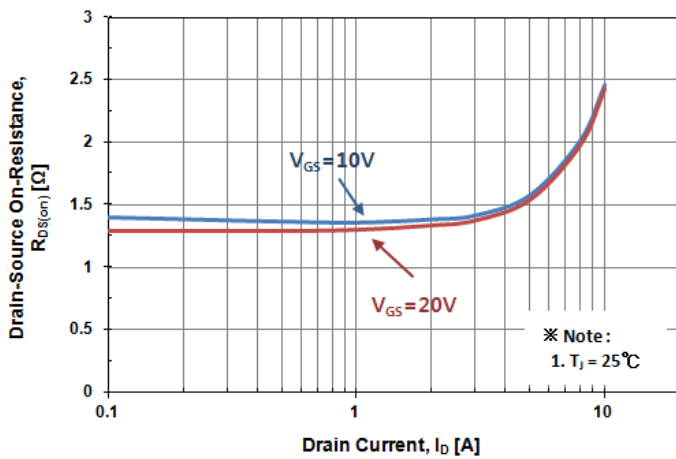


Fig. 4 Body Diode Forward Voltage Variation with Source Current and Temperature

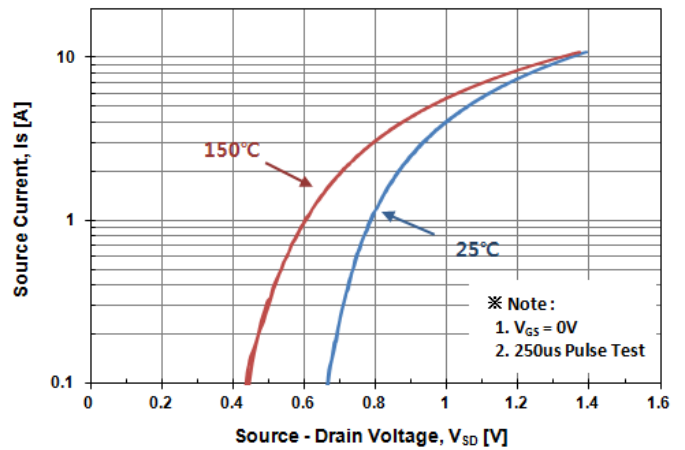


Fig. 5 Typical Capacitance Characteristics

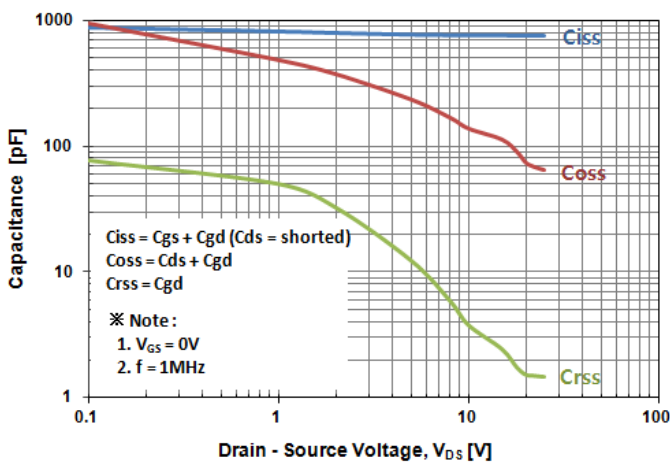


Fig. 6 Typical Total Gate Charge Characteristics

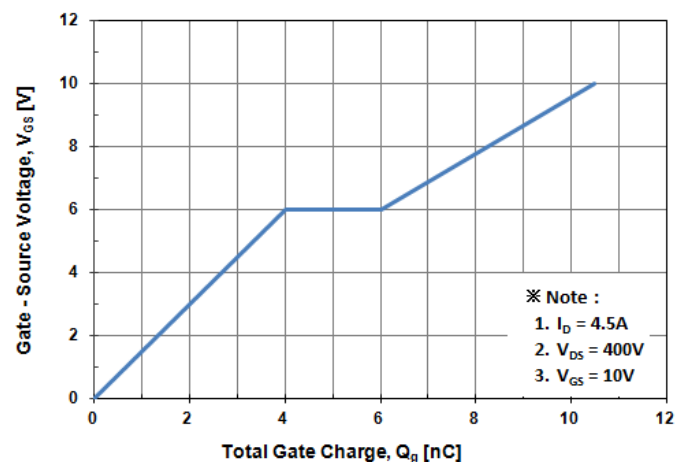


Fig. 7 Breakdown Voltage Variation vs. Temperature

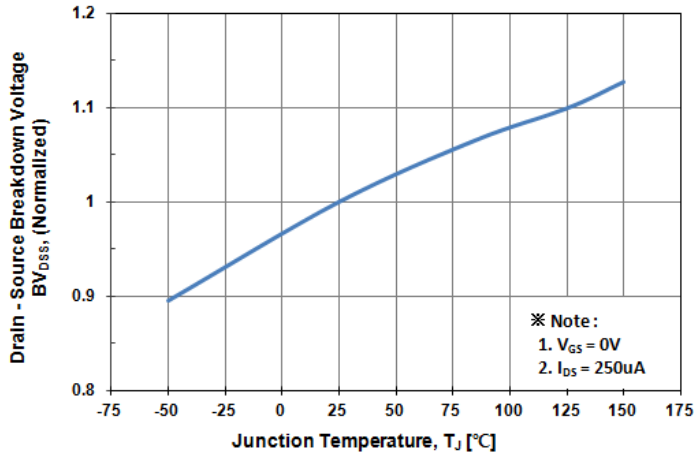


Fig. 8 On-Resistance Variation vs. Temperature

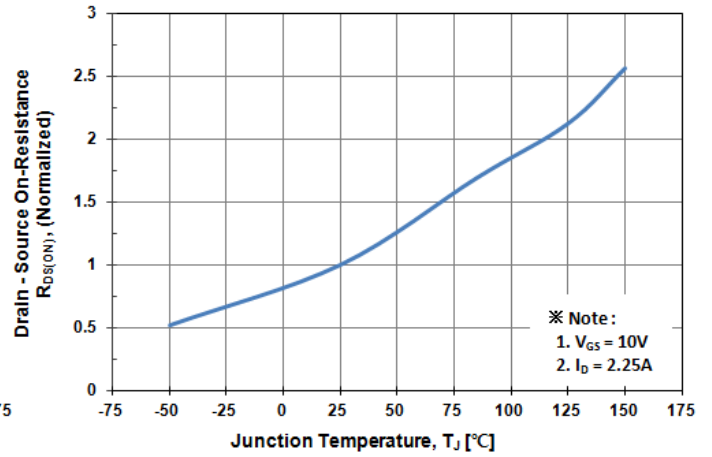


Fig. 9 Maximum Drain Current vs. Case Temperature

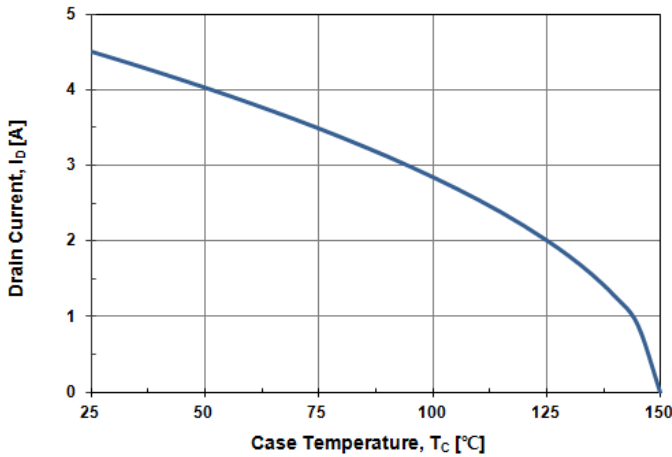


Fig. 10 Maximum Safe Operating Area

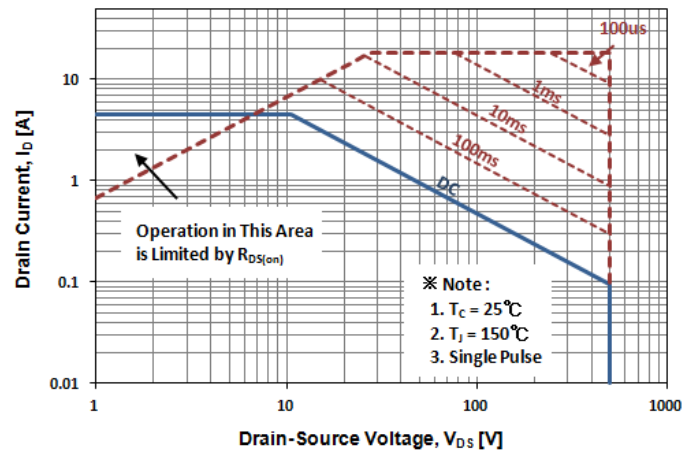


Fig. 11 Transient Thermal Impedance

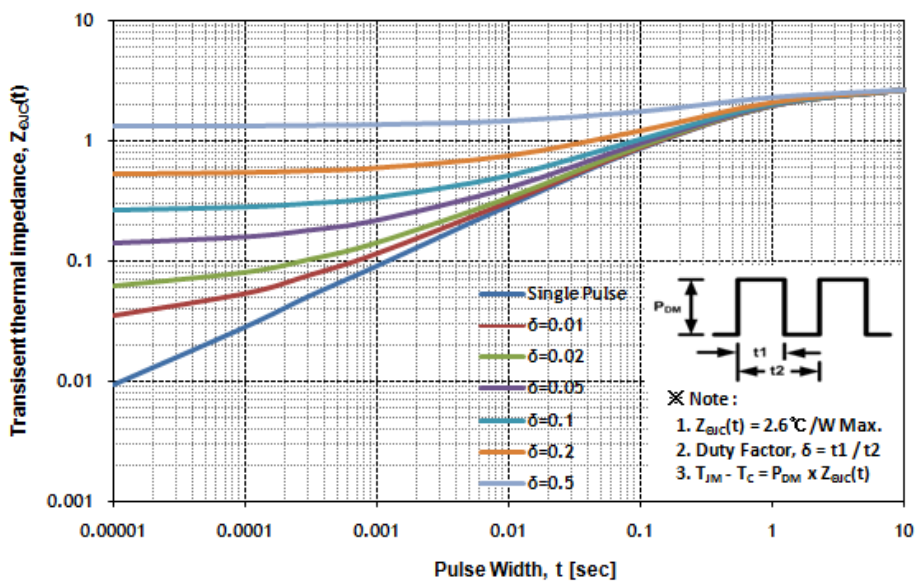


Fig. 12 Gate Charge Test Circuit & Waveform

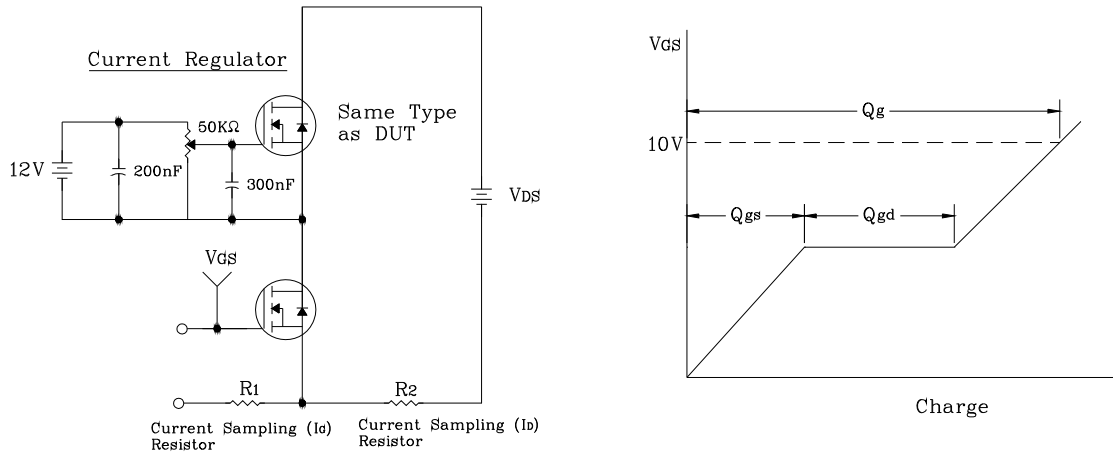


Fig. 13 Resistive Switching Test Circuit & Waveform

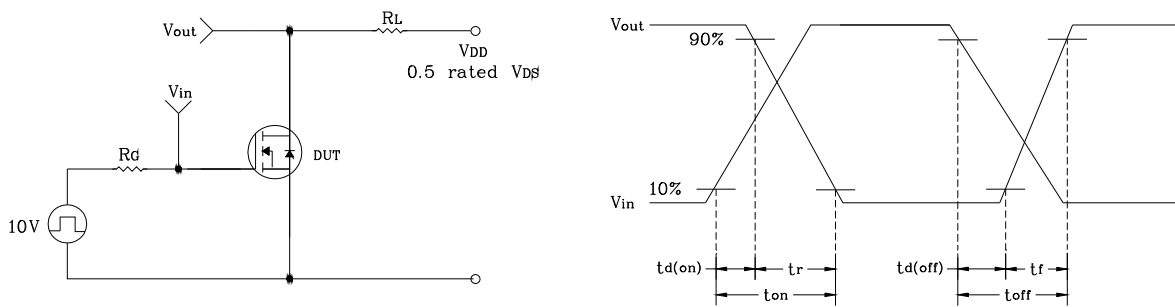
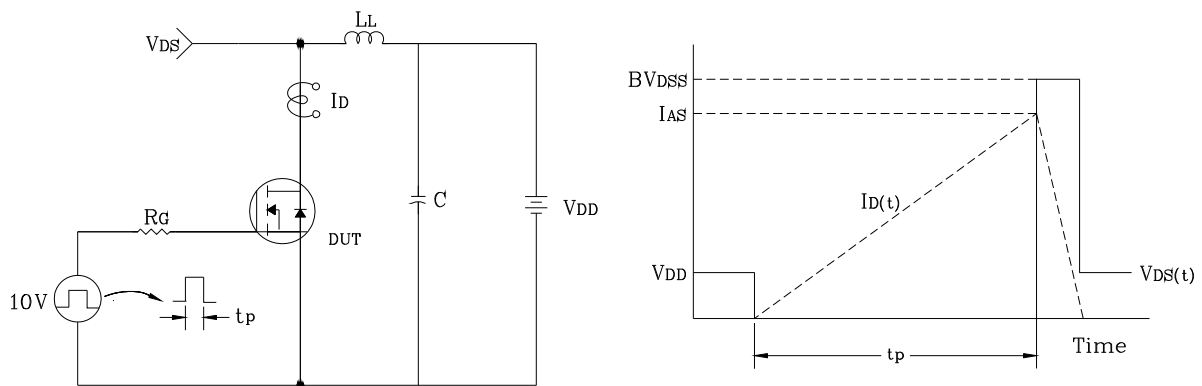


Fig. 14 E_{AS} Test Circuit & Waveform



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