MSM6912

PCM CHANNEL FILTER

GENERAL DESCRIPTION

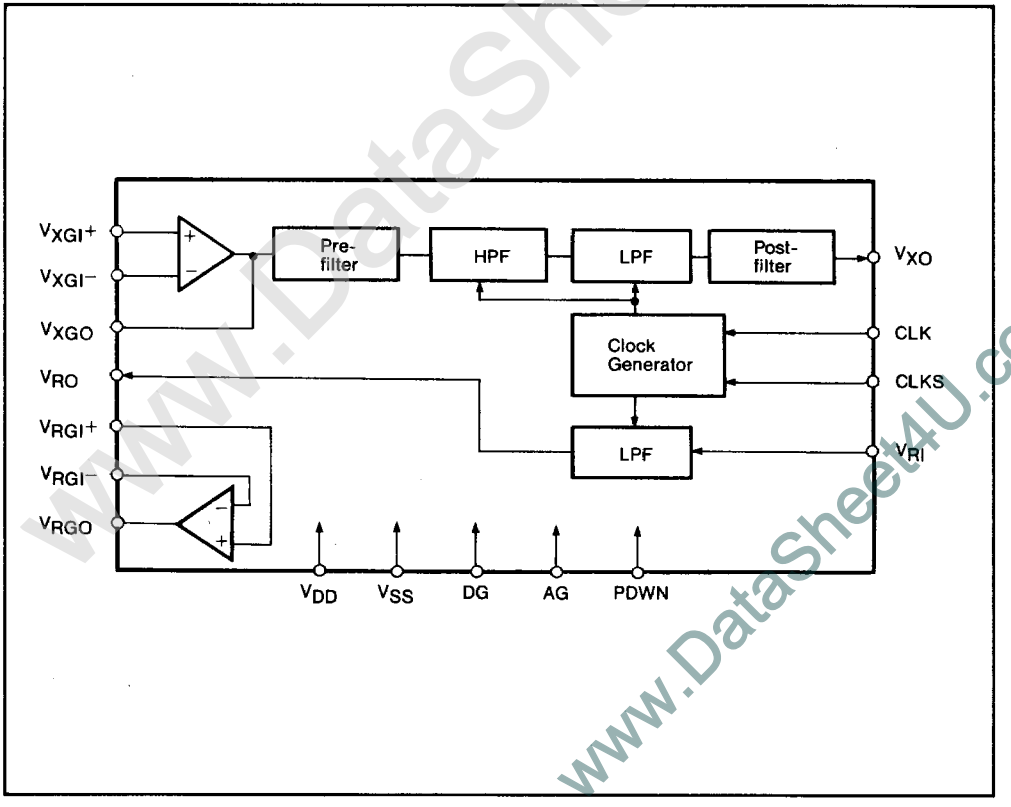
The MSM6912 is a PCM channel filter LSI which is fabricated by OKI's low power consumption CMOS silicon gate technology.

It consists of pre-filter, HPF, post filter and two LPF's.

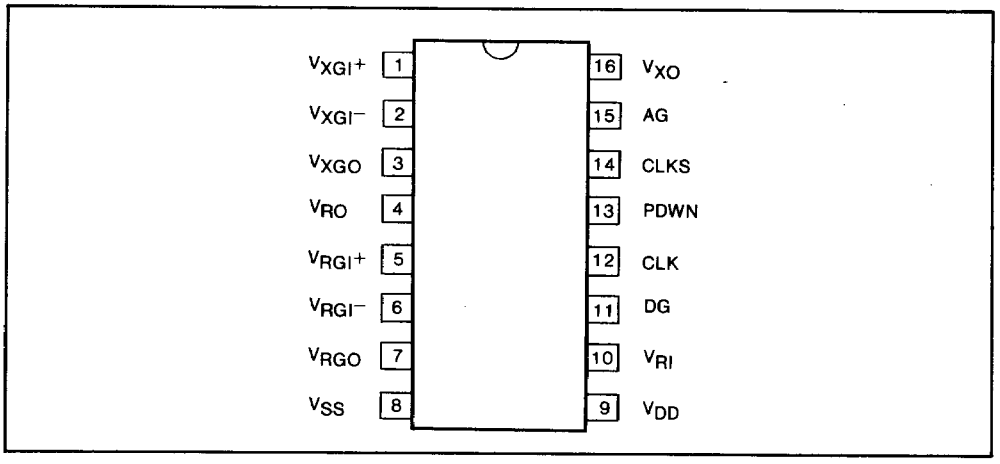
FEATURES

- CCITT G.712 standard
- 50/60 Hz rejection filter on-chip
- SIN x/x compensation filter on-chip
- External gain adjustment, both transmit and receive filters
- Power-down mode available
- 128 KHz or 2048 KHz external clock for operation
- Power supply, ±5 V
- 16-pin ceramic DIP package

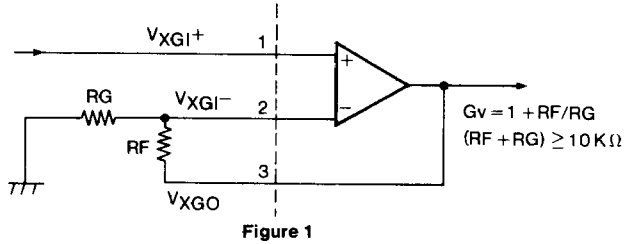
BLOCK DIAGRAM



PIN CONFIGURATION



PIN DESCRIPTION

Pin No.	Pin Name	Function
1	$V_{XGI}+$	$V_{XGI}+$ is the non-inverting input of the gain-setting Op Amp in the transmit filter section. The input analog signal is typically applied to this pin.
2	$V_{XGI}-$	$V_{XGI}-$ is the inverting input of the gain-setting Op Amp in the transmit filter section.
3	V_{XGO}	V_{XGO} is connected to the output of the gain-setting Op Amp in the transmit filter section. An appropriate voltage gain can be set as shown in Figure 1 below.  **Figure 1** As the transmit filter section has a gain of approx. +3 dB excluding this amplifier, a suitable level diagram has to be selected. The DC offset voltage of V_{XGO} becomes 50·Gv (mV) in the worst case. The load resistance connected to V_{XGO} should be greater than 10 KΩ.
4	V_{RO}	V_{RO} is the analog output of the receive filter. Because the output impedance is not so low, it is better to use the gain setting OP Amp as a output buffer. The resistive loads connected to V_{RO} should be greater than 10 KΩ.
5	$V_{RGI}+$	$V_{RGI}+$ is the non-inverting input of the gain setting Op Amp in the receive filter section.
6	$V_{RGI}-$	$V_{RGI}-$ is the inverting input of the gain setting Op Amp in the receive filter section.

Pin No.	Pin Name	Function
7	V_{RGO}	V_{RGO} is the output of the gain setting Op Amp in the receive filter section. An appropriate voltage gain can be set as shown in Figure 2 and 3.

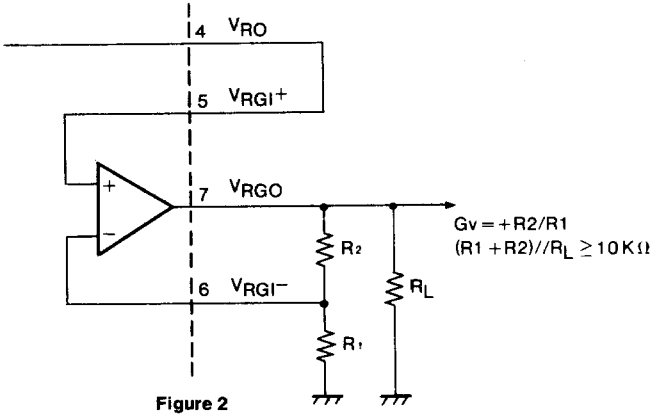


Figure 2

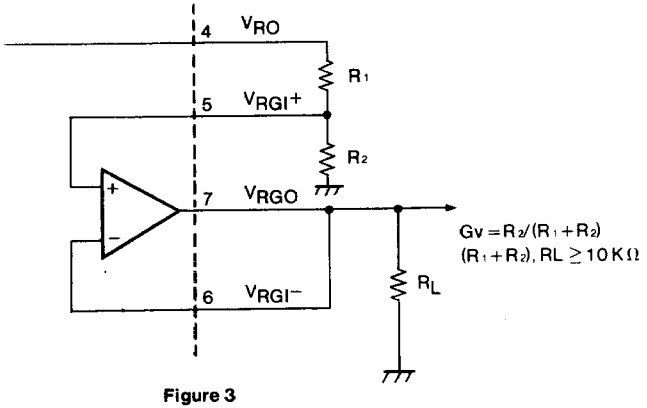


Figure 3

Use Figure 2 for amplification and Figure 3 for attenuation. As the receive filter section has a gain of approx. 0 dB excluding this amplifier, a suitable level diagram has to be calculated.
The DC offset voltage of V_{RGO} becomes as follows in the worst case;

Figure 2 ... (200 + 50) · Gv = 250 · Gv (mV)
Figure 3 ... 200 · Gv + 50 (mV)

The resistive loads connected to V_{RGO} should be greater than 10 KΩ.

<table>
<tr><th>Pin No.</th><th>Pin Name</th><th>Function</th></tr>
<tr><td>8</td><td>V_{SS}</td><td>V_{SS} is the negative supply pin. The voltage supplied to this pin should be $-5V \pm 5\%$.</td></tr>
<tr><td>9</td><td>V_{DD}</td><td>V_{DD} is the positive supply pin. The voltage supplied to this pin should be $+5V \pm 5\%$.</td></tr>
<tr><td>10</td><td>V_{RI}</td><td>V_{RI} is the analog input to the receive filter. The receive signal is typically generated by the decoder section of a companding CODEC (ex. MSM6917AS).
The receive filter provides the sin x/x correction over the passband.</td></tr>
<tr><td>11</td><td>DG</td><td>This pin is connected to the digital system ground.</td></tr>
<tr><td>12</td><td>CLK</td><td>CLK is the digital clock signal input. Two clock frequency (128 KHz, 2,048 KHz) can be applied.
The desired clock frequency is selected by the CLKS input.
For proper operation, this clock should be tied to the receive clock of the CODEC.</td></tr>
<tr><td>13</td><td>PDWN</td><td>This control input enables MSM6912AS in the powerdown mode. Power down occurs when the signal of this input is pulled high.</td></tr>
<tr><td>14</td><td>CLKS</td><td>This control pin is used to select the desired clock frequency.
<table>
<tr><th>CLK (Pin 12)</th><th>CLKS (Pin 14)</th></tr>
<tr><td>128 KHz</td><td>Digital "L"</td></tr>
<tr><td>2,048 KHz</td><td>Digital "H"</td></tr>
</table></td></tr>
<tr><td>15</td><td>AG</td><td>This pin is connected to the analog system ground.</td></tr>
<tr><td>16</td><td>V_{XO}</td><td>V_{XO} is the analog output of the transmit filter. The output voltage range is ± 2.5 V and the output DC offset voltage is less than 200 mV. This output should be AC-coupled to the encoder section of the CODEC. The resistive load connected to V_{XO} should be greater than 5 KΩ.</td></tr>
</table>

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	Ta=25°C with respect to DG and AG	−0.3 ~ 7	V
	V_{SS}		+0.3 ~ −7	
Digital input voltage	V_{DIN}		−0.3 ~ V_{DD} + 0.3	V
Analog input voltage	V_{AIN}		V_{SS}−0.3 ~ V_{DD}+0.3	V
Operating temperature	T_{OP}		0 ~ 70	°C
Storage temperature	T_{ST}		−55 ~ 150	°C

Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply voltage	V_{DD}	With respect to DG and AG	4.75	5	5.25	V
	V_{SS}		−4.75	−5	−5.25	V
Operating temperature	T_{OP}		0		70	°C

DC and Digital Interface Characteristics

(V_{DD} = +5V ± 5%, V_{SS} = −5V ± 5%, Ta = 0 ~ 70°C)

Parameter	Symbol	Conditions	Limits			Unit
			Min	Typ	Max	
Standby supply current	I_{DDS}	PDWN = V_{IH}	–	0.01	1	mA
	I_{SSS}		–	0.01	1	mA
Operating supply current	I_{DDO}	PDWN = V_{IL}	–	5	10	mA
	I_{SSO}		–	5	10	mA
Input leakage current	I_{IL}	V_I = 0V	–	–	10	μA
	I_{IH}	V_I = 5V	–	–	10	μA
Input voltage	V_{IL}	With respect to DG	–	–	0.8	V
	V_{IH}		2.4	–	–	V

Analog Interface, Gain Setting Amplifier and Transmit Filter

(V_{DD} = +5V ± 5%, V_{SS} = −5V ± 5%, Ta = 0 ~ 70°C)

	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Gain setting amplifier	Input leakage current $V_{XGI}+$ $V_{XGI}-$	I_{BX}	$-3.2V \leq V_{IN} \leq +3.2V$	–	–	10	μA
	Input resistance $V_{XGI}+$ $V_{XGI}-$	R_{IX}		2	–	–	MΩ
	Input offset voltage	V_{OSXI}	$-3.2V \leq V_{IN} \leq +3.2V$	–	–	50	mV
	DC open loop voltage gain	A_{VX}		66	–	–	dB
	Open loop unity gain bandwidth	fcx		–	2	–	MHz
	Load capacitance	C_{LX1}		–	–	200	PF
	Load resistance	R_{LX1}		10	–	–	KΩ
	Output voltage swing	V_{OX1}	RL ≥ 10KΩ	±2.5	–	–	V
Filter	Output resistance	R_{OX1}		–	–	100	Ω
	Output offset voltage	V_{OSX}	$V_{XGI}+$ = AG Input OP Amp at Unity gain	–	–	200	mV
	Load capacitance	C_{LX2}		–	–	200	PF
	Load resistance	R_{LX2}		5	–	–	KΩ
	Output voltage swing	V_{OX2}	$R_L \geq 5K\Omega$	±2.5	–	–	V

Analog Interface, Receive Filter and Gain Setting Amplifier

(V_{DD} = +5V ± 5%, V_{SS} = −5V ± 5%, Ta = 0 ~ 70°C)

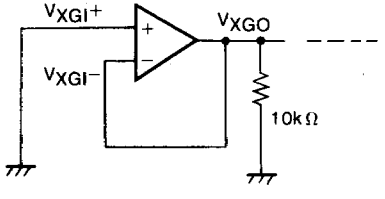
	Parameter	Symbol	Conditions	Limits			Unit
				Min	Typ	Max	
Filter	Input leakage current	I_{BR1}	$-3.2V \leq V_{IN} \leq +3.2V$	–	–	10	μA
	Input resistance	R_{IR1}		2	–	–	MΩ
	Output resistance	R_{OR1}		–	–	200	Ω
	Output offset voltage	V_{OSR}	$V_{RI} = AG$	–	–	200	mV
	Load capacitance	C_{LR1}		–	–	200	PF
	Load resistance	R_{LR1}		10	–	–	KΩ
	Output voltage swing	V_{OR1}	$R_L \geq 10K\Omega$	±2.5	–	–	V
Gain setting amplifier	Input leakage current $V_{RGI}+$, $V_{RGI}-$	I_{BR2}	$-3.2V \leq V_{IN} \leq +3.2V$	–	–	10	μA
	Input resistance $V_{RGI}+$, $V_{RGI}-$	R_{IR2}		2	–	–	MΩ
	Input offset voltage	V_{OSRI}	$-3.2V \leq V_{IN} \leq +3.2V$	–	–	50	mV
	DC open loop voltage gain	A_{VR}		66	–	–	dB
	Open loop unity gain bandwidth	f_{CR}		–	2	–	MHz
	Output resistance	R_{OR2}	At unity gain	–	–	20	Ω
	Load capacitance	C_{LR2}		–	–	200	PF
	Load resistance	R_{LR2}		10	–	–	KΩ
	Output voltage swing	V_{OR2}	$RL \geq 10K\Omega$	±2.5	–	–	V

Transmit Filter Transfer Characteristics

(V_{DD} = +5V ± 5%, V_{SS} = −5V ± 5%, Ta = 0 ~ 70°C)

Parameter		Symbol	Conditions	Limits				Unit
				Amp	Min	Typ	Max	
Absolute passband gain (900 Hz)		G_{AX}	Input = 0 dBmo ≅1.25 Vrms Output = +3 dBmo ≅1.77 Vrms	0 dB	2.8	3.0	3.2	dB
Relative gain (to GAX)	Below 60 Hz	G_{RX}			–	−20		
	300~3000 Hz				−0.25	–	+0.1	
	3300 Hz				−0.35	–	+0.1	
	3400 Hz				−0.85	–	+0.1	
	4000 Hz				–	–	−14	
	4600 Hz and above				–	–	−28	
Gain variation with temperature		G_{AXT}	Input = 0 dBmo 900 Hz		–	0.0005	–	dB/°C
Gain variation with supplies		G_{AXS}	Input = 0 dBmo 900 Hz Supplies: ±5%		–	0.05	–	dB/V
Crosstalk, Receive to Transmit		CT_{RX}	*1		–	–	−60	dB
Total C message noise at output		N_{CX1}			–	8	–	dBrnco
Total C message noise at output		N_{CX2}		20 dB	–	10	–	
Differential envelope delay		D_{DX}	0.9 ~ 2.6 KHz	0 dB	–	–	60	μS
Absolute delay		D_{AX}	900 Hz		–	200	–	
Single frequency distortion products		D_{PX}	V_{XO} = +3 dBmo 900 Hz	20 dB	–	–	−45	dB
Positive power supply rejection ratio		P_{SRR1}	V_{XO}, 900 Hz V_{DD}	0 dB	25	30	–	
Negative power supply rejection ratio		P_{SRR2}	V_{XO}, 900 Hz V_{SS}		23	28	–	

*1 V_{RI} = 0 dBmo, 900 Hz



Receive Filter Transfer Characteristics

(V_{DD} = +5V ± 5%, V_{SS} = −5V ± 5%, Ta = 0 ~ 70°C)

Parameter		Symbol	Conditions	Limits				Unit
				Amp	Min	Typ	Max	
Absolute passband gain (900 Hz)		G_{AR}	Input = 0 dBmo = 1.25 Vrms	0 dB	−0.25	−0.1	0	dB
Relative gain (to GAR)	Below 300 Hz	G_{RR}	Output = +3 dBmo = 1.77 Vrms With sin x/x correction where x = πf/8000		−0.25	–	+0.1	
	300~3000 Hz				−0.25	–	+0.1	
	3300 Hz				−0.35	–	+0.1	
	3400 Hz				−0.85	–	+0.1	
	4000 Hz				–	–	−14	
	4600 Hz and above				–	–	−28	
Gain variation with temperature		G_{ART}	Input = 0 dBmo 900 Hz		–	0.0005	–	dB/°C
Gain variation with supplies		G_{AXS}	Input = 0 dBmo 900 Hz Supplies: ±5%		–	0.05	–	dB/V
Crosstalk, transmit to receive		CT_{XR}	*1		–	–	−60	dB
Total C message noise at output		N_{CR}			–	7	–	dBrnco
Differential envelope delay		D_{DR}	0.9 ~ 2.6 KHz		–	–	120	μs
Absolute delay		D_{AR}	900 Hz		–	120	–	
Single frequency distortion products		D_{PR}	V_{RGO} = +3 dBmo 900 Hz *2		–	–	−50	dB
Positive power supply rejection ratio		P_{SRR3}	V_{RGO}, 900 Hz V_{DD}		30	35	–	
Negative power supply rejection ratio		P_{SRR4}	V_{RGO}, 900 Hz V_{SS}		30	35	–	

*1 V_{XO} = +3 dBmo, 900 Hz
V_{RI} = AG

*2 Removing the component of 128 KHz