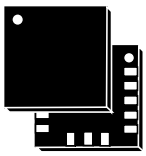
LIS3DE

MEMS digital output motion sensor: ultra-low-power high-performance 3-axis "nano" accelerometer

Datasheet - production data



LGA-16 (3x3x1 mm)

Features

- Wide supply voltage, 1.71 V to 3.6 V
- Independent IO supply (1.8 V) and supply voltage compatible
- Ultra-low-power mode consumption down to 2 µA
- ±2*g*/±4*g*/±8*g*/±16*g* dynamically selectable full scales
- I^2C/SPI digital output interface
- 8-bit data output
- 2 independent programmable interrupt generators for free-fall and motion detection
- 6D/4D orientation detection
- “Sleep-to-wake” and “Return-to-sleep” functions
- Free-fall detection
- Motion detection
- Embedded temperature sensor
- Embedded self-test
- Embedded FIFO
- 10000 *g* high shock survivability
- ECOPACK®, RoHS and “Green” compliant

Applications

- Motion-activated functions
- Free-fall detection
- Click/double-click recognition
- Intelligent power saving for handheld devices
- Pedometers
- Display orientation
- Gaming and virtual reality input devices
- Impact recognition and logging
- Vibration monitoring and compensation

Description

The LIS3DE is an ultra-low-power high-performance 3-axis linear accelerometer belonging to the “nano” family, with digital I^2C/SPI serial interface standard output. The device features ultra-low-power operational modes that allow advanced power saving and smart embedded functions.

The LIS3DE has dynamically user-selectable full scales of ±2*g*/±4*g*/±8*g*/±16*g* and is capable of measuring accelerations with output data rates from 1 Hz to 5 kHz. The self-test capability allows the user to check the functioning of the sensor in the final application. The device may be configured to generate interrupt signals by two independent inertial wakeup/free-fall events as well as by the position of the device itself. Thresholds and the timing of interrupt generators are programmable by the end user on the fly. The LIS3DE has an integrated 32-level first-in, first-out (FIFO) buffer allowing the user to store data in order to limit intervention by the host processor. The LIS3DE is available in a small thin plastic land grid array package (LGA) and it is guaranteed to operate over an extended temperature range from -40 °C to +85 °C.

Table 1. Device summary

Order codes	Temp. range [°C]	Package	Packaging
LIS3DE	-40 to +85	LGA-16	Tray
LIS3DETR	-40 to +85	LGA-16	Tape and reel

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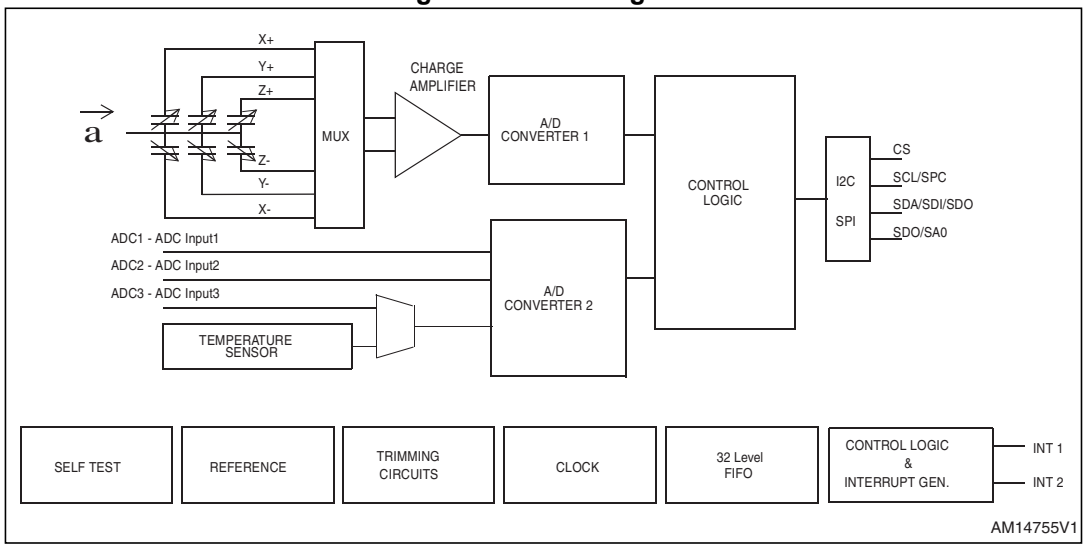
1.1 Block diagram

Figure 1. Block diagram



1.2 Pin description

Figure 2. Pin connections

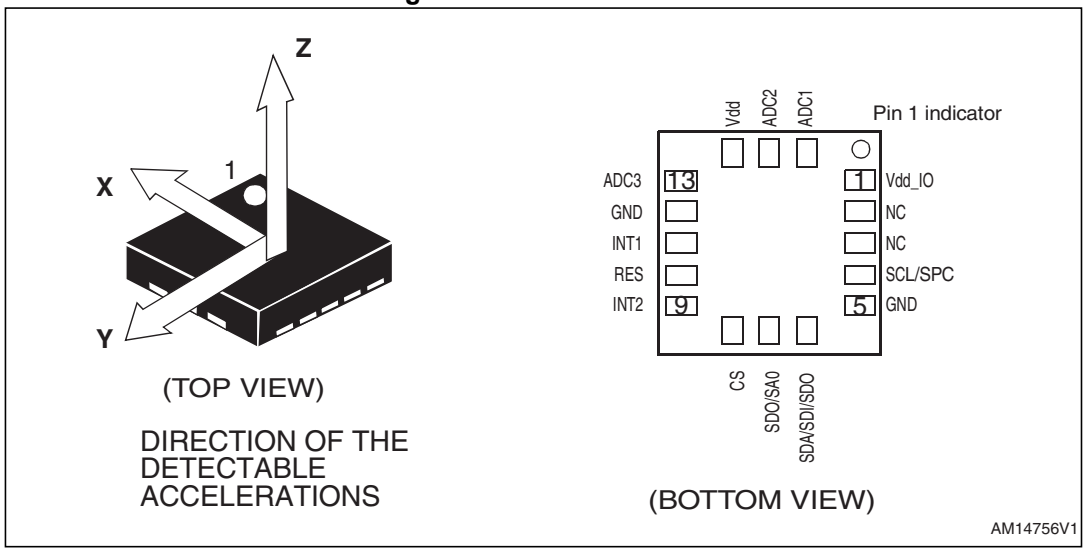


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO	Power supply for I/O pins
2	NC	Not connected
3	NC	Not connected
4	SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
5	GND	0 V supply
6	SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
7	SDO SA0	SPI serial data output (SDO) I^2C least significant bit of the device address (SA0)
8	CS	SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
9	INT2	Interrupt 2
10	RES	Connect to GND
11	INT1	Interrupt 1
12	GND	0 V supply
13	ADC3	Analog-to-digital converter input 3
14	Vdd	Power supply
15	ADC2	Analog-to-digital converter input 2
16	ADC1	Analog-to-digital converter input 1

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

Vdd = 2.5 V, T = 25 °C unless otherwise noted[a].

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.[1]	Max.	Unit
FS	Measurement range[2]	FS bit set to 00		±2.0		*g*
		FS bit set to 01		±4.0		
		FS bit set to 10		±8.0		
		FS bit set to 11		±16.0		
So	Sensitivity	FS bit set to 00		15.6		mg/digit
		FS bit set to 01		31.2		mg/digit
		FS bit set to 10		62.5		mg/digit
		FS bit set to 11		187.5		mg/digit
TCSo	Sensitivity change vs. temperature	FS bit set to 00		±0.05		%/°C
TyOff	Typical zero-*g* level offset accuracy[3][4]	FS bit set to 00		±100		m*g*
TCOff	Zero-*g* level change vs. temperature	Max. delta from 25 °C		±0.8		m*g*/°C
Vst	Self-test output change[5][6][7]	FS bit set to 00 X-axis	50		1800	m*g*
		FS bit set to 00 Y-axis	50		1800	m*g*
		FS bit set to 00 Z-axis	50		1800	m*g*
T_{op}	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical zero-*g* level offset value after MSL3 preconditioning.
4. Offset can be eliminated by enabling the built-in high-pass filter.
5. The sign of the “self-test output change” is defined by CTRL_REG4 ST sign bits, for all axes.
6. The “self-test output change” is defined as the absolute value of: $OUTPUT[LSB]_{(CTRL\_REG4\ ST1,\ ST0\ bits=01)} - OUTPUT[LSB]_{(CTRL\_REG4\ ST1,\ ST0\ bits=00)}$
7. Output data reaches 99% of final value after 1ms+1/ODR when enabling the self-test mode, due to device filtering.

a. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.

2.2 Temperature sensor characteristics

Vdd = 2.5 V, T = 25 °C unless otherwise noted [b].

Table 4. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
TSDr	Temperature sensor output change vs. temperature			1		digit/°C(2)
TODR	Temperature refresh rate			ODR		Hz
T_{op}	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed. Temperature sensor operation is guaranteed in the range 2 V - 3.6 V.
2. 8-bit resolution.

2.3 Electrical characteristics

Vdd = 2.5 V, T = 25 °C unless otherwise noted [c].

Table 5. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		1.71	2.5	3.6	V
Vdd_IO	I/O pins supply voltage(2)		1.71		Vdd+0.1	V
Idd	Current consumption in normal mode	50 Hz ODR		11		µA
Idd	Current consumption in normal mode	1 Hz ODR		2		µA
IddLP	Current consumption in low-power mode	50 Hz ODR		6		µA
IddPdn	Current consumption in power-down mode			0.5		µA
VIH	Digital high-level input voltage		0.8*Vdd_IO			V
VIL	Digital low-level input voltage				0.2*Vdd_IO	V
VOH	High-level output voltage		0.9*Vdd_IO			V
VOL	Low-level output voltage				0.1*Vdd_IO	V
BW	System bandwidth(3)			ODR/2		Hz
T_{op}	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. It is possible to remove Vdd while maintaining Vdd_IO without blocking the communication busses. In this condition the measurement chain is powered off.
3. Refer to *Table 26* for the ODR value and configuration.

b. The product is factory calibrated at 2.5 V.

c. The product is factory calibrated at 2.5 V. The operational power supply range is from 1.71 V to 3.6 V.

2.4 Communication interface characteristics

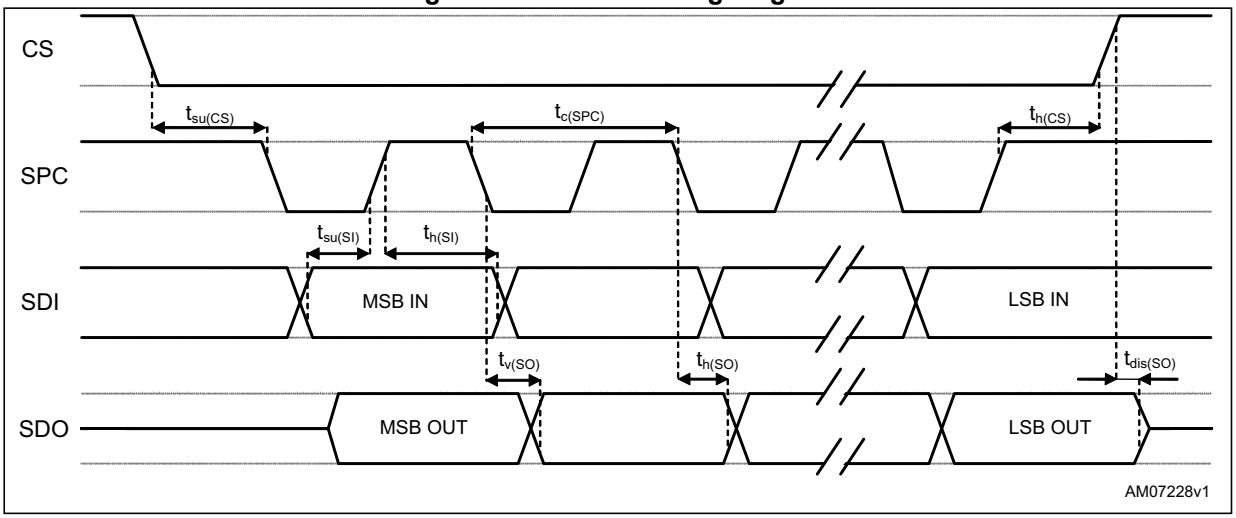
2.4.1 SPI - serial peripheral interface

Subject to general operating conditions for Vdd and T_{op}.

Table 6. SPI slave timing values

Symbol	Parameter	Value (1)		Unit
		Min.	Max.	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

Figure 3. SPI slave timing diagram



Note: Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both the input and output ports.

2.4.2 I²C - inter-IC control interface

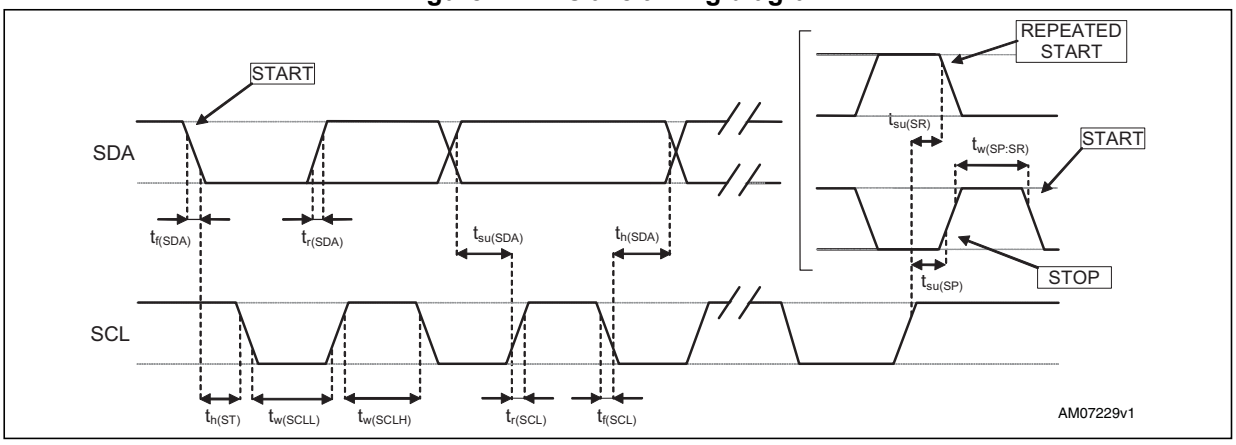
Subject to general operating conditions for Vdd and T_{op}.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0.01	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ (2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.
2. C_b = total capacitance of one bus line, in pF.

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (CS, SCL/SPC, SDA/SDI/SDO, SDO/SA0)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 2.5 V)	3000 for 0.5 ms	g
		10000 for 0.1 ms	g
A_{UNP}	Acceleration (any axis, unpowered)	3000 for 0.5 ms	g
		10000 for 0.1 ms	g
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

Note: Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Terminology and functionality

3.1 Terminology

3.1.1 Sensitivity

Sensitivity describes the gain of the sensor and can be determined, for example, by applying 1 *g* acceleration to it. As the sensor can measure DC accelerations, this can be done easily by pointing the axis of interest towards the center of the Earth, noting the output value, rotating the sensor by 180 degrees (pointing to the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and also time. The sensitivity tolerance describes the range of sensitivities of a large population of sensors.

3.1.2 Zero-*g* level

Zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady-state on a horizontal surface measures 0 *g* on the X-axis and 0 *g* on the Y-axis whereas the Z-axis measures 1 *g*. The output is ideally in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called Zero-*g* offset. Offset is, to some extent, a result of stress to the MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Zero-*g* level change vs. temperature". The Zero-*g* level tolerance (TyOff) describes the standard deviation of the range of Zero-*g* levels of a population of sensors.

3.2 Functionality

3.2.1 Normal mode, low-power mode

The LIS3DE provides two different operating modes: *normal mode* and *low-power mode*. *Table 9* summarizes how to select the operating mode.

Table 9. Operating mode selection

CTRL_REG1 [3] (LPen bit)	Operating mode
1	Low-power mode
0	Normal mode

3.2.2 Self-test

The self-test allows the sensor functionality to be checked without moving it. The self-test function is off when the self-test bit (ST) is programmed to '0'. When the self-test bit is programmed to '1', an actuation force is applied to the sensor, simulating a definite input acceleration. In this case the sensor outputs exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity.

When the self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

3.2.3 6D / 4D orientation detection

The LIS3DE includes 6D / 4D orientation detection.

6D / 4D orientation recognition: In this configuration the interrupt is generated when the device is stable in a known direction. In 4D configuration Z-axis position detection is disabled.

3.2.4 Sleep-to-wake and return-to-sleep functions

The LIS3DE can be programmed to automatically switch to low-power mode upon recognition of a determined event. Once the event condition is over, the device returns to the preset normal mode.

To enable this function, the desired threshold value must be stored in the *Act_THS (3Eh)* registers, while the duration value must be written in the *Act_DUR (3Fh)* register.

When the acceleration, which is internally high-pass filtered, becomes lower than the threshold value on all of the three axes, the device automatically switches to low-power mode (10 Hz ODR).

During this condition, the ODRx bits and LPen bit inside *CTRL_REG1 (20h)* are not considered.

Once the acceleration rises above the threshold (at least on one axis), the system restores the operating mode and ODRs as per the *CTRL_REG1 (20h)* and *CTRL_REG4 (23h)* settings.

3.3 Sensing element

A proprietary process is used to create a surface micro-machined accelerometer. The technology allows processing suspended silicon structures which are attached to the substrate in a few points called anchors and are free to move in the direction of the sensed acceleration. To be compatible with the traditional packaging techniques, a cap is placed on top of the sensing element to avoid the moving parts from being blocked during the molding phase of the plastic encapsulation.

When an acceleration is applied to the sensor the proof mass displaces from its nominal position, causing an imbalance in the capacitive half bridge. This imbalance is measured using charge integration in response to a voltage pulse applied to the capacitor.

At steady-state the nominal value of the capacitors are a few pF and when an acceleration is applied, the maximum variation of the capacitive load is in the fF range.

3.4 IC interface

The complete measurement chain is made up of a low-noise capacitive amplifier which converts the capacitive unbalancing of the MEMS sensor into an analog voltage using an analog-to-digital converter.

The acceleration data may be accessed through an I^2C/SPI interface, therefore making the device particularly suitable for direct interfacing with a microcontroller.

The LIS3DE features a data-ready signal (DRDY) which indicates when a new set of measured acceleration data is available, therefore simplifying data synchronization in the digital system that uses the device.

The LIS3DE may also be configured to generate an inertial wakeup and free-fall interrupt signal according to a programmed acceleration event along the enabled axes. Both free-fall and wakeup can be available simultaneously on two different pins.

3.5 Factory calibration

The IC interface is factory calibrated for sensitivity (So) and Zero-*g* level (TyOff).

The trimming values are stored inside the device in non-volatile memory. Any time the device is turned on, the trimming parameters are downloaded into the registers to be used during the active operation. This allows the device to be used without further calibration.

3.6 FIFO

The LIS3DE contains a 32-level FIFO for each of the three output channels, X, Y and Z. Buffered output allows 4 operation modes: FIFO, Stream, Stream-to-FIFO and Bypass. Where FIFO Bypass mode is activated FIFO is not operating and remains empty. In FIFO mode, data from acceleration detection on the X-, Y-, and Z-axis measurements are stored in FIFO.

3.7 Auxiliary ADC

The LIS3DE contains an auxiliary 10-bit ADC with 3 separate dedicated inputs.

3.8 Temperature sensor

The LIS3DE is equipped with an internal temperature sensor. Temperature data can be enabled by setting the TEMP_EN bit of the *TEMP_CFG_REG (1Fh)* register to “1”.

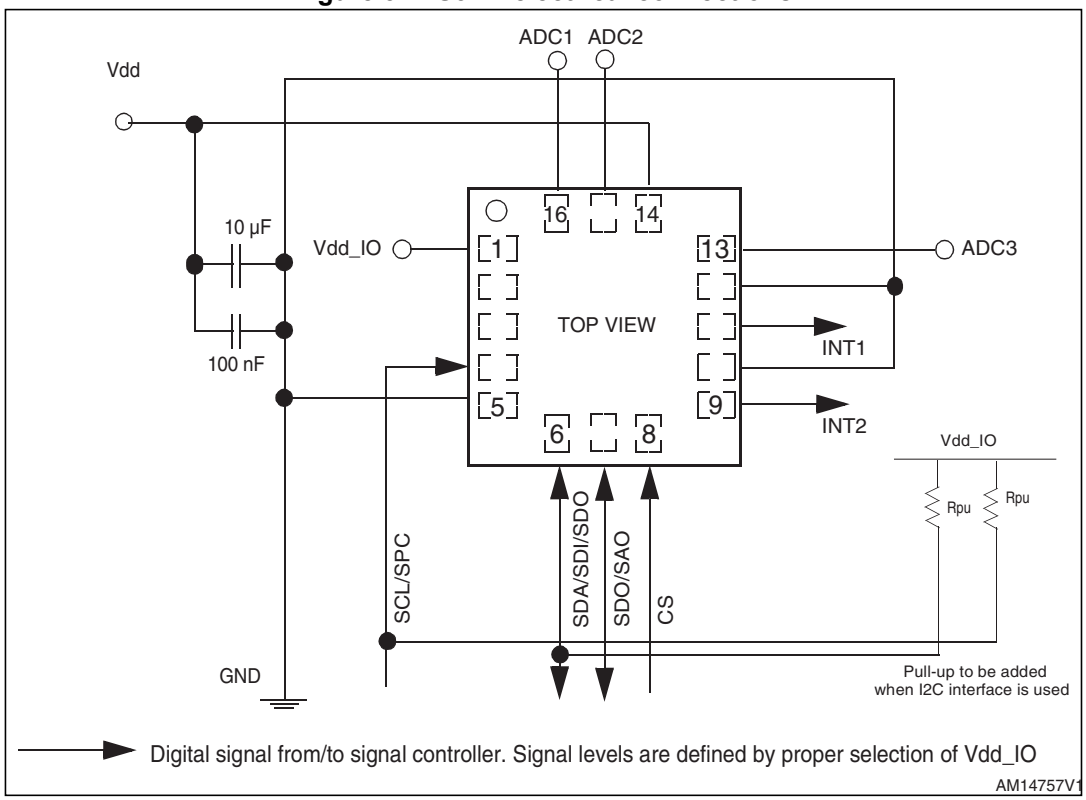
When the auxiliary ADC and temperature sensor are enabled, the third channel of the ADC is used to digitize the temperature sensor output.

To retrieve the temperature sensor data, the BDU bit on *CTRL_REG4 (23h)* must be set to “1”. Both the OUT_ADC3_H and OUT_ADC3_L registers must be read.

Temperature data is stored inside OUT_ADC3_H as two’s complement data, in 8-bit format, left-justified.

4 Application hints

Figure 5. LIS3DE electrical connections



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (100 nF ceramic, 10 µF aluminum) should be placed as near as possible to pin 14 of the device (common design practice).

All the voltage and ground supplies must be present at the same time to have proper behavior of the IC (refer to *Figure 5*). It is possible to remove Vdd maintaining Vdd_IO without blocking the communication bus, in this condition the measurement chain is powered off.

The functionality of the device and the measured acceleration data is selectable and accessible through the I^2C or SPI interfaces. When using the I^2C, CS must be tied high.

ADC1, ADC2 and ADC3, if not used, can be left floating or kept connected to Vdd or GND.

The functions, the threshold and the timing of the two interrupt pins (INT1 and INT2) can be completely programmed by the user through the I^2C/SPI interface.

4.1 Soldering information

The LGA package is compliant with the ECOPACK®, RoHS and “Green” standards.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com.

5 Digital main blocks

5.1 FIFO

The LIS3DE embeds a 32-level data FIFO for each of the three output channels, X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

In order to enable the FIFO buffer, the FIFO_EN bit in *CTRL_REG5 (24h)* must be set to ‘1’.

This buffer can work according to four different modes: Bypass mode, FIFO mode, Stream mode and Stream-to-FIFO mode. Each mode is selected by the FM [1:0] bits in *FIFO_CTRL_REG (2Eh)*. Programmable FIFO watermark level, FIFO empty or FIFO overrun events can be enabled to generate dedicated interrupts on the INT1 pin (configuration through *CTRL_REG3 (22h)*).

FIFO_SRC_REG (EMPTY) is equal to ‘1’ when all FIFO samples are ready and FIFO is empty.

FIFO_SRC_REG (WTM) goes to ‘1’ if a new data is written in the buffer and FIFO_SRC_REG (FSS [4:0]) is greater than or equal to FIFO_CTRL_REG (FTH [4:0]). FIFO_SRC_REG (WTM) goes to ‘0’ if reading X, Y, Z data slot from FIFO and FIFO_SRC_REG (FSS [4:0]) is less than or equal to FIFO_CTRL_REG (FTH [4:0]). FIFO_SRC_REG (OVRN_FIFO) is equal to ‘1’ if a FIFO slot is overwritten.

5.1.1 Bypass mode

In Bypass mode the FIFO is not operational and for this reason it remains empty. For each channel only the first address is used. The remaining FIFO levels are empty.

Bypass mode must be used in order to reset the FIFO buffer when a different mode is operating (i.e. FIFO mode).

5.1.2 FIFO mode

In FIFO mode, the buffer continues filling data from the X, Y and Z accelerometer channels until it is full (32 samples set stored). When the FIFO is full, it stops collecting data from the input channels and the FIFO content remains unchanged.

An overrun interrupt can be enabled, INT1_OVERRUN = '1' in the *CTRL_REG3 (22h)* register, in order to be raised when the FIFO stops collecting data. When overrun interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input channels.

At the end of the reading procedure it is necessary to exit Bypass mode in order to reset the FIFO content. After this reset command, it is possible to restart FIFO mode just by selecting the FIFO mode configuration (FM bits) in register *FIFO_CTRL_REG (2Eh)*.

5.1.3 Stream mode

In Stream mode the FIFO continues filling data from X, Y, and Z accelerometer channels, when the buffer is full (32 samples set stored) the FIFO buffer index restarts from the beginning and older data is replaced by the current. The oldest values continue to be overwritten until a read operation frees FIFO slots.

An overrun interrupt can be enabled, INT1_OVERRUN = '1' in the *CTRL_REG3 (22h)* register, in order to read the entire FIFO content at once. If, in the application, it is mandatory not to lose data and it is not possible to read at least one sample for each axis within one ODR period, a watermark interrupt can be enabled in order to read partially the FIFO and leave memory slots free for incoming data.

Setting the FTH [4:0] bit in the *FIFO_CTRL_REG (2Eh)* register to value N, the number of X, Y and Z data samples that should be read at the watermark interrupt rising is up to (N+1).

5.1.4 Stream-to-FIFO mode

In Stream-to-FIFO mode, data from the X, Y and Z accelerometer channels are collected in a combination of Stream mode and FIFO mode; the FIFO buffer starts operating in Stream mode and switches to FIFO mode when the selected interrupt occurs.

The FIFO operating mode changes according to the INT1 pin value if the TR bit is set to ‘0’ in the *FIFO_CTRL_REG (2Eh)* register or the INT2 pin value if the TR bit is set to ‘1’ in the *FIFO_CTRL_REG (2Eh)* register.

When the interrupt pin is selected and the interrupt event is configured on the related pin, the FIFO operates in Stream mode if the pin value is equal to ‘0’ and it operates in FIFO mode if the pin value is equal to ‘1’. The switch mode is dynamically performed according to the pin value.

Stream-to-FIFO can be used in order to analyze the sample history that generated an interrupt; the standard operation is to read FIFO content when FIFO mode is triggered and the FIFO buffer is full and stopped.

5.1.5 Retrieving data from FIFO

FIFO reads must start from register 28h.

FIFO X, Y and Z data are read from *OUT_X (29h)*, *OUT_Y (2Bh)* and *OUT_Z (2Dh)*. When the FIFO is in Stream, Stream-to-FIFO or FIFO mode, a read operation to the *OUT_X (29h)*, *OUT_Y (2Bh)* and *OUT_Z (2Dh)* registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed in the *OUT_X (29h)*, *OUT_Y (2Bh)* and *OUT_Z (2Dh)* registers and both single read and read_burst[(d)] operations can be used.

d. The read address is automatically updated by the device and rolls back to 0x28 when register 0x2D is reached. In order to read all FIFO levels in a multiple bytes read, 196 bytes (6 output registers by 32 levels) must be read. FIFO reads must start from register 0x28 for output update and 0x2D for FIFO pointer update.

6 Digital interfaces

The registers embedded inside the LIS3DE may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pads. To select/exploit the I^2C interface, the CS line must be tied high (i.e. connected to Vdd_IO).

Table 10. Serial interface pin description

Pin name	Pin description
CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
SCL SPC	I^2C serial clock (SCL) SPI serial port clock (SPC)
SDA SDI SDO	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
SA0 SDO	I^2C least significant bit of the device address (SA0) SPI serial data output (SDO)

6.1 I^2C serial interface

The LIS3DE I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 11. Serial interface pin description

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus; the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both lines must be connected to Vdd_IO through an external pull-up resistor. When the bus is free, both lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with normal mode.

6.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH-to-LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the master, the bus is considered busy. The next byte of data transmitted after the START condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a START condition with its address. If they match, the device considers itself addressed by the master.

The slave address (SAD) associated to the LIS3DE is 010100xb. The **SDO**/**SA0** pad can be used to modify the least significant bit of the device address. If the SA0 pad is connected to a voltage supply, LSB is '1' (address 0101001b) or, if the SA0 pad is connected to ground, the LSB value is '0' (address 0101000b). This solution permits two different accelerometers to be connected and addressed to the same I²C lines.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the LIS3DE behaves like a slave device and the following protocol must be adhered to. After the START condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, an 8-bit sub-address (SUB) is transmitted: the 7 LSB represent the actual register address while the MSB enables address auto increment. If the MSB of the SUB field is '1', the SUB (register address) is automatically increased to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit is '1' (read), a repeated START (SR) condition must be issued after the two sub-address bytes; if the bit is '0' (write), the master transmits to the slave with direction unchanged. *Table 12* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 12. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SA0	R/W	SAD+R/W
Read	010100	0	1	01010001 (51h)
Write	010100	0	0	01010000 (50h)
Read	010100	1	1	01010011 (53h)
Write	010100	1	0	01010010 (52h)

Table 13. Transfer when master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 14. Transfer when master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 15. Transfer when master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 16. Transfer when master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the most significant bit (MSB) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real-time function) the data line must be left HIGH by the slave. The master can then abort the transfer. A LOW-to-HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of the first register to be read.

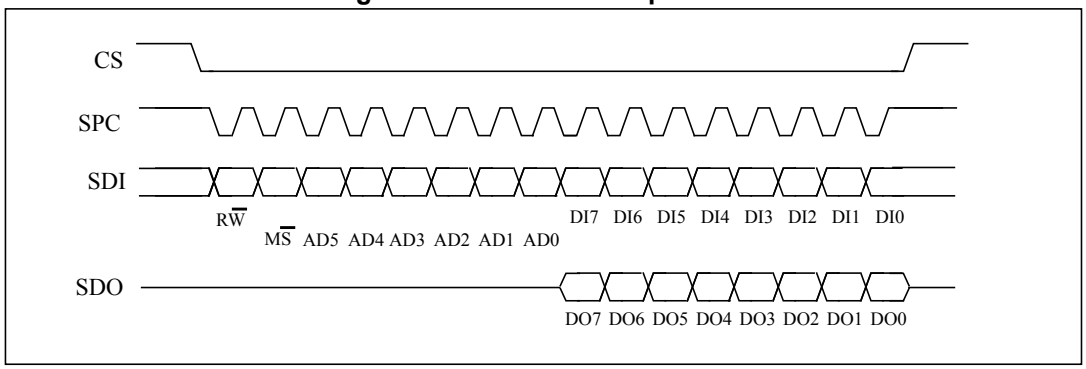
In the presented communication format, MAK is master acknowledge and NMAK is no master acknowledge.

6.2 SPI bus interface

The LIS3DE SPI is a bus slave. The SPI allows reading from and writing to the registers of the device.

The serial interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 6. Read and write protocol



CS is the serial port enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the serial port clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the serial port data input and output. These lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the read register and write register commands are completed in 16 clock pulses or in multiples of 8 in the case of multiple read/write bytes. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23,...) starts at the last falling edge of SPC just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip drives **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address remains unchanged in multiple read/write commands. When 1, the address is auto incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (Write mode). This is the data that is written into the device (MSB first).

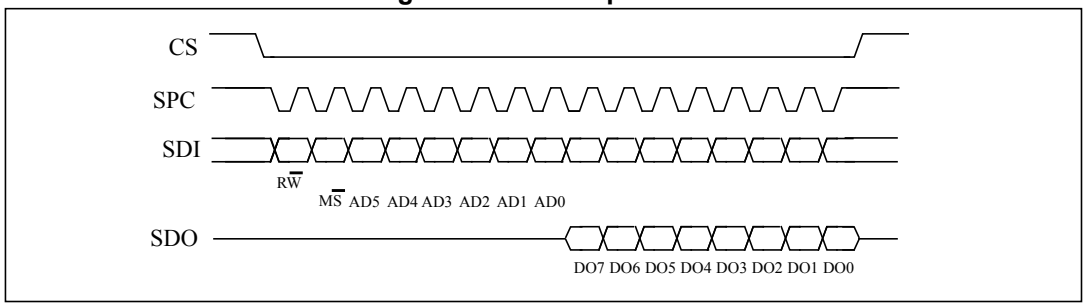
bit 8-15: data DO(7:0) (Read mode). This is the data that is read from the device (MSB first).

In multiple read/write commands further blocks of 8 clock periods are added. When the M$\overline{S}$ bit is '0', the address used to read/write data remains the same for every block. When the M$\overline{S}$ bit is '1', the address used to read/write data is increased at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

6.2.1 SPI read

Figure 7. SPI read protocol



The SPI read command is performed with 16 clock pulses. Multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: READ bit. The value is 1.

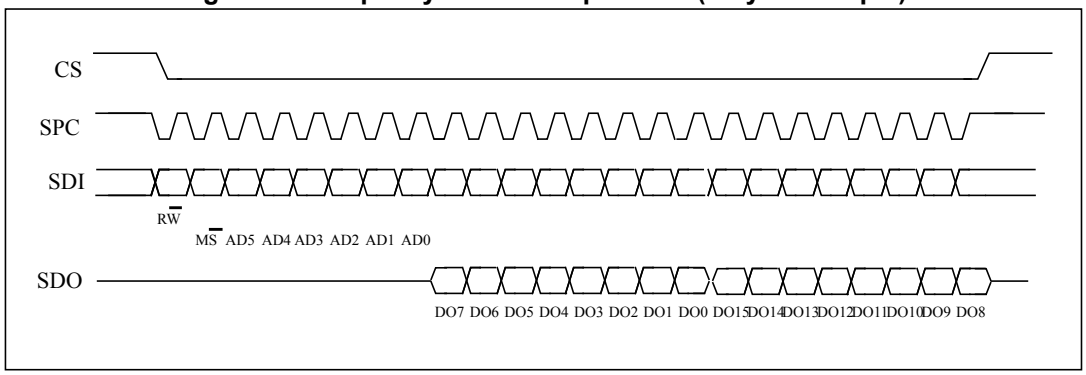
bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (Read mode). This is the data that is read from the device (MSB first).

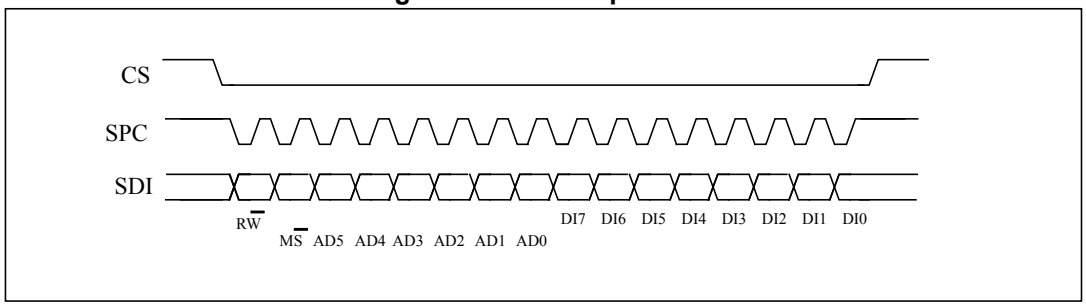
bit 16-...: data DO(...-8). Further data in a multiple byte read.

Figure 8. Multiple byte SPI read protocol (2-byte example)



6.2.2 SPI write

Figure 9. SPI write protocol



The SPI write command is performed with 16 clock pulses. The multiple byte write command is performed by adding blocks of 8 clock pulses to the previous one.

bit 0: WRITE bit. The value is 0.

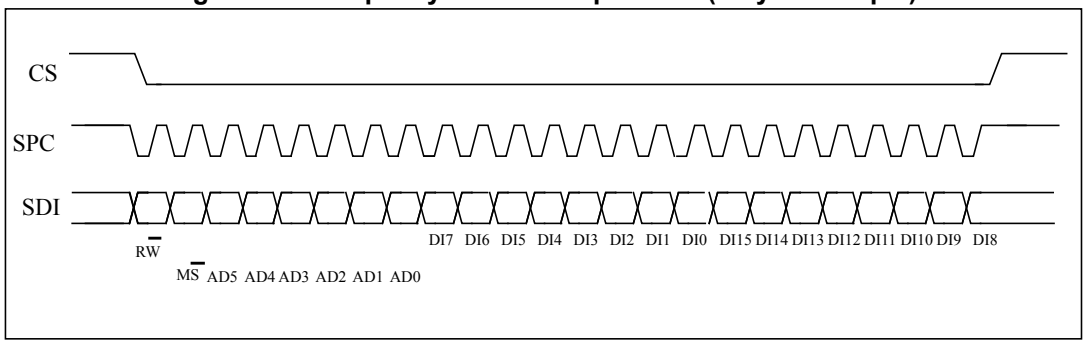
bit 1: MS bit. When 0, does not increment the address; when 1, increments the address in multiple writes.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (Write mode). This is the data that is written inside the device (MSB first).

bit 16-...: data DI(...-8). Further data in multiple byte writes.

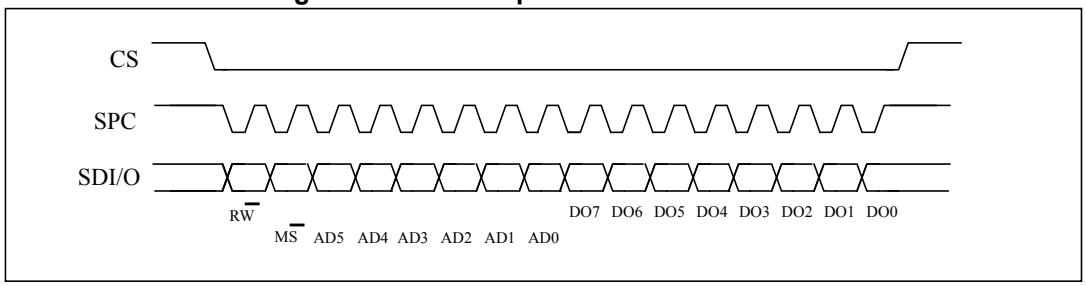
Figure 10. Multiple byte SPI write protocol (2-byte example)



6.2.3 SPI read in 3-wire mode

3-wire mode is entered by setting the SIM (SPI serial interface mode selection) bit to '1' in CTRL_REG4.

Figure 11. SPI read protocol in 3-wire mode



The SPI read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: $M\overline{S}$ bit. When 0, does not increment the address; when 1, increments the address in multiple reads.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (Read mode). This is the data that is read from the device (MSB first).

The multiple read command is also available in 3-wire mode.

7 Register mapping

Table 17 provides a list of the 8-bit registers embedded in the device and the corresponding addresses.

Table 17. Register address map

Name	Type	Register address		Default	Comment
		Hex	Binary		
Reserved (do not modify)		00 - 06			Reserved
STATUS_REG_AUX	r	07	000 0111		
OUT_ADC1_L	r	08	000 1000	Output	
OUT_ADC1_H	r	09	000 1001	Output	
OUT_ADC2_L	r	0A	000 1010	Output	
OUT_ADC2_H	r	0B	000 1011	Output	
OUT_ADC3_L	r	0C	000 1100	Output	
OUT_ADC3_H	r	0D	000 1101	Output	
INT_COUNTER_REG	r	0E	000 1110		
WHO_AM_I	r	0F	000 1111	00110011	Dummy register
Reserved (do not modify)		10 - 1E			Reserved
TEMP_CFG_REG	rw	1F	001 1111		
CTRL_REG1	rw	20	010 0000	00000111	
CTRL_REG2	rw	21	010 0001	00000000	
CTRL_REG3	rw	22	010 0010	00000000	
CTRL_REG4	rw	23	010 0011	00000000	
CTRL_REG5	rw	24	010 0100	00000000	
CTRL_REG6	rw	25	010 0101	00000000	
REFERENCE	rw	26	010 0110	00000000	
STATUS_REG2	r	27	010 0111	00000000	
Reserved (do not modify)	-	28	010 1000	00000000	Reserved
OUT_X	r	29	010 1001	Output	
Reserved (do not modify)	-	2A	010 1010	00000000	Reserved
OUT_Y	r	2B	010 1011	Output	
Reserved (do not modify)	r	2C	010 1100	00000000	Reserved
OUT_Z	r	2D	010 1101	Output	
FIFO_CTRL_REG	rw	2E	010 1110	00000000	
FIFO_SRC_REG	r	2F	010 1111		
IG1_CFG	rw	30	011 0000	00000000	

Table 17. Register address map (continued)

Name	Type	Register address		Default	Comment
		Hex	Binary		
IG1_SOURCE	r	31	011 0001	00000000	
IG1_THS	rw	32	011 0010	00000000	
IG1_DURATION	rw	33	011 0011	00000000	
IG2_CFG	rw	34	011 0100	00000000	
IG2_SOURCE	r	35	011 0101	00000000	
IG2_THS	rw	36	011 0110	00000000	
IG2_DURATION	rw	37	011 0111	00000000	
CLICK_CFG	rw	38	011 1000	00000000	
CLICK_SRC	r	39	011 1001	00000000	
CLICK_THS	rw	3A	011 1010	00000000	
TIME_LIMIT	rw	3B	011 1011	00000000	
TIME_LATENCY	rw	3C	011 1100	00000000	
TIME_WINDOW	rw	3D	011 1101	00000000	
Act_THS	rw	3E	011 1110	00000000	
Act_DUR	rw	3F	011 1111	00000000	

Registers marked as *Reserved* must not be changed. Writing to those registers may cause permanent damage to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered up.

8 Register description

8.1 STATUS_REG_AUX (07h)

Table 18. STATUS_REG_AUX register

321OR	3OR	2OR	1OR	321DA	3DA	2DA	1DA

Table 19. STATUS_REG_AUX register description

321OR	1, 2 and 3-channel data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous set)
3OR	3rd channel data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the 3rd ADC channel has overwritten the previous data)
2OR	2nd channel data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the 2nd ADC channel has overwritten the previous data)
1OR	1st channel data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the 1st ADC channel has overwritten the previous data)
321DA	1st, 2nd and 3rd channel new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
3DA	3rd channel new data available. Default value: 0 (0: new data for the 3rd ADC channel is not yet available; 1: new data for the 3rd ADC channel is available)
2DA	2nd channel new data available. Default value: 0 (0: new data for the 2nd ADC channel is not yet available; 1: new data for the 2nd ADC channel is available)
1DA	1st channel new data available. Default value: 0 (0: new data for the 1st ADC channel is not yet available; 1: new data for the 1st ADC channel is available)

8.2 OUT_ADC1_L (08h), OUT_ADC1_H (09h)

Acceleration data - auxiliary ADC1 data. The value is expressed in two's complement.

8.3 OUT_ADC2_L (0Ah), OUT_ADC2_H (0Bh)

Acceleration data - auxiliary ADC2 data. The value is expressed in two's complement.

8.4 OUT_ADC3_L (0Ch), OUT_ADC3_H (0Dh)

Acceleration or temperature sensor data - auxiliary ADC3 data. The value is expressed in 2's complement.

8.5 INT_COUNTER_REG (0Eh)

Table 20. INT_COUNTER_REG register

IC7	IC6	IC5	IC4	IC3	IC2	IC1	IC0

INT2 pin counter. This register can be reset by reading the *REFERENCE (26h)* register.

8.6 WHO_AM_I (0Fh)

Table 21. WHO_AM_I register

0	0	1	1	0	0	1	1

Device identification register.

8.7 TEMP_CFG_REG (1Fh)

Table 22. TEMP_CFG_REG register

ADC_PD	TEMP_EN	0	0	0	0	0	0

Table 23. TEMP_CFG_REG register description

ADC_PD	ADC enable. Default value: 0 (0: ADC disabled; 1: ADC enabled)
TEMP_EN	Temperature sensor (T) enable. Default value: 0 (0: T disabled; 1: T enabled)

8.8 CTRL_REG1 (20h)

Table 24. CTRL_REG1 register

ODR3	ODR2	ODR1	ODR0	LPen	Zen	Yen	Xen

Table 25. CTRL_REG1 register description

ODR [3:0]	Data rate selection. Default value: 00 (0000: 50 Hz; Others: Refer to *Table 26*)3
LPen	Low-power mode enable. Default value: 0 (0: Normal mode, 1: Low-power mode)
Zen	Z-axis enable. Default value: 1 (0: Z-axis disabled; 1: Z-axis enabled)
Yen	Y-axis enable. Default value: 1 (0: Y-axis disabled; 1: Y-axis enabled)
Xen	X-axis enable. Default value: 1 (0: X-axis disabled; 1: X-axis enabled)

ODR [3:0] is used to set power mode and ODR selection. The following table provides all frequencies resulting from a combination of ODR [3:0].

Table 26. Data rate configuration

ODR3	ODR2	ODR1	ODR0	Power mode selection
0	0	0	0	Power-down mode
0	0	0	1	Normal / Low-power mode (1 Hz)
0	0	1	0	Normal / Low-power mode (10 Hz)
0	0	1	1	Normal / Low-power mode (25 Hz)
0	1	0	0	Normal / Low-power mode (50 Hz)
0	1	0	1	Normal / Low-power mode (100 Hz)
0	1	1	0	Normal / Low-power mode (200 Hz)
0	1	1	1	Normal / Low-power mode (400 Hz)
1	0	0	0	Low-power mode (1.6 KHz)
1	0	0	1	Normal (1.344 kHz) / Low-power mode (5.376 kHz)

8.9 CTRL_REG2 (21h)

Table 27. CTRL_REG2 register

HPM1	HPM0	HPCF2	HPCF1	FDS	HPCLICK	HPIS2	HPIS1

Table 28. CTRL_REG2 register description

HPM [1:0]	High-pass filter mode selection. Default value: 00 Refer to *Table 29*
HPCF [2:1]	High-pass filter cutoff frequency selection
FDS	Filtered data selection. Default value: 0 (0: internal filter bypassed; data from internal filter sent to output register and FIFO)
HPCLICK	High-pass filter enabled for CLICK function. (0: filter bypassed; 1: filter enabled)
HPIS2	High-pass filter enabled for IG2 (0: filter bypassed; 1: filter enabled)
HPIS1	High-pass filter enabled for IG1 (0: filter bypassed; 1: filter enabled)

Table 29. High-pass filter mode configuration

HPM1	HPM0	High pass filter mode
0	0	Normal mode (reset by reading the □□□□□□□□□□□□ register)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Auto-reset on interrupt event

8.10 CTRL_REG3 (22h)

Table 30. CTRL_REG3 register

INT1_ CLICK	INT1_IG1	INT1_IG2	INT1_ DRDY1	INT1_ DRDY2	INT1_ WTM	INT1_ OVERRUN	--

Table 31. CTRL_REG3 register description

INT1_CLICK	Click interrupt on INT1. Default value 0 (0: disable; 1: enable)
INT1_IG1	IG1 interrupt generator 1 on INT1. Default value 0 (0: disable; 1: enable)
INT1_IG2	IG2 interrupt generator 2 on INT1. Default value 0 (0: disable; 1: enable)
INT1_DRDY1	DRDY1 interrupt on INT1. Default value 0 (0: disable; 1: enable)
INT1_DRDY2	DRDY2 interrupt on INT1. Default value 0 (0: disable; 1: enable)
INT1_WTM	FIFO watermark interrupt on INT1. Default value 0 (0: disable; 1: enable)
INT1_OVERRUN	FIFO overrun interrupt on INT1. Default value 0 (0: disable; 1: enable)

8.11 CTRL_REG4 (23h)

Table 32. CTRL_REG4 register

BDU	-	FS1	FS0	-	ST1	ST0	SIM

Table 33. CTRL_REG4 register description

BDU	Block data update. Default value: 0 (0: continuous update. For linear acceleration data output this bit must be set to 0; 1: this bit must be set to 1 for temperature sensor reading only)
FS [1:0]	Full scale selection. Default value: 00 (00: ±2*g*; 01: ±4*g*; 10: ±8*g*; 11: ±16*g*)
ST [1:0]	Self-test enable. Default value: 00 (00: self-test disabled; Other: See *Table 34*)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface)

Table 34. Self-test mode configuration

ST1	ST0	Self-test mode
0	0	Normal mode
0	1	Self-test 0
1	0	Self-test 1
1	1	--

8.12 CTRL_REG5 (24h)

Table 35. CTRL_REG5 register

BOOT	FIFO_EN	--	--	LIR_IG1	D4D_IG1	LIR_IG2	D4D_IG2

Table 36. CTRL_REG5 register description

BOOT	Reboot memory content. Default value: 0 (0: Normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO enable)
LIR_IG1	Latch interrupt request on IG1_SOURCE register, with IG1_SOURCE register cleared by reading IG1_SOURCE itself. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
D4D_IG1	4D enable: 4D detection is enabled on INT1 when 6D bit on IG1_CFG is set to ‘1’
LIR_IG2	Latch interrupt request on IG2_SOURCE register, with IG2_SOURCE register cleared by reading IG2_SOURCE itself. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
D4D_IG2	4D enable: 4D detection is enabled on Interrupt 2 generator when 6D bit on IG2_CFG is set to ‘1’

8.13 CTRL_REG6 (25h)

Table 37. CTRL_REG6 register

INT2_CLICK	INT2_IG1	INT2_IG2	INT2_BOOT	INT2_ACT	-	H_LACTIVE	-

Table 38. CTRL_REG6 register description

INT2_CLICK	Click interrupt on INT2 pin. Default value: 0 (0: disable; 1: enable)
INT2_IG1	Interrupt generator 1 enabled on INT2 pin. Default value: 0 (0: function disable; 1: function enable)
INT2_IG2	Interrupt generator 2 enabled on INT2 pin. Default value: 0 (0: function disable; 1: function enable)
INT2_BOOT	Boot on INT2 pin enable. Default value: 0 (0: disable; 1: enable)
INT2_ACT	“Sleep-to-wake” / “Return-to-sleep” function interrupt enable on INT2 pin. Default value: 0 (0: disable; 1: enable)
H_LACTIVE	Interrupt active value. Default value: 0 (0: interrupt active high; 1: interrupt active low)

8.14 REFERENCE (26h)

Table 39. REFERENCE register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 40. REFERENCE register description

Ref [7:0]	Reference value for interrupt generation. Default value: 0000 0000

8.15 STATUS_REG2 (27h)

Table 41. STATUS_REG2 register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 42. STATUS_REG2 register description

ZYXOR	X-, Y- and Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new set of data has overwritten the previous set)
ZOR	Z-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X-axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X-, Y- and Z-axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z-axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y-axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XDA	X-axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

8.16 OUT_X (29h)

X-axis acceleration data. The value is expressed in two’s complement with 8-bit data representation left-justified.

8.17 OUT_Y (2Bh)

Y-axis acceleration data. The value is expressed in two's complement with 8-bit data representation left-justified.

8.18 OUT_Z (2Dh)

Z-axis acceleration data. The value is expressed in two's complement with 8-bit data representation left-justified.

8.19 FIFO_CTRL_REG (2Eh)

Table 43. FIFO_CTRL_REG register

FM1	FM0	TR	FTH4	FTH3	FTH2	FTH1	FTH0

Table 44. FIFO_CTRL_REG register description

FM [1:0]	FIFO mode selection. Default value: 00 (see *Table 45*)
TR	Trigger selection. Default value: 0 0: trigger event linked to trigger signal on INT1 1: trigger event linked to trigger signal on INT2
FTH [4:0]	Default value: 0

Table 45. FIFO mode configuration

FM1	FM0	Self-test mode
0	0	Bypass mode
0	1	FIFO mode
1	0	Stream mode
1	1	Stream-to-FIFO mode

8.20 FIFO_SRC_REG (2Fh)

Table 46. FIFO_SRC_REG register

WTM	OVRN_FIFO	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 47. FIFO_SRC_REG register description

WTM	WTM bit is set high when FIFO content exceeds watermark level
OVRN_FIFO	OVRN bit is set high when FIFO buffer is full; this means that the FIFO buffer contains 32 unread samples. At the following ODR a new sample set replaces the oldest FIFO value. The OVRN bit is set to 0 when the first sample set has been read
EMPTY	EMPTY flag is set high when all FIFO samples have been read and FIFO is empty
FSS [4:0]	FSS [4:0] field always contains the current number of unread samples stored in the FIFO buffer. When FIFO is enabled, this value increases at ODR frequency until the buffer is full, whereas, it decreases every time one sample set is retrieved from FIFO

8.21 IG1_CFG (30h)

Table 48. IG1_CFG register

AOI	6D	ZHIE/ ZUPE	ZLIE/ ZDOWNE	YHIE/ YUPE	YLIE/ YDOWNE	XHIE/ XUPE	XLIE/ XDOWNE

Table 49. IG1_CFG register description

AOI	AND/OR combination of interrupt events. Default value: 0 (Refer to *Table 50*)
6D	6-direction detection function enabled. Default value: 0 (Refer to *Table 50*)
ZHIE/ ZUPE	Enable interrupt generation on Z high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
ZLIE/ ZDOWNE	Enable interrupt generation on Z low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YHIE/ YUPE	Enable interrupt generation on Y high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
YLIE/ YDOWNE	Enable interrupt generation on Y low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
XHIE/ XUPE	Enable interrupt generation on X high event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)
XLIE/ XDOWNE	Enable interrupt generation on X low event or on direction recognition. Default value: 0 (0: disable interrupt request; 1: enable interrupt request)

The content of this register is loaded at boot.

A write operation to this address is possible only after system boot.

Table 50. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

The difference between AOI-6D = ‘01’ and AOI-6D = ‘11’.

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when the orientation moves from an unknown zone to a known zone. The interrupt signal remains for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when the orientation is inside a known zone. The interrupt signal remains until the orientation is within the zone.

8.22 IG1_SOURCE (31h)

Table 51. IG1_SOURCE register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 52. IG1_SOURCE register description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Interrupt 1 source register. Read-only register.

Reading at this address clears the IG1_SOURCE IA bit (and the interrupt signal on the INT1 pin) and allows data in the IG1_SOURCE register to be refreshed if the latched option was chosen.

8.23 IG1_THS (32h)

Table 53. IG1_THS register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 54. IG1_THS register description

THS [6:0]	Interrupt 1 threshold. Default value: 000 0000

8.24 IG1_DURATION (33h)

Table 55. IG1_DURATION register

0	D6	D5	D4	D3	D2	D1	D0

Table 56. IG1_DURATION register description

D [6:0]	Duration value. Default value: 000 0000

D [6:0] bits set the minimum duration of the interrupt 1 event to be recognized. Duration steps and maximum values depend on the ODR chosen.

8.25 IG2_CFG (34h)

Table 57. IG2_CFG register

AOI	6D	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 58. IG2_CFG register description

AOI	AND/OR combination of interrupt events. Default value: 0 (Refer to *Table 59: Interrupt mode*)
6D	6-direction detection function enabled. Default value: 0 (Refer to *Table 59: Interrupt mode*)
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value lower than preset threshold)

The content of this register is loaded at boot.

A write operation to this address is possible only after system boot.

Table 59. Interrupt mode

AOI	6D	Interrupt mode
0	0	OR combination of interrupt events
0	1	6-direction movement recognition
1	0	AND combination of interrupt events
1	1	6-direction position recognition

The difference between AOI-6D = ‘01’ and AOI-6D = ‘11’.

AOI-6D = ‘01’ is movement recognition. An interrupt is generated when the orientation moves from an unknown zone to a known zone. The interrupt signal remains for a duration ODR.

AOI-6D = ‘11’ is direction recognition. An interrupt is generated when orientation is within a known zone. The interrupt signal remains while the orientation is within this zone.

8.26 IG2_SOURCE (35h)

Table 60. IG2_SOURCE register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 61. IG2_SOURCE register description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X high event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X low event has occurred)

Interrupt 2 source register. Read-only register.

Reading at this address clears the IG2_SOURCE IA bit (and the interrupt signal on the INT2 pin) and allows data in the IG2_SOURCE register to be refreshed if the latched option was chosen.

8.27 IG2_THS (36h)

Table 62. IG2_THS register

0	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 63. IG2_THS register description

THS[6:0]	Interrupt 1 threshold. Default value: 000 0000

8.28 IG2_DURATION (37h)

Table 64. IG2_DURATION register

0	D6	D5	D4	D3	D2	D1	D0

Table 65. IG2_DURATION register description

D [6:0]	Duration value. Default value: 000 0000

The **D [6:0]** bits set the minimum duration of the Interrupt 2 event to be recognized. Duration time steps and maximum values depend on the ODR chosen.

8.29 CLICK_CFG (38h)

Table 66. CLICK_CFG register

--	--	ZD	ZS	YD	YS	XD	XS

Table 67. CLICK_CFG register description

ZD	Enable interrupt double-click on Z-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
ZS	Enable interrupt single-click on Z-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YD	Enable interrupt double-click on Y-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
YS	Enable interrupt single-click on Y-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XD	Enable interrupt double-click on X-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)
XS	Enable interrupt single-click on X-axis. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured accel. value higher than preset threshold)

8.30 CLICK_SRC (39h)

Table 68. CLICK_SRC register

-	IA	DCLICK	SCLICK	Sign	Z	Y	X

Table 69. CLICK_SRC register description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
DCLICK	Double-click enable. Default value: 0 (0: double-click detection disable, 1: double-click detection enable)
SCLICK	Single-click enable. Default value: 0 (0: single-click detection disable, 1: single-click detection enable)
Sign	Click sign. 0: positive detection, 1: negative detection
Z	Z click detection. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
Y	Y click detection. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
X	X click detection. Default value: 0 (0: no interrupt, 1: X high event has occurred)

8.31 CLICK_THS (3Ah)

Table 70. CLICK_THS register

LIR	THS6	THS5	THS4	THS3	THS2	THS1	THS0

Table 71. CLICK_THS register description

LIR	Latch interrupt request on CLICK_SRC register, with CLICK_SRC register cleared by reading CLICK_SRC itself. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched)
THS [6:0]	Click threshold. Default value: 000 0000

8.32 TIME_LIMIT (3Bh)

Table 72. TIME_LIMIT register

-	TLI6	TLI5	TLI4	TLI3	TLI2	TLI1	TLI0

Table 73. TIME_LIMIT register description

TLI [6:0]	Click time limit. Default value: 000 0000

8.33 TIME_LATENCY (3Ch)

Table 74. TIME_LATENCY register

TLA7	TLA6	TLA5	TLA4	TLA3	TLA2	TLA1	TLA0

Table 75. TIME_LATENCY register description

TLA [7:0]	Double-click time latency. Default value: 0000 0000

8.34 TIME_WINDOW (3Dh)

Table 76. TIME_WINDOW register

TW7	TW6	TW5	TW4	TW3	TW2	TW1	TW0

Table 77. TIME_WINDOW register description

TW [7:0]	Double-click time window. Default value: 0000 0000

8.35 Act_THS (3Eh)

Table 78. Act_THS register

--	Acth6	Acth5	Acth4	Acth3	Acth2	Acth1	Acth0

Table 79. Act_THS register description

Acth [6:0]	Sleep-to-wake, Return-to-sleep activation threshold 1LSB = 16 m*g* @ 2*g* FS

8.36 Act_DUR (3Fh)

Table 80. Act_DUR register

ActD7	ActD6	ActD5	ActD4	ActD3	ActD2	ActD1	ActD0

Table 81. Act_DUR register description

ActD [7:0]	Sleep-to-wake, Return-to-sleep duration DUR = (Act_DUR + 1)*8/ODR

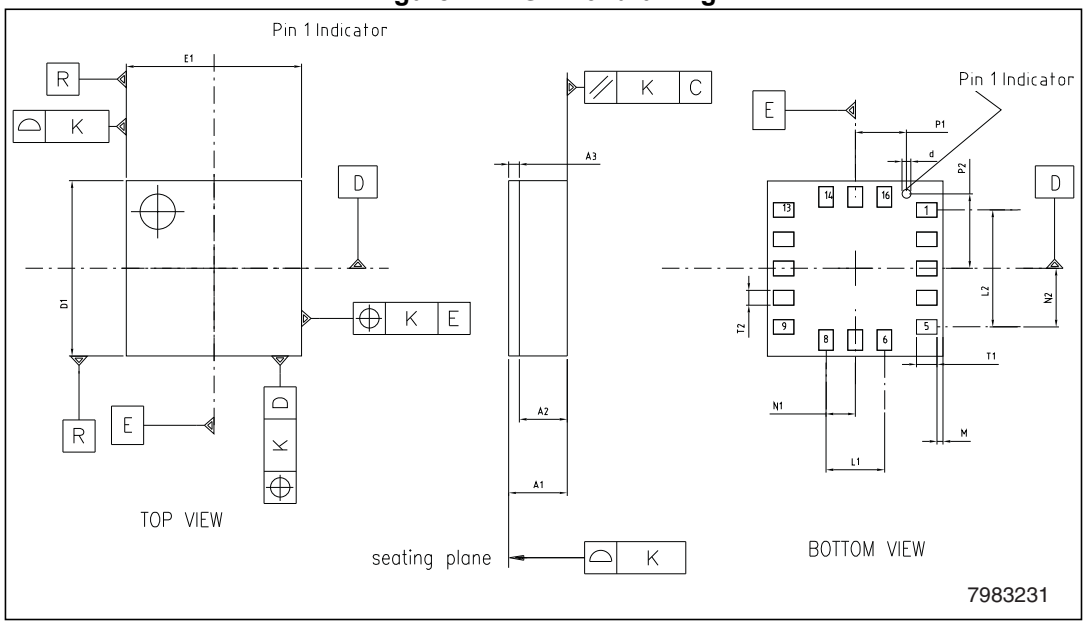
9 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: *www.st.com.* ECOPACK is an ST trademark.

Table 82. LGA-16: mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A1			1
A2		0.785	
A3		0.2	
D1	2.85	3	3.15
E1	2.85	3	3.15
L1		1	1.06
L2		2	2.06
N1		0.5	
N2		1	
M	0.04	0.1	0.16
P1		0.875	
P2		1.275	
T1	0.29	0.35	0.41
T2	0.19	0.25	0.31
d		0.15	
k		0.05	

Figure 12. LGA-16: drawing



10 Revision history

Table 83. Document revision history

Date	Revision	Changes
21-Sep-2012	1	Initial release.
30-Jan-2013	2	Document status promoted from preliminary to production data.
19-Jun-2014	3	Updated Trigger mode to Stream-to-FIFO mode Minor textual modifications throughout document.

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