Atmel ATWILC1000-MR110PA

IEEE 802.11 b/g/n IoT Module

PRELIMINARY DATASHEET

Description

The Atmel® WILC1000-MR110PA is a low-power consumption 802.11 b/g/n IoT (Internet of Things) module which is specifically optimized for low power IoT applications. The highly integrated module features small form factor (21.5mm x 14.5mm x3.4mm) while fully integrating Power Amplifier, LNA, Switch, Power Management and PCB antenna. With seamless roaming capabilities and advanced security, it could be interoperable with various vendors' 802.11b/g/n Access Points in wireless LAN. The module provides SPI and SDIO to interface to host controller.

Features

Key features of the WILC1000-MR110PA:

- EEE 802.11 b/g/n RF/PH/MAC SoC
- IEEE 802.11 b/g/n (1x1) for up to 72 Mbps
- Single spatial stream in 2.4GHz RF band
- Integrated PA and T/R Switch
- Integrated PCB antenna
- Superior Sensitivity and Range via advanced PHY signal processing
- Advanced Equalization and Channel Estimation
- Advanced Carrier and Timing Synchronization

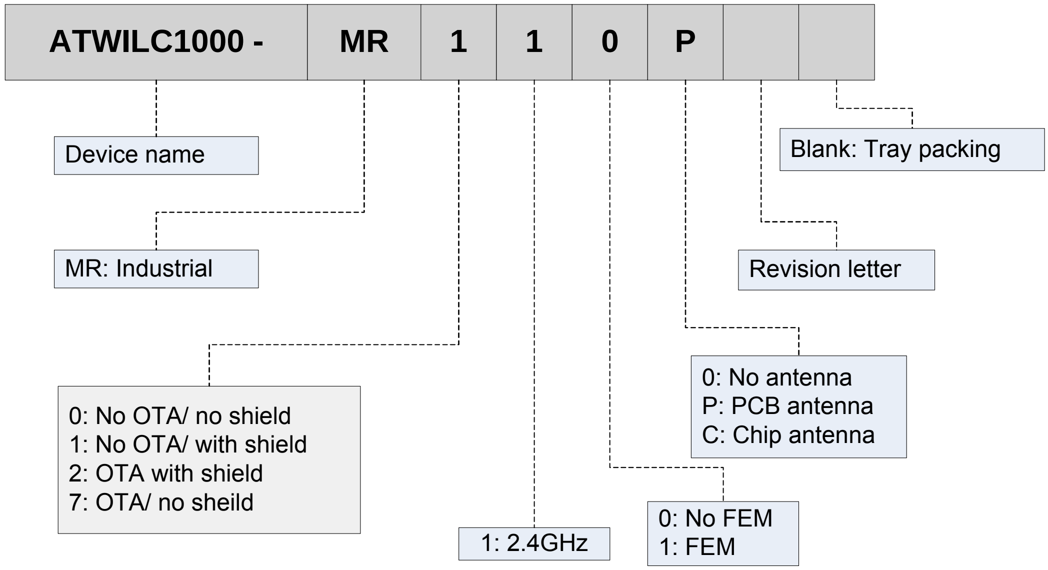
System features of the WILC1000-MR110PA:

- Wi-Fi Direct and Soft-AP support
- Supports IEEE 802.11 WEP, WPA, WPA2 Security
- On-chip memory management engine to reduce host load
- I/O operating range of 1.8V to 3.6V
- Operating temperature range of -30°C to +85°C
- SPI and SDIO host interfaces
- Power Save Modes
  - 4µA Deep Power Down mode typical @3.3V I/O
  - 850µA Doze mode (State is preserved)
  - On-chip low power sleep oscillator
  - Fast host wake-up by chip pin or clock-less transaction
- Wi-Fi security WEP, WPA, WPA2 and WPS

1. Ordering Information

Ordering code	Package	Description
ATWILC1000-MR110PA	22 X 15mm	Certified module with ATWILC1000A-Mu chip and PCB antenna

Figure 1-1. ATWILC1000-MR110PA ordering information details



2. Deliverable

2.1 Deliverable

The following products and software will be part of the product.

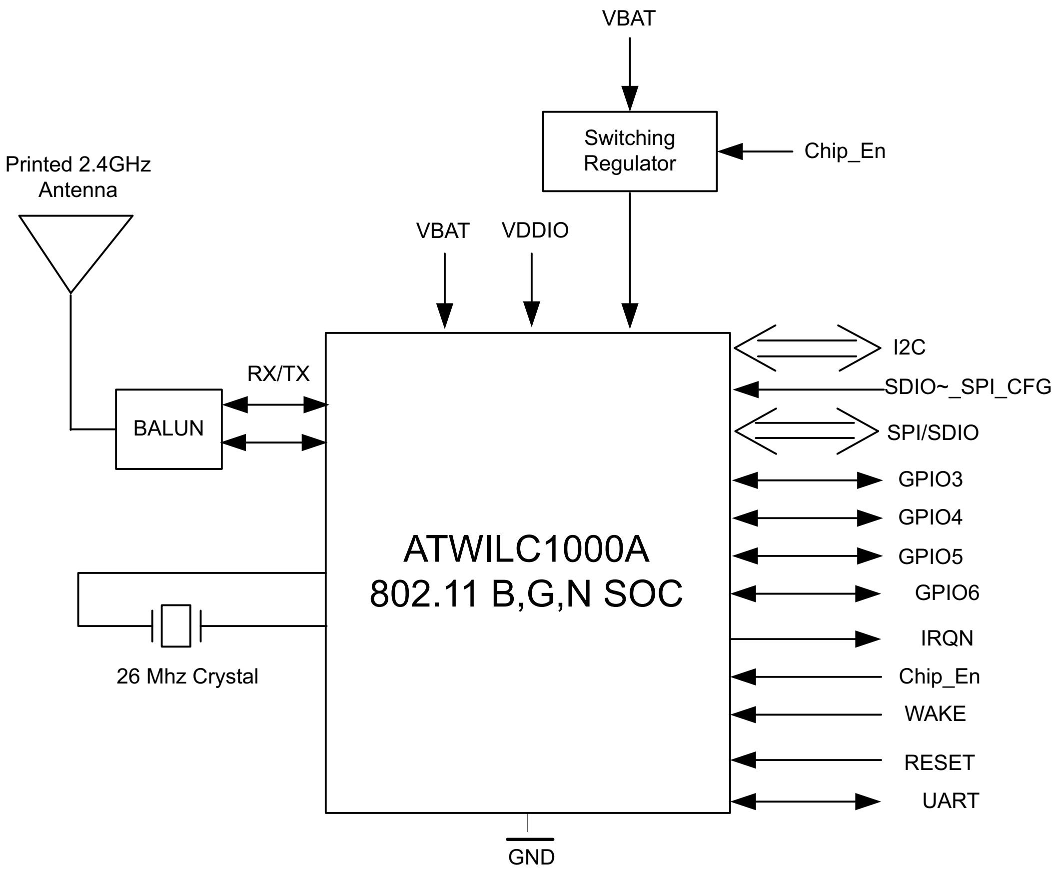
- Module with packaging
- Evaluation kits
- Software utility for integration and performance test
- Product Datasheet

2.2 Regulatory certificates

The product is a pre-tested module certified to FCC Part 15, CE and TELEC.

3. Block Diagram

Figure 3-1. ATWILC1000-MR110PA Block Diagram



4. General Specifications

4.1 Wi-Fi RF Specification

Table 4-1. Conditions: VBAT=3.6V; VDDIO=3.3V; Temp: 25°C

Feature	Description
Module Part Number	ATWILC1000-MR110PA
WLAN Standard	IEEE 802.11b/g/n, Wi-Fi compliant
Host Interface	SPI, SDIO
Dimension	L x W x H: 21.5 x 14.5 x 1.5 (typical) mm
Frequency Range	2.412 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)
Number of Channels	11 for North America, 13 for Europe, and 14 for Japan
Modulation	802.11b: DQPSK, DBPSK, CCK 802.11g/n: OFDM /64-QAM,16-QAM, QPSK, BPSK

Table 4-1. Conditions: VBAT=3.6V; VDDIO=3.3V; Temp: 25°C (Continued)

Feature	Description
Output Power	802.11b /11Mbps: 19 dBm ± 1.5 dB @ EVM -9dB
	802.11g /54Mbp : 14.5 dBm ± 2 dB @ EVM -25dB
	802.11n /65Mbps : 13 dBm ± 2 dB @ EVM -28dB
Receive Sensitivity (11n,20MHz) @10% PER	MCS=0, PER @ -90 ± 1dBm, typical
	MCS=1, PER @ -86 ± 1dBm, typical
	MCS=2, PER @ -84 ± 1dBm, typical
	MCS=3, PER @ -81.5 ± 1dBm, typical
	MCS=4, PER @ -78 ± 1dBm, typical
	MCS=5, PER @ -74 ± 1dBm, typical
	MCS=6, PER @ -72.5 ± 1dBm, typical
	MCS=7, PER @ -71.5 ± 1dBm, typical
Receive Sensitivity (11g) @10% PER	6Mbps, PER @ -91 ± 1dBm, typical
	9Mbps, PER @ -89 ± 1dBm, typical
	12Mbps, PER @ -88.5 ± 1dBm, typical
	18Mbps, PER @ -86.5 ± 1dBm, typical
	24Mbps, PER @ -84 ± 1dBm, typical
	36Mbps, PER @ -78.5 ± 1dBm, typical
	48Mbps, PER @ -77 ± 1dBm, typical
	54Mbps, PER @ -75 ± 1dBm, typical
Receive Sensitivity (11b) @8% PER	1Mbps, PER @ -98 ± 1dBm, typical
	2Mbps, PER @ -95 ± 1dBm, typical
	5.5Mbps, PER @ -93 ± 1dBm, typical
	11Mbps, PER @ -89 ± 1dBm, typical
Data Rate	802.11b: 1, 2, 5.5, 11Mbps
	802.11g 6, 9, 12, 18, 24, 36, 48, 54Mbps
Data Rate	802.11n: 6.5, 13, 19.5, 26, 39, 52, 58.5, 65Mbps
Data Rate (20MHz ,short GI,400ns)	802.11n: 7.2, 14.4, 21.7, 28.9, 43.3, 57.8, 65,72.2Mbps
Maximum Input Level	802.11b: 0dBm typical
	802.11g/n: -5dBm typical

Table 4-1. Conditions: VBAT=3.6V; VDDIO=3.3V; Temp: 25°C (Continued)

Feature	Description
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 85°C
Humidity	Operating Humidity 10% to 95% Non-Condensing Storage Humidity 5% to 95% Non-Condensing

4.2 Voltages

4.2.1 Absolute Maximum Ratings

Table 4-2. Absolute Maximum Ratings

Symbol	Description	Min	Typical	Max	Unit
VBAT	Input supply voltage	-0.3		5.5	V
VDDIO	SPI voltage	-0.3		3.6	V

4.2.2 Recommended Operating Ratings

Table 4-3. Recommended Operating Ratings

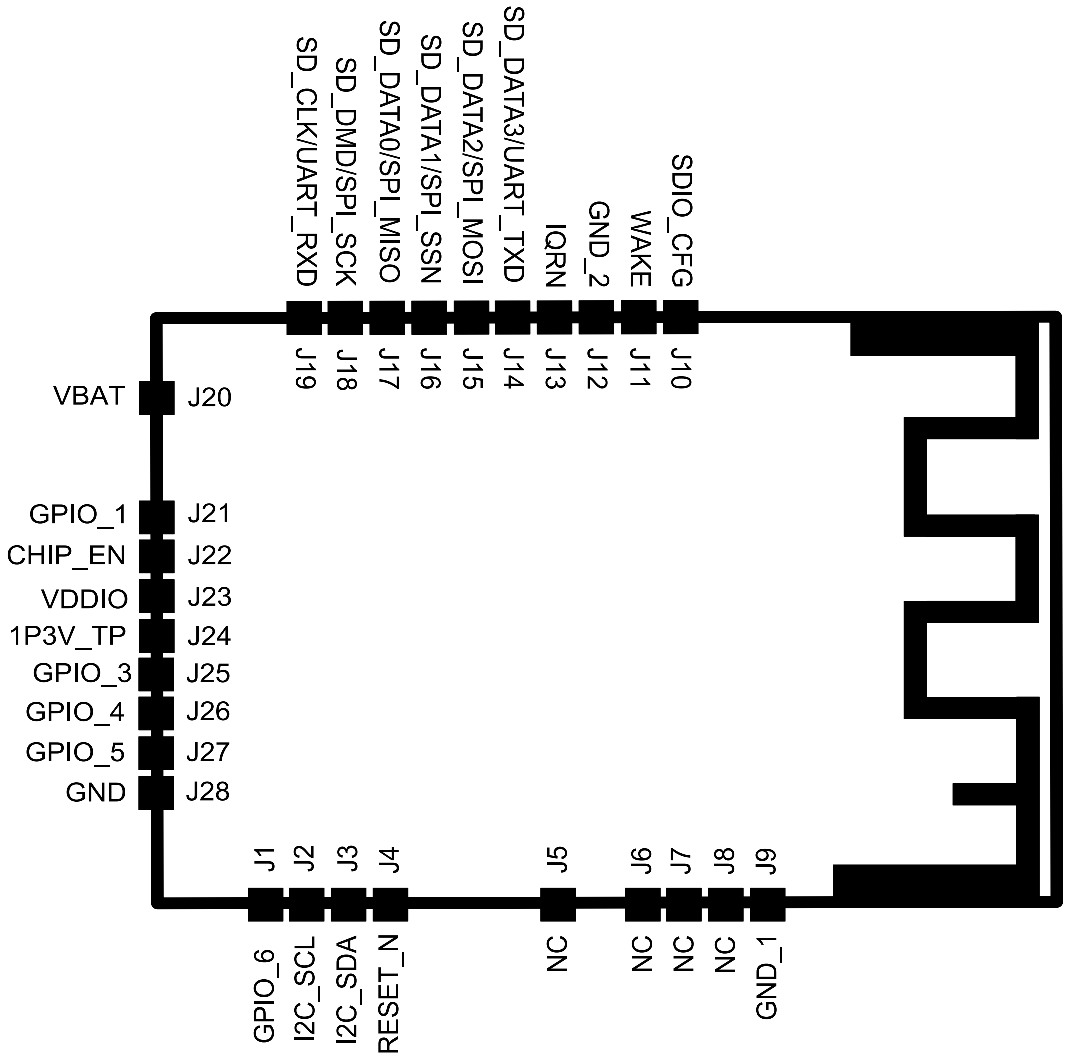
Symbol	Test conditions	Min	Typical	Max	Unit
VBAT	-30°C - +85°C	3.0	3.6	4.2	V
VDDIO(1)	-30°C - +85°C	1.8	3.3	3.6	V

Note: 1. The voltage of VDDIO is dependent on system I/O voltage.

5. Pin Assignments

5.1 Top View

Figure 5-1. Top View



5.2 Pin Descriptions

Table 5-1. Pin Definitions

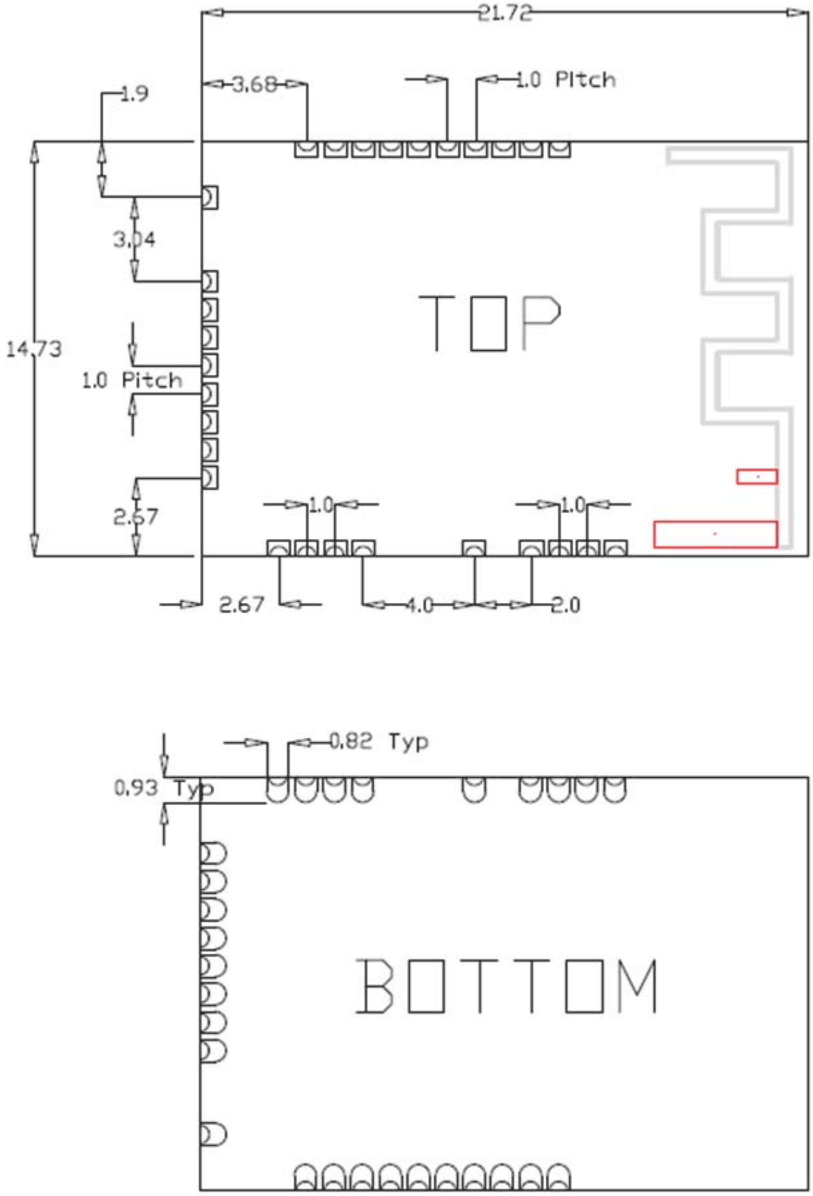
Pin #	Name	Type	Description	Programmable Pull-up Resistor
1	GPIO_6	I/O	General purpose I/O.	Yes
2	I2C_SCL	I/O	I^2C Slave Clock. Can be configured as either master or slave. I^2C interface is only used for test purposes. This pin should be brought to a test point only. Do not add a pull-up resistor.	Yes
3	I2C_SDA	I/O	I^2C Slave Data. Can be configured as either master or slave. I^2C interface is only used for test purposes. This pin should be brought to a test point only. Do not add a pull-up resistor.	Yes
4	RESET_N	I	Active-Low Hard Reset. When asserted to a low level, the module will be placed in a reset state. When asserted to a high level, the module will run normally. Connect to a host output that defaults low at power up. If the output floats, add a 1M ohm pull-down resistor if necessary to ensure a low level at power up.	No
5	NC	-	No connect	
6	NC	-	No connect	
7	NC	-	No connect	
8	NC	-	No connect	
9	GND_1	-	GND	
10	SDIO~_SPI_CFG	I	Tie to VDDIO through a 1M ohm resistor to enable the SPI interface. Connect to ground to enable SDIO interface.	No
11	WAKE	I	Host Wake control. Can be used to wake up the module from Doze mode. Connect to a host GPIO.	No
12	GND_2	-	GND	
13	IRQN	O	ATWINC1500 Device Interrupt.	No
14	SD_DAT3/UART_TXD	SDIO=I/O UART=O	SDIO Data Line 3 from ATWILC1000-MR110PA when module is configured for SDIO. UART Transmit Output from ATWILC1000 when module is configured for SPI.	Yes
15	SD_DAT2/SPI_RXD	SDIO=I/O SPI=I	SDIO Data Line 2 signal from ATWILC1000-MR110PA when module is configured for SDIO. SPI MOSI (Master Out Slave In) pin when module is configured for SPI.	Yes

Table 5-1. Pin Definitions (Continued)

Pin #	Name	Type	Description	Programmable Pull-up Resistor
16	SD_DAT1/SPI_SSN	SDIO=I/O SPI=I	SDIO Data Line 1 from ATWILC1000-MR110PA when module is configured for SDIO. Active Low SPI Slave Select from ATWILC1000 when module is configured for SPI.	Yes
17	SD_DAT0/SPI_TXD	SDIO=I/O SPI=O	SDIO Data Line 0 from ATWILC1000-MR110PA when module is configured for SDIO. SPI MISO (Master In Slave Out) pin from ATWILC1000 when module is configured for SPI.	Yes
18	SD_CMD/SPI_CLK	SDIO=I/O SPI=I	SDIO CMD Line from ATWILC1000-MR110PA when module is configured for SDIO. SPI Clock from ATWILC1000 when module is configured for SPI.	Yes
19	SD_CLK/UART_RXD	SDIO=I UART=I	SDIO Clock Line from ATWILC1000-MR110PA when module is configured for SDIO. UART Receive input to ATWILC1000 when module is configured for SPI.	Yes
20	VBATT	-	Battery power supply	
21	GPIO_1	I	General Purpose I/O.	Yes
22	CHIP_EN	I	Module enable. High level enables module, low level places module in Power Down mode. Connect to a host Output that defaults low at power up. If the output floats, add a 1M ohm pull-down resistor if necessary to ensure a low level at power up.	No
23	VDDIO	-	I/O Power Supply. Must match host I/O voltage.	
24	1P3V_TP	-	1.3V VDD Core Test Point	
25	GPIO_3	-	General purpose I/O.	Yes
26	GPIO_4	I/O	General purpose I/O.	Yes
27	GPIO_5	I/O	General purpose I/O.	Yes
28	GND_3	-	GND	

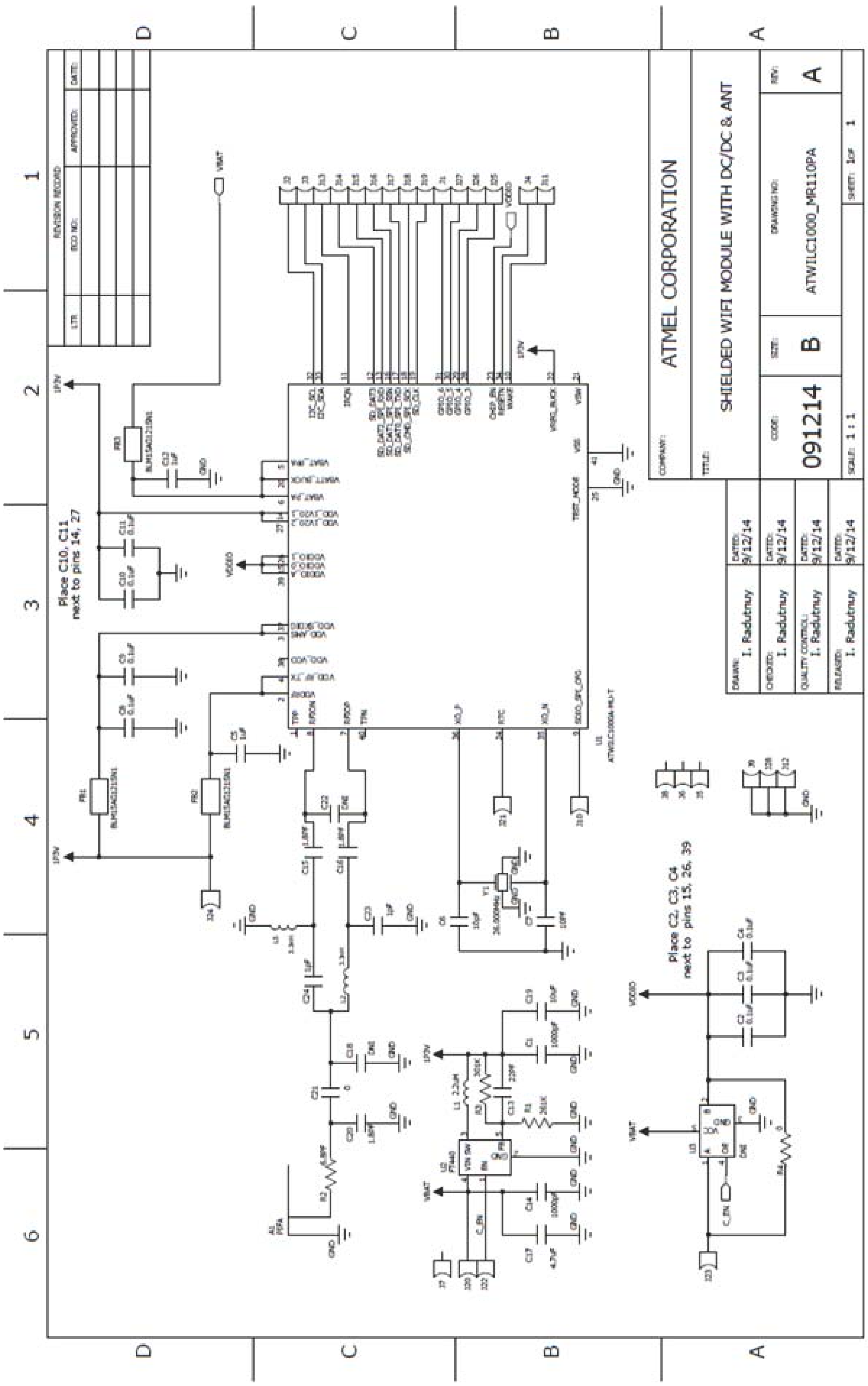
6. Module Outline Drawings

Figure 6-1. Module Drawings - Top and Bottom Views



7. Module Schematic

Figure 7-1. ATWILC1000-MR110PA Schematic



8. Module Bill of Materials (BOM)

Table 8-1. ATWILC1000-MR110PA Bill of Material

WiFi shielded module with DC/DC, discrete balun, no load switch, with printed antenna Revised: Thursday, September 11, 2014

ATWILC1000-MR110P Revision: A

Item	Qty	Reference	Value	Description	Manufacturer	Part Number	Footprint
1	2	C5,C12	1.0uF	CAP,CER,1.0uF,20%,X5R,0402,6.3V	Panasonic	ECJ-0EB0J105M	CS0402
2	2	C1,C14 C2,C3,C4,C8,C9,C10,	1000PF	CAP CER 1000PF 50V 10% X7R 0402	Murata	GRM155R71H102KA01D	CS0402
3	7	C11	0.1uF	CAP,CER,0.1uF,10%,X5R,0402,10V	AVX	0402ZD104KAT2A	CS0402
4	1	C13	22pF	CAP,CER,22pF,5%,NPO,0402,50V	Murata	GRM1555C1H220JZ01	CS0402
5	1	C17	4.7uF	CAP CER 4.7UF 4V 20% X5R 0402	Murata	GRM155R60G475ME47D	CS0402
6	2	C23,C24	1pF	CAP CER 1PF 50V NP0 0201	Murata	GRM0335C1H1R0CA01D	CS0201
7	2	C6,C7	10PF	CAP CER 10PF 50V 1% NP0 0402	Murata	GRM1555C1H100FA01D	CS0402
8	2	C15,C16	1.8PF	CAP CER 1.8PF 50V NP0 0201	Murata	GRM0335C1H1R8CA01D	CS0201
9	1	C19	10uF	CAP CER 10UF 4V 20% X5R 0402	Murata	GRM155R60G106ME44D	CS0402
10	1	C21	0	RES 0.0 OHM 1/20W JUMP 0201 SMD	Panasonic	ERJ-1GN0R00C	RS0201
11	1	C20	1.8PF	CAP CER 1.8PF 50V NP0 0201	Murata	GRM0335C1H1R8CA01D	CS0201
12		C18,C22	DNI				
13	3	FB1,FB2,FB3	BLM15AG121SN1	FERRITE,120 OHM @100MHz,0402	Murata	BLM15AG121SN1	FBS0402
14	1	L1	2.2uH	POWER INDUCTOR,2.2uH,20%,1250mA,0.22ohms,0603	Murata	LQM18PN2R2MFRL	LPS0603
15	2	L2,L5	3.3nH	INDUCTOR 3.3+/-0.2NH 750MA 0201	Murata	LQP03TN3N3C02D	LS0201
16	1	R1	261k	RES 261K OHM 1/10W 1% 0402 SMD	Panasonic	ERJ-2RKF2613X	RS0402
17	1	R2	6.8PF	CAP,CER,6.8pF,NPO,0402,50V	Murata	GRM1555C1H6R8CA01	CS0402
18	1	R3	301k	RES 301K OHM 1/10W 1% 0402 SMD	Panasonic	ERJ-2RKF3013X	RS0402
19	1	R4	0	RES 0.0 OHM 1/20W JUMP 0201 SMD	Panasonic	ERJ-1GN0R00C	RS0201
20	1	U1	ATWILC1000A-MU	IC, WiFi, 40QFN	Atmel	ATWILC1000A-MU	40QFN
21	1	U2	FT440Aa	1.5MHz, 600mA, Synchronous Step-Down Converter	FMD	FT440Aa	SOT23-5
22	1	U3	DNI				
23	1	Y1	26.000MHz	CRYSTAL 26MHZ 10PF SMD	Abracon	ABM10-26.000MHZ-D30-T3	4 SMD
24	1	PCB	-	ATWILC1000-MR110PA	Createk		
25	1	Shield	-	Metal Shield	Createk	NMI RF Shield rev1	

Revision A - Initial release to production

9. Host Interfaces

9.1 SPI Interface

9.1.1 Overview

When the module is configured for SPI mode by connecting the SDIO~_SPI_CFG pin to VDDIO, the ATWILC1000-MR110PA has a Serial Peripheral Interface (SPI) that operates as a SPI slave. The SPI interface can be used for control and for serial I/O of 802.11 data. The SPI pins are mapped as shown in Table 9-1. The SPI is a full-duplex slave-synchronous serial interface that is available immediately following reset when pin 10 (SPI_CFG) is tied to VDDIO.

Table 9-1. SPI Interface Pin Mapping

Pin #	SPI Function
10	CFG: Must be tied to VDDIO
16	SSN: Active low slave select
15	MOSI: Serial Data Receive
18	SCK: Serial Clock
17	MISO: Serial Data Transmit

When the SPI is not selected, i.e., when SSN is high, the SPI interface will not interfere with data transfers between the serial-master and other serial-slave devices. When the serial slave is not selected, its transmitted data output is buffered, resulting in a high impedance drive onto the MISO line.

The SPI interface responds to a protocol that allows an external host to read or write any register in the chip as well as initiate DMA transfers.

The SPI SSN, MOSI, MISO and SCK pins of the ATWILC1000-MR110PA have internal programmable pull-up resistors (see section 9.1). These resistors should be programmed to be disabled. Otherwise, if any of the SPI pins are driven to a low level while the ATWILC1000-MR110PA is in the low power sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module.

9.1.2 SPI Timing

The SPI timing is provided in Figure 9-1 and in Table 9-2 on page 13.

Figure 9-1. SPI Timing Diagram (SPI Mode CPOL=0, CPHA=0)

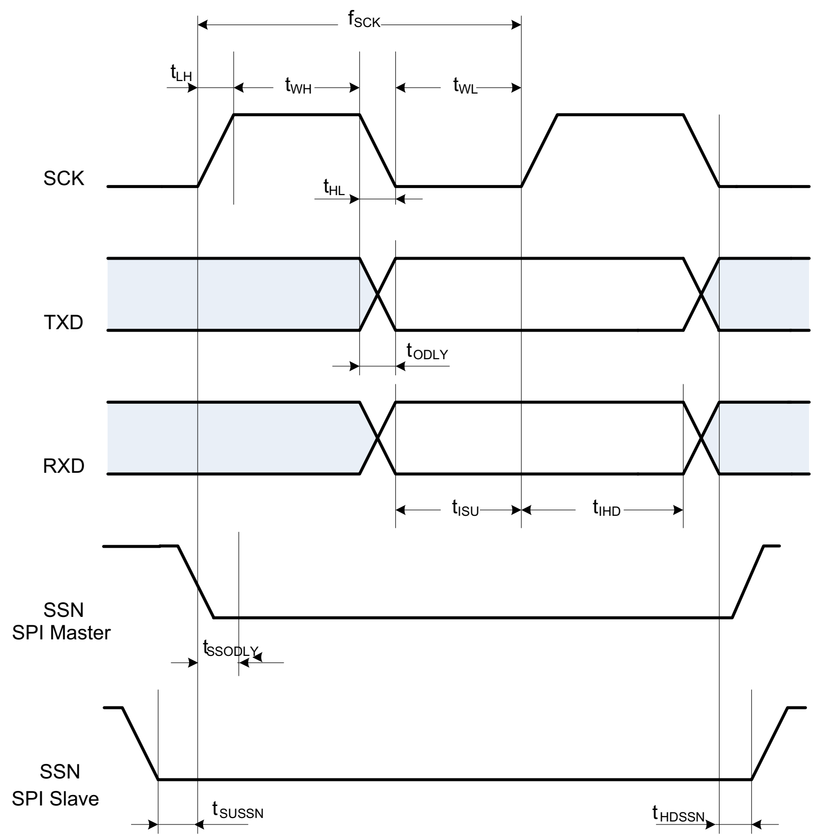


Table 9-2. SPI Slave Timing Parameters

Parameter	Symbol	Min	Max	Units
Clock input frequency	f_{SCK}		48	MHz
Clock low pulse width	t_{WL}	15		ns
Clock high pulse width	t_{WH}	15		ns
Clock rise time	t_{LH}		10	ns
Clock fall time	t_{HL}		10	ns
Input setup time	t_{ISU}	5		ns
Input hold time	t_{IHD}	5		ns
Output Delay	t_{ODLY}	0	20	ns
Slave select setup time	t_{SUSSN}	5		ns
Slave select hold time	t_{HDSSN}	5		ns

9.2 UART

When the module is configured for SPI mode by connecting the SDIO~_SPI_CFG pin to VDDIO, the ATWILC1000-MR110PA has a Universal Asynchronous Receiver / Transmitter (UART) interface available on pins J14 and J19. It can be used for control or data transfer if the baud rate is sufficient for a given application. The UART is compatible with the RS-232 standard, where NMC1000 operates as Data Terminal Equipment (DTE). It has a two-pin RXD/TXD interface.

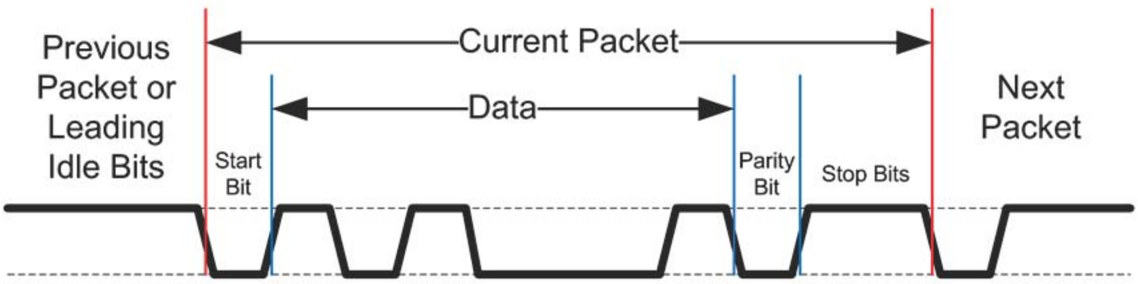
The UART features programmable baud rate generation with fractional clock division, which allows transmission and reception at a wide variety of standard and non-standard baud rates. The UART input clock is selectable between 10MHz, 5MHz, 2.5MHz, and 1.25MHz. The clock divider value is programmable as 13 integer bits and 3 fractional bits (with 8.0 being the smallest recommended value for normal operation). This results in the maximum supported baud rate of 10MHz / 8.0 = 1.25 MBd.

The UART can be configured for seven or eight bit operation, with or without parity, with four different parity types (odd, even, mark, or space), and with one or two stop bits. It also has Rx and Tx FIFOs, which ensure reliable high speed reception and low software overhead transmission. FIFO size is 4 x 8 for both Rx and Tx direction. The UART also has status registers showing the number of received characters available in the FIFO and various error conditions, as well the ability to generate interrupts based on these status bits.

An example of UART receiving or transmitting a single packet is shown in Figure 9-2. This example shows 7-bit data (0x45), odd parity, and two stop bits.

See the ATWILC1000-MR110PA Programming Guide for information on configuring the UART.

Figure 9-2. Example of UART Rx or Tx Packet



9.3 SDIO Interface

When the module is configured for SDIO mode by connecting the SDIO~_SPI_CFG pin to Ground, the ATWILC1000-MR110PA has a SDIO interface. The SDIO interface can be used for control and for serial I/O of 802.11 data. The SDIO pins are mapped as shown in Figure 9-3. The SDIO interface is available immediately following reset when pin 10 (SPI_CFG) is tied to ground.

The ATWILC1000-MR110PA SDIO is a full speed interface. The interface supports the 1-bit/4-bit SD transfer mode at the clock range of 0-50MHz. The Host can use this interface to read and write from any register within the chip as well as configure the ATWILC1000-MR110PA for data DMA.

Table 9-3. SDIO Interface Pin Mapping

Pin #	SDIO Function
10	CFG: Must be tied to ground
14	DAT3: Data 3
15	DAT2: Data 2
16	DAT1: Data 1
17	DAT0: Data 0
18	CMD: Command
19	CLK: Clock

When the SDIO card is inserted into an SDIO aware host, the detection of the card will be via the means described in SDIO specification. During the normal initialization and interrogation of the card by the host, the card will identify itself as an SDIO device. The host software will obtain the card information in a tuple (linked list) format and determine if that card's I/O function(s) are acceptable to activate. If the card is acceptable, it will be allowed to power up fully and start the I/O function(s) built into it.

The SD memory card communication is based on an advanced 9-pin interface (Clock, Command, 4 Data and 3 Power lines) designed to operate at maximum operating frequency of 50MHz.

9.3.1 Features

- Meets SDIO card specification version 2.0.
- Host clock rate variable between 0 and 50 MHz
- 1 bit/4-bit SD bus modes supported
- Allows card to interrupt host
- Responds to Direct read/write (IO52) and Extended read/write (IO53) transactions.
- Supports Suspend/Resume operation.

9.3.2 SDIO Timing

Figure 9-3. SDIO Timing Diagram

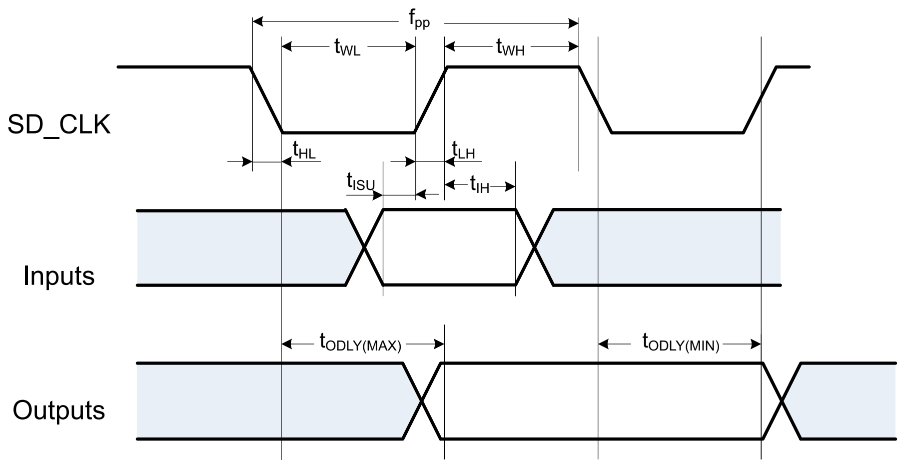


Table 9-4. SDIO Timing Parameters

Parameter	Symbol	Min.	Max.	Unit
Clock Input Frequency	f_{PP}	0	50	MHz
Clock Low Pulse Width	t_{WL}	10		ns
Clock High Pulse Width	t_{WH}	10		ns
Clock Rise Time	t_{LH}		10	ns
Clock Fall Time	t_{HL}		10	ns
Input Setup Time	t_{ISU}	5		ns
Input Hold Time	t_{IH}	5		ns
Output Delay	t_{ODLY}	0	14	ns

9.4 I^{2}C Interface

ATWILC1000-MR110PA provides an I2C bus slave that allows the host processor to read or write any register in the chip. ATWILC1000-MR110PA supports I2C bus Version 2.1 - 2000.

The I^{2}C interface, used primarily for debug, is a two-wire serial interface consisting of a serial data line (SDA, Pin 17) and a serial clock (SCL, Pin 18). It responds to the seven bit address value 0x60. The ATWILC1000-MR110PA I2C interface can operate in standard mode (with data rates up to 100 Kb/s) and fast mode (with data rates up to 400 Kb/s).

The I^{2}C is a synchronous serial interface. The SDA line is a bidirectional signal and changes only while the SCL line is low, except for STOP, START, and RESTART conditions. The output drivers are open-drain to perform wire-AND functions on the bus. The maximum number of devices on the bus is limited by only the maximum capacitance specification of 400pF. Data is transmitted in byte packages.

For specific information, please refer to the Philips Specification entitled “The I^{2}C -Bus Specification, Version 2.1”.

9.4.1 I^{2}C Timing

The I^{2}C timing is provided in Figure 9-4 and Table 8-5.

Figure 9-4. I^{2}C Timing Diagram

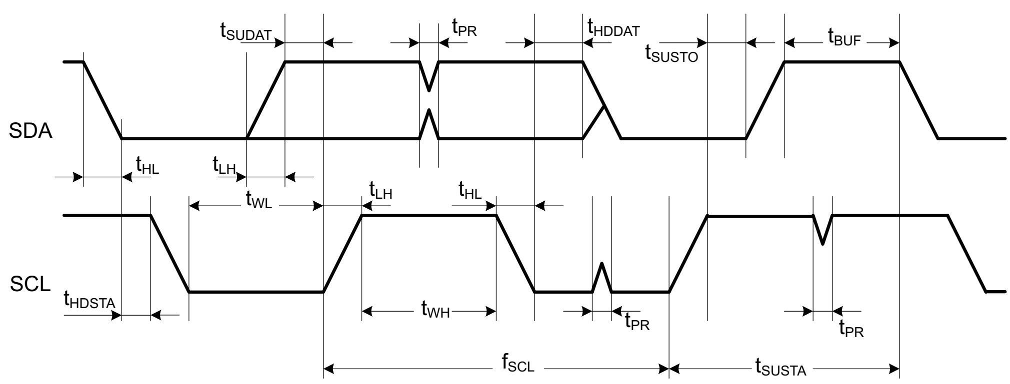
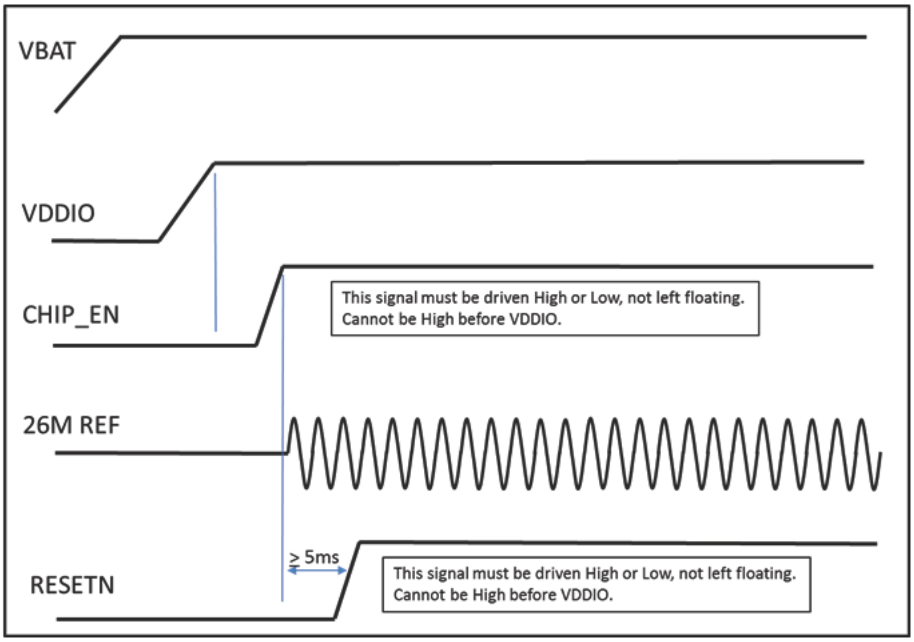


Table 9-5. I^2C Timing Parameters

Parameter	Symbol	Min.	Max.	Unit	Remarks
SCL Clock Frequency	f_{SCL}	0	400	kHz	
SCL Low Pulse Width	t_{WL}	1.3		µs	
SCL High Pulse Width	t_{WH}	0.6		µs	
SCL, SDA Fall Time	t_{HL}		300	ns	
SCL, SDA Rise Time	t_{LH}		300	ns	This is dictated by external components
START Setup Time	t_{SUSTA}	0.6		µs	
START Hold Time	t_{HDSTA}	0.6		µs	
SDA Setup Time	t_{SUDAT}	100		ns	
SDA Hold Time	t_{HDDAT}	0 40		ns ns	Slave and Master Default Master Programming Option
STOP Setup time	t_{SUSTO}	0.6		µs	
Bus Free Time Between STOP and START	t_{BUF}	1.3		µs	
Glitch Pulse Reject	t_{PR}	0	50	ns	

9.5 Host Interface Power-up Sequence Timing Diagram

Figure 9-5. Host Interface Power up Sequence Timing Diagram



10. Notes On Interfacing To The ATWILC1000-MR110PA

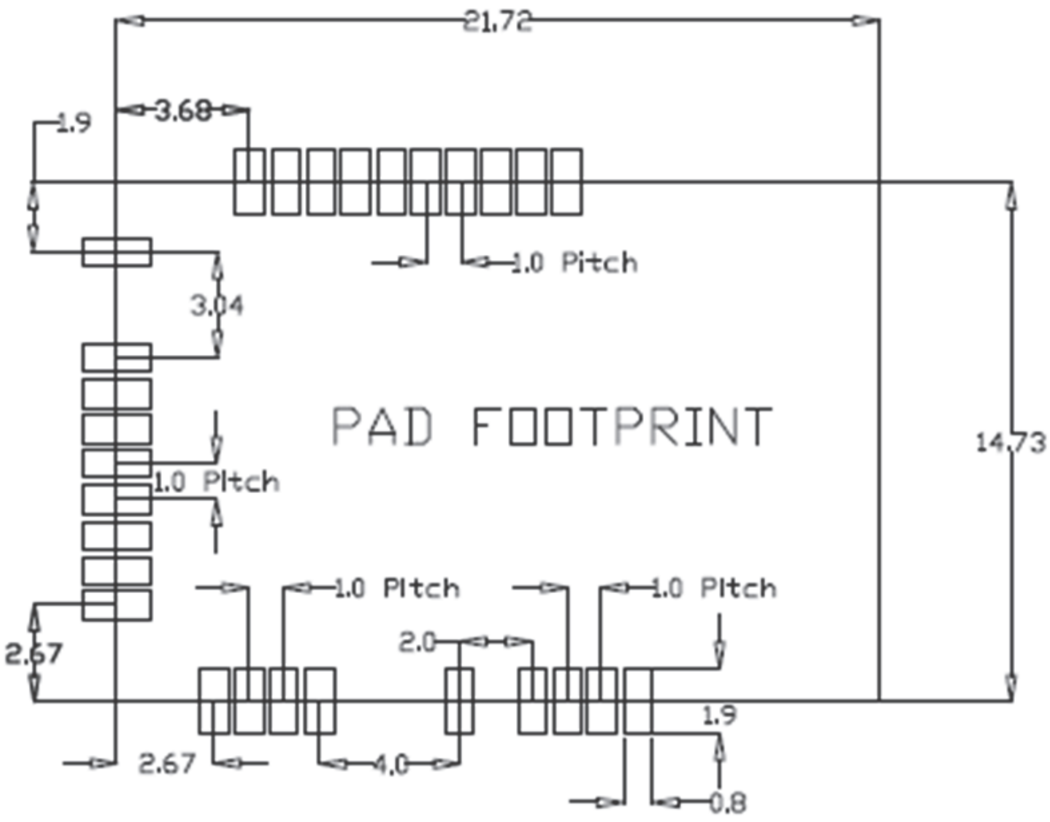
10.1 Programmable Pull Up Resistors

The ATWILC1000-MR110PA provides programmable pull-up resistors on various pins. The purpose of these resistors is to keep any unused input pins from floating which can cause excess current to flow through the input buffer from the VDDIO supply. Any unused module pin on the ATWILC1000-MR110PA should leave these pull-up resistors enabled so the pin will not float. The default state at power up is for the pull-up resistor to be enabled. However, any pin which is used should have the pull-up resistor disabled. The reason for this is that if any pins are driven to a low level while the ATWILC1000-MR110PA is in the low power sleep state, current will flow from the VDDIO supply through the pull-up resistors, increasing the current consumption of the module. Since the value of the pull-up resistor is approximately 100K ohms, the current through any pull-up resistor that is being driven low will be VDDIO/100K. For VDDIO = 3.3V, the current through each pull-up resistor that is driven low would be approximately 3.3V/100K = 33µA. Pins which are used and have had the programmable pull-up resistor disabled should always be actively driven to either a high or low level and not be allowed to float.

See the ATWILC1000-MR110PA Programming Guide for information on enabling/disabling the programmable pull up resistors.

11. Recommended Footprint (Unit: mm)

Figure 11-1. Footprint Drawing

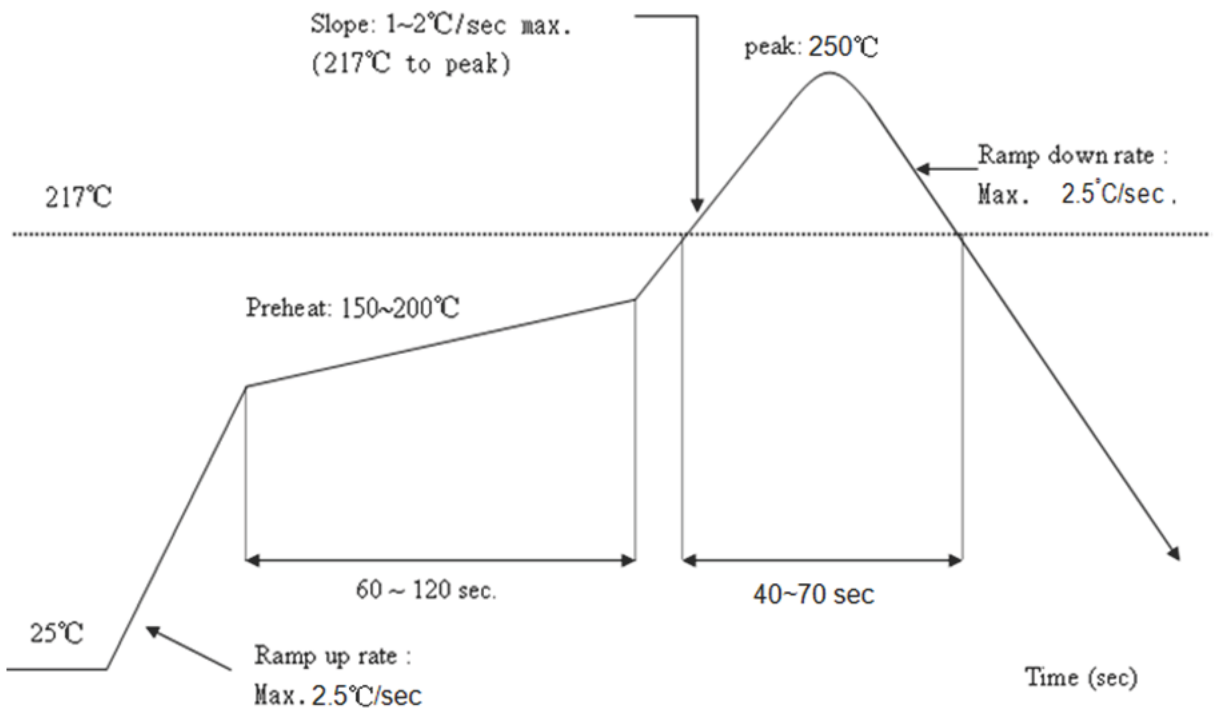


12. Recommended Reflow Profile

Referred to IPC/JEDEC standard. Peak Temperature: <250°C

Number of times: 2 times maximum

Figure 12-1. Typical Reflow Profile



13. Application Schematic

Figure 13-1. SDIO Application Schematic

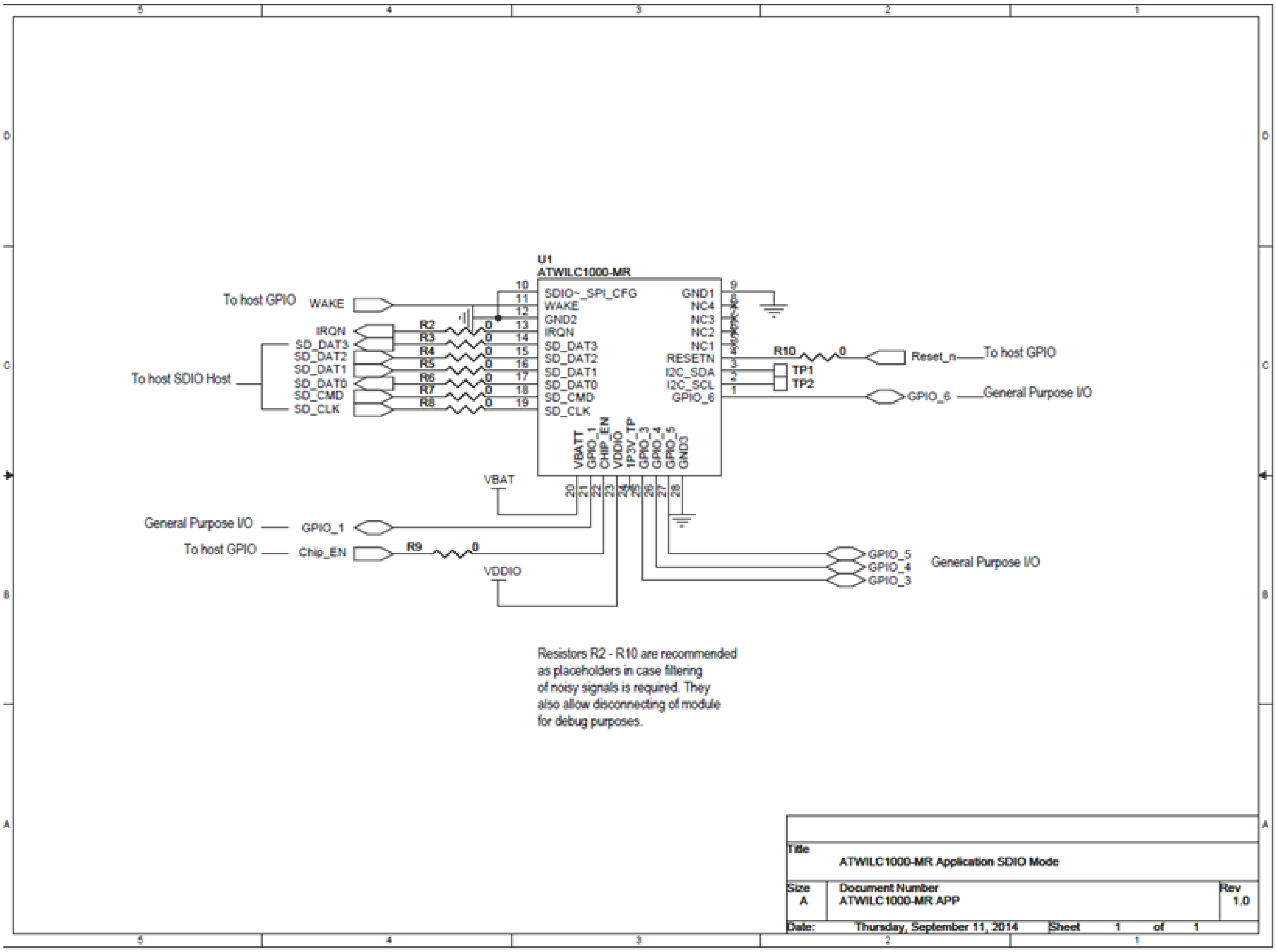
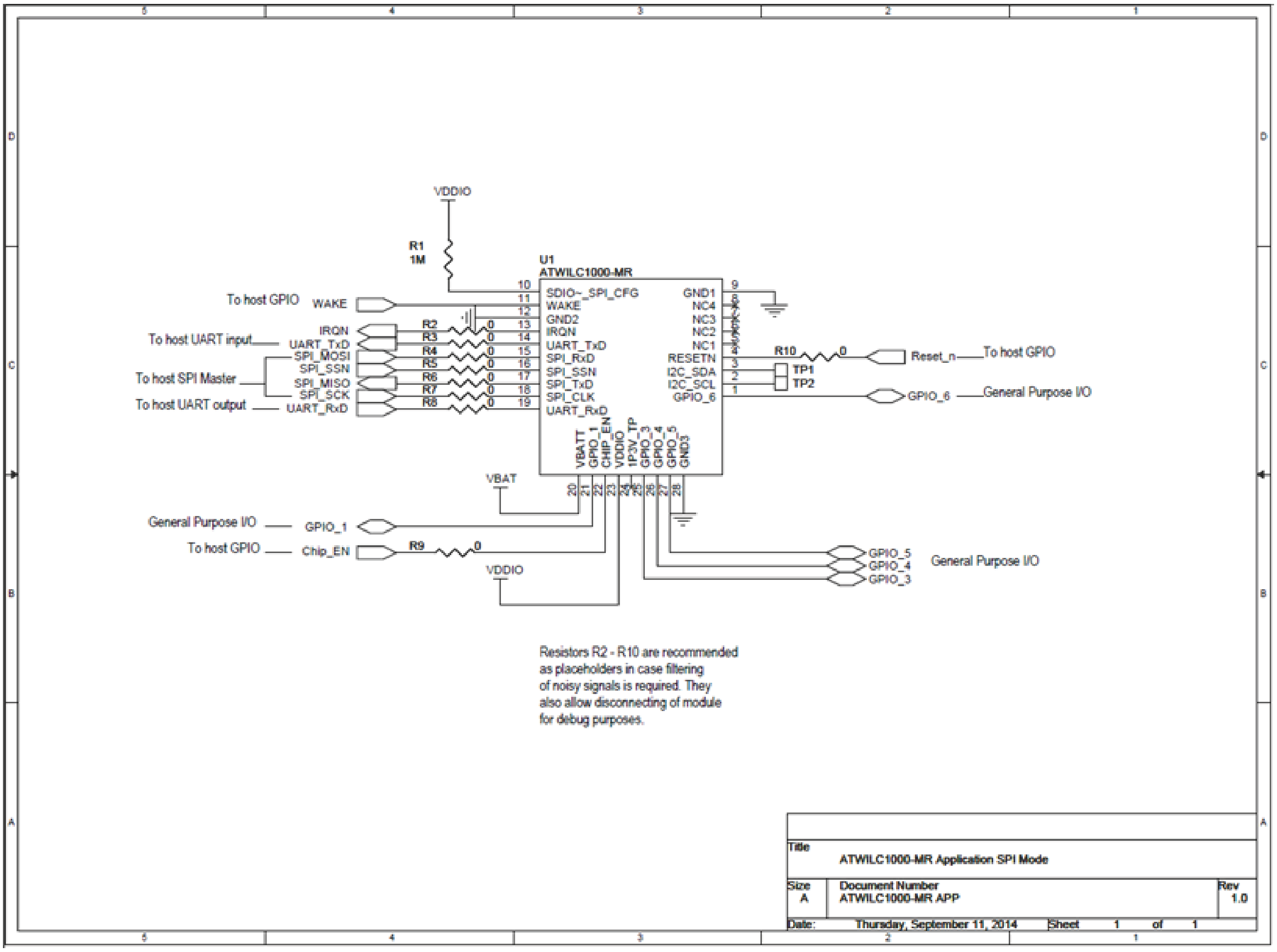


Figure 13-2. SPI Application Schematic



14. Technical Support and Resources

For technical support and other resources visit: http://www.atmel.com/design-support

15. Revision History

Doc. Rev.	Date	Comments
42380B	10/2014	Product name corrected from ATWILC1000-MR110P to ATWILC1000-MR110PA.
42380A	10/2014	Initial document release.

Atmel Corporation 1600 Technology Drive, San Jose, CA 95110 USA **T:** (+1)(408) 441.0311 **F:** (+1)(408) 436.4200 | **www.atmel.com**

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