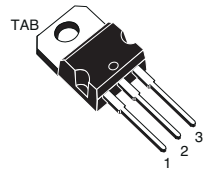
STP110N55F6

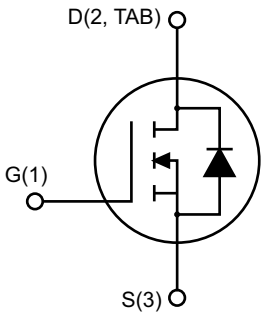
N-channel 55 V, 4.5 Ω typ., 110 A STripFET™ F6 Power MOSFET in a TO-220 package

Datasheet - production data



TO-220

Figure 1. Internal schematic diagram



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STP110N55F6	55 V	5.2 mΩ	110 A

- Low gate charge
- Very low on-resistance
- High avalanche ruggedness

Applications

- Switching applications

Description

This device is an N-channel Power MOSFET developed using the STripFET™ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits a very low $R_{DS(on)}$ in all packages.

Table 1. Device summary

Order code	Marking	Packages	Packaging
STP110N55F6	110N55F6	TO-220	Tube

Contents

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	55	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at T_C = 25 °C	110	A
I_D	Drain current (continuous) at T_C = 100 °C	85	A
I_{DM} (1)	Drain current (pulsed)	440	A
P_{TOT}	Total dissipation at T_C = 25 °C	150	W
	Derating factor	1	W/°C
T_{stg}	Storage temperature	- 55 to 175	°C
T_j	Operating junction temperature		

1. Current limited by package.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj\text{-}case}$	Thermal resistance junction-case max	1	°C/W
$R_{thj\text{-}amb}$	Thermal resistance junction-ambient max	62.5	°C/W

2 Electrical characteristics

(T_{CASE} = 25 °C unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0, I_D = 250 µA	55			V
I_{DSS}	Zero gate voltage Drain current	V_{GS} = 0, V_{DS} = 55 V			1	µA
		V_{GS} = 0, V_{DS} = 55 V, T_C=125 °C			100	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = ± 20 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	2		4	V
$R_{DS(on)}$	Static drain-source on- resistance	V_{GS} = 10 V, I_D = 60 A		4.5	5.2	mΩ

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{GS} = 0, V_{DS} = 25 V, f = 1 MHz	-	7390	-	pF
C_{oss}	Output capacitance		-	504	-	pF
C_{rss}	Reverse transfer capacitance		-	355	-	pF
Q_g	Total gate charge	V_{DD} = 44 V, I_D = 110 A, V_{GS} = 10 V *(see Figure 14)*	-	126	-	nC
Q_{gs}	Gate-source charge		-	32	-	nC
Q_{gd}	Gate-drain charge		-	38	-	nC

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 27.5 V, I_D = 55 A R_G = 4.7 Ω V_{GS} = 10 V *(see Figure 13)*	-	23	-	ns
t_r	Rise time		-	65	-	ns
$t_{d(off)}$	Turn-off-delay time		-	503	-	ns
t_f	Fall time		-	237	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
I_{SD}	Source-drain current		-		110	A
I_{SDM} (1)	Source-drain current (pulsed)		-		440	A
V_{SD} (2)	Forward on voltage	I_{SD} = 110 A, V_{GS} = 0	-		1.5	V
t_{rr}	Reverse recovery time	I_{SD} = 110 A, V_{DD} = 44 V di/dt = 100 A/µs, T_j = 150 °C *(see Figure 15)*	-	44		ns
Q_{rr}	Reverse recovery charge		-	82		nC
I_{RRM}	Reverse recovery current		-	3.8		A

1. Current limited by package.
2. Pulsed: pulse duration = 300 µs, duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

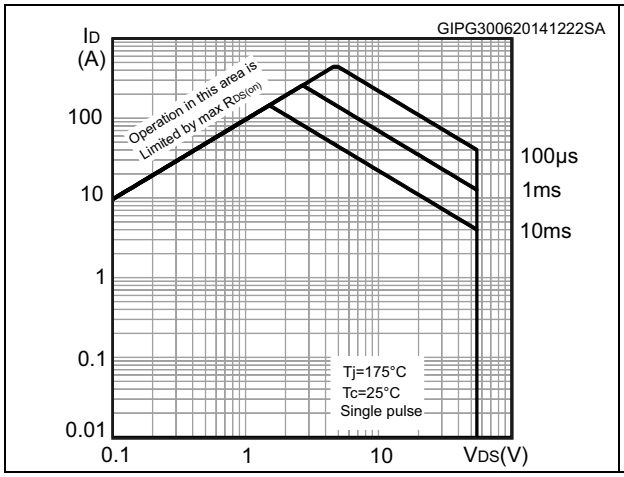


Figure 3. Thermal impedance

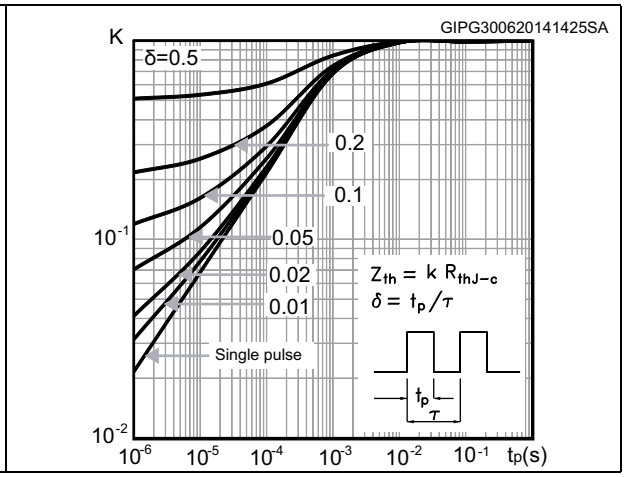


Figure 4. Output characteristics

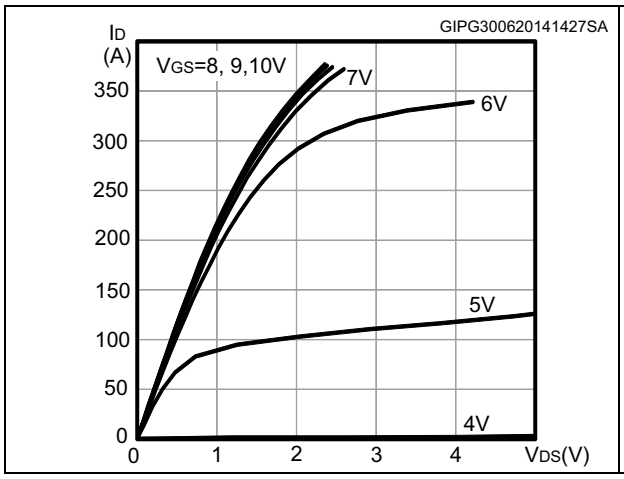


Figure 5. Transfer characteristics

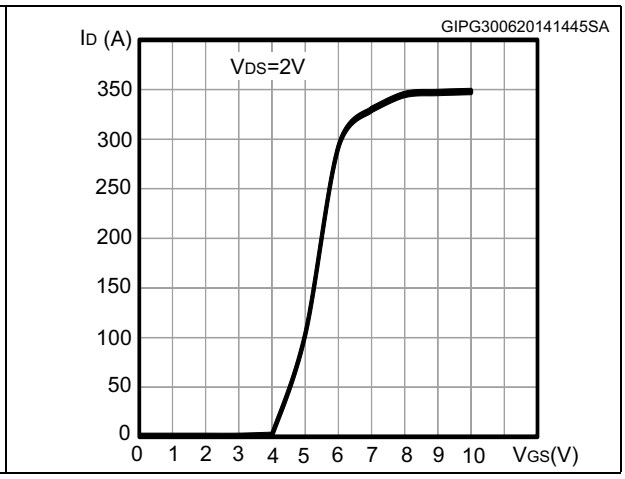


Figure 6. Gate charge vs gate-source voltage

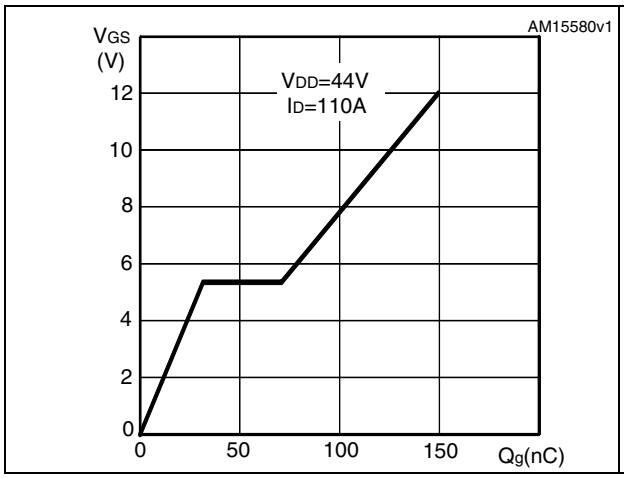


Figure 7. Static drain-source on-resistance

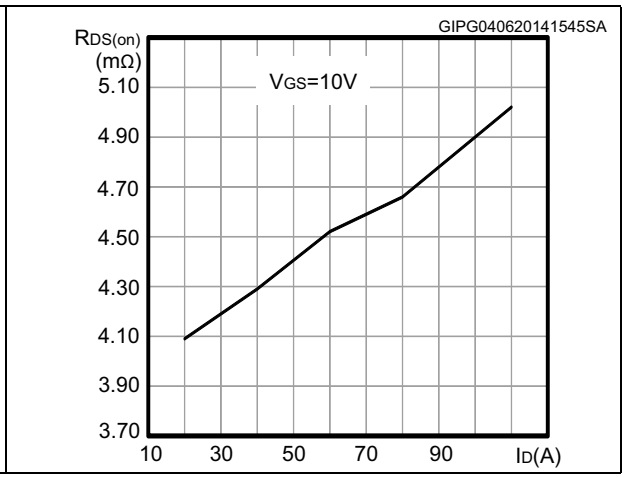


Figure 8. Capacitance variations

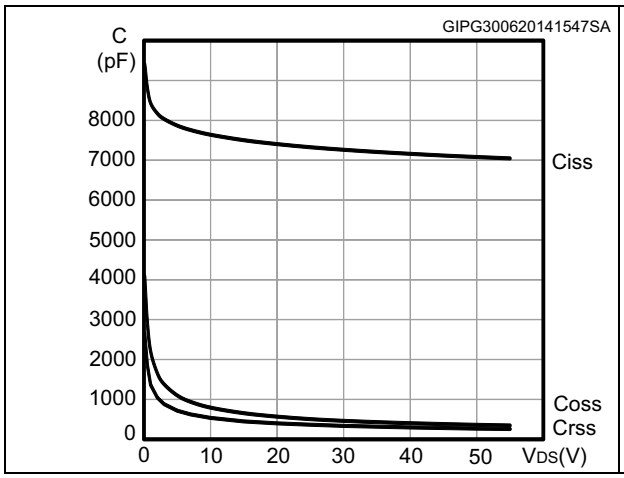


Figure 9. Normalized gate threshold voltage vs temperature

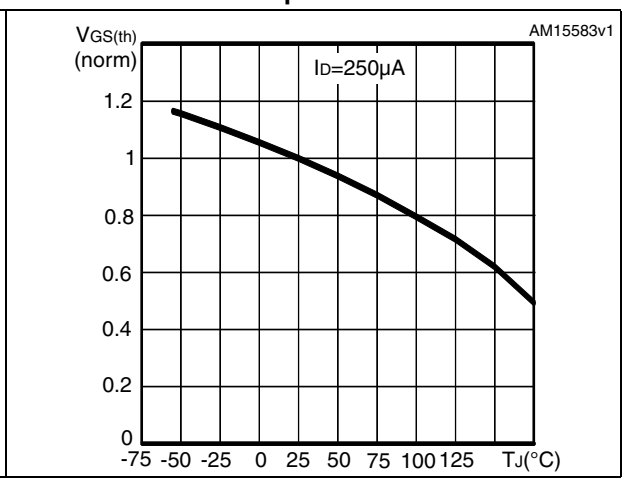


Figure 10. Normalized on-resistance vs temperature

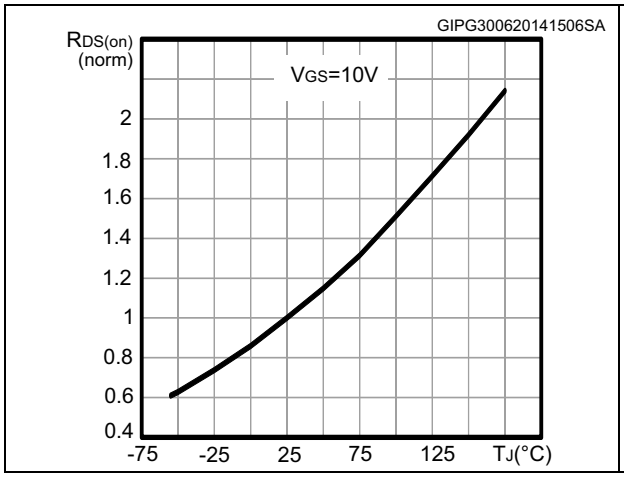


Figure 11. Source-drain diode forward characteristics

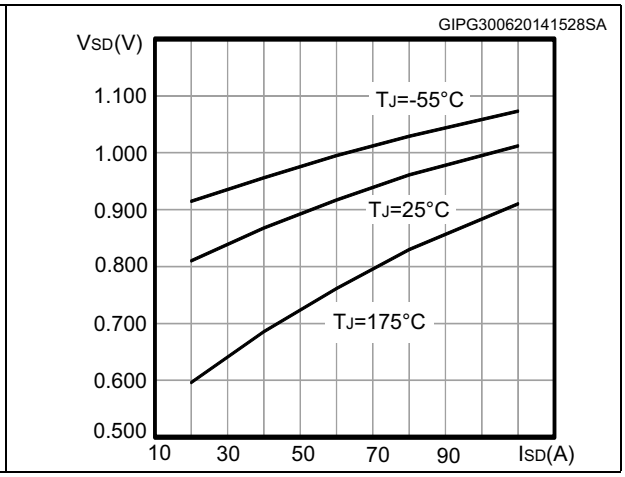
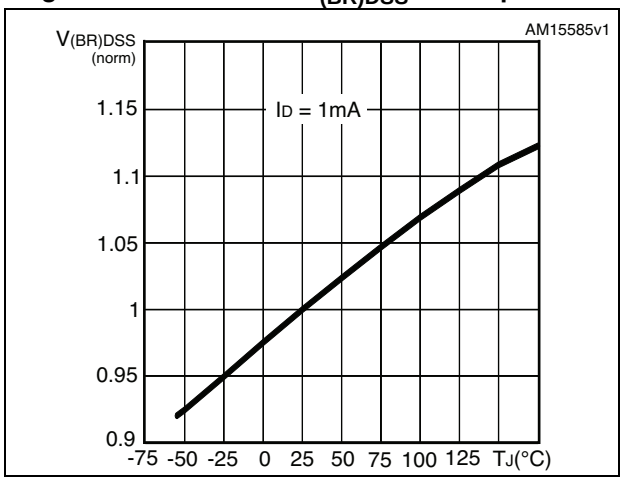


Figure 12. Normalized $V_{(BR)DSS}$ vs temperature



3 Test circuits

Figure 13. Switching times test circuit for resistive load

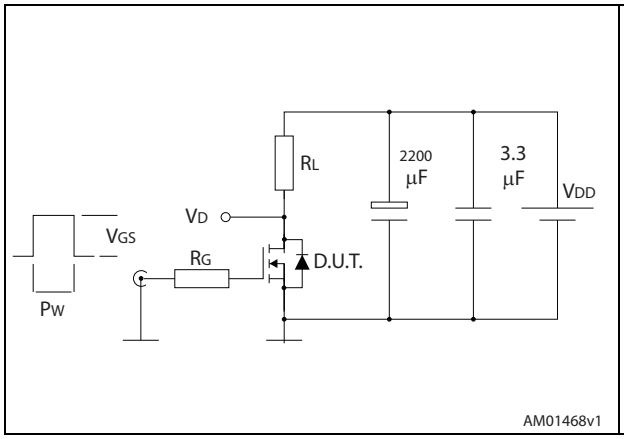


Figure 14. Gate charge test circuit

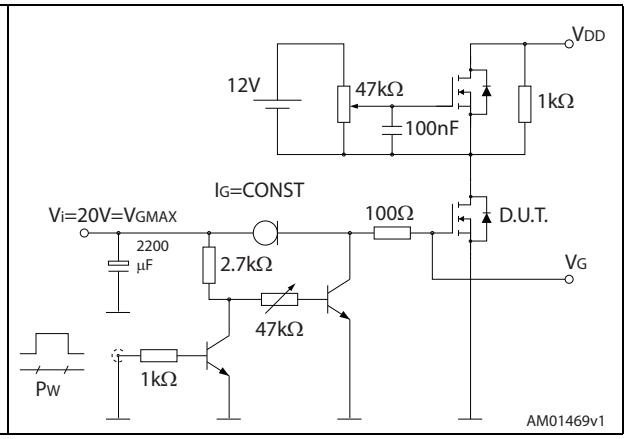


Figure 15. Test circuit for inductive load switching and diode recovery times

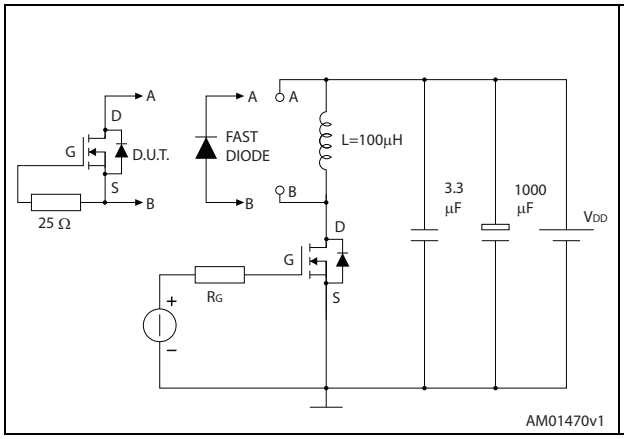


Figure 16. Unclamped inductive load test circuit

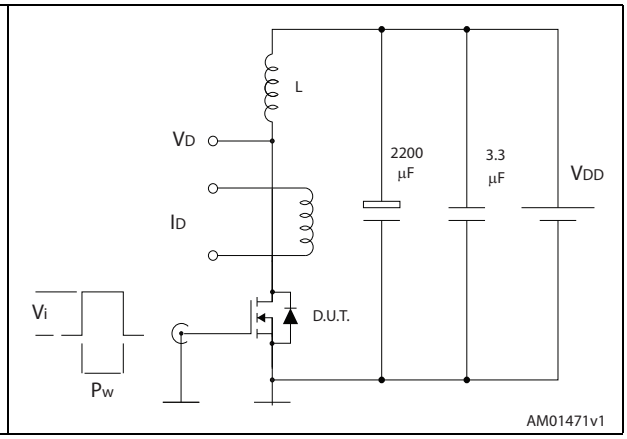


Figure 17. Unclamped inductive waveform

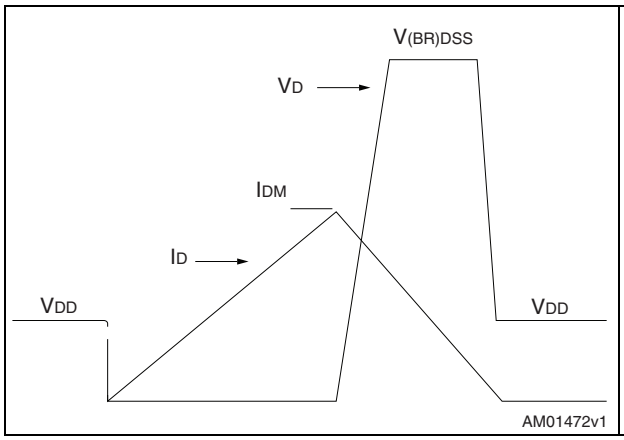
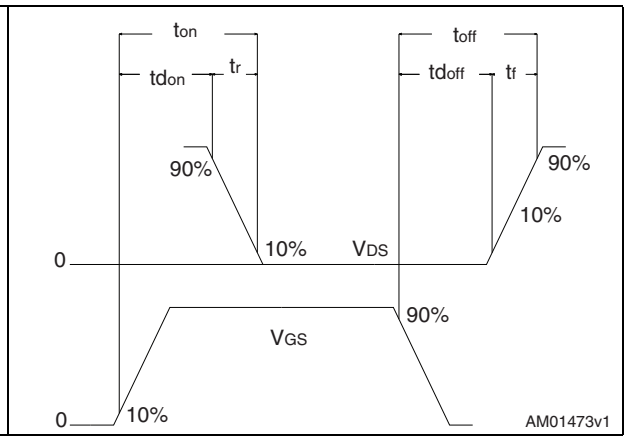


Figure 18. Switching time waveform



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.
ECOPACK is an ST trademark.

Figure 19. TO-220 type A drawing

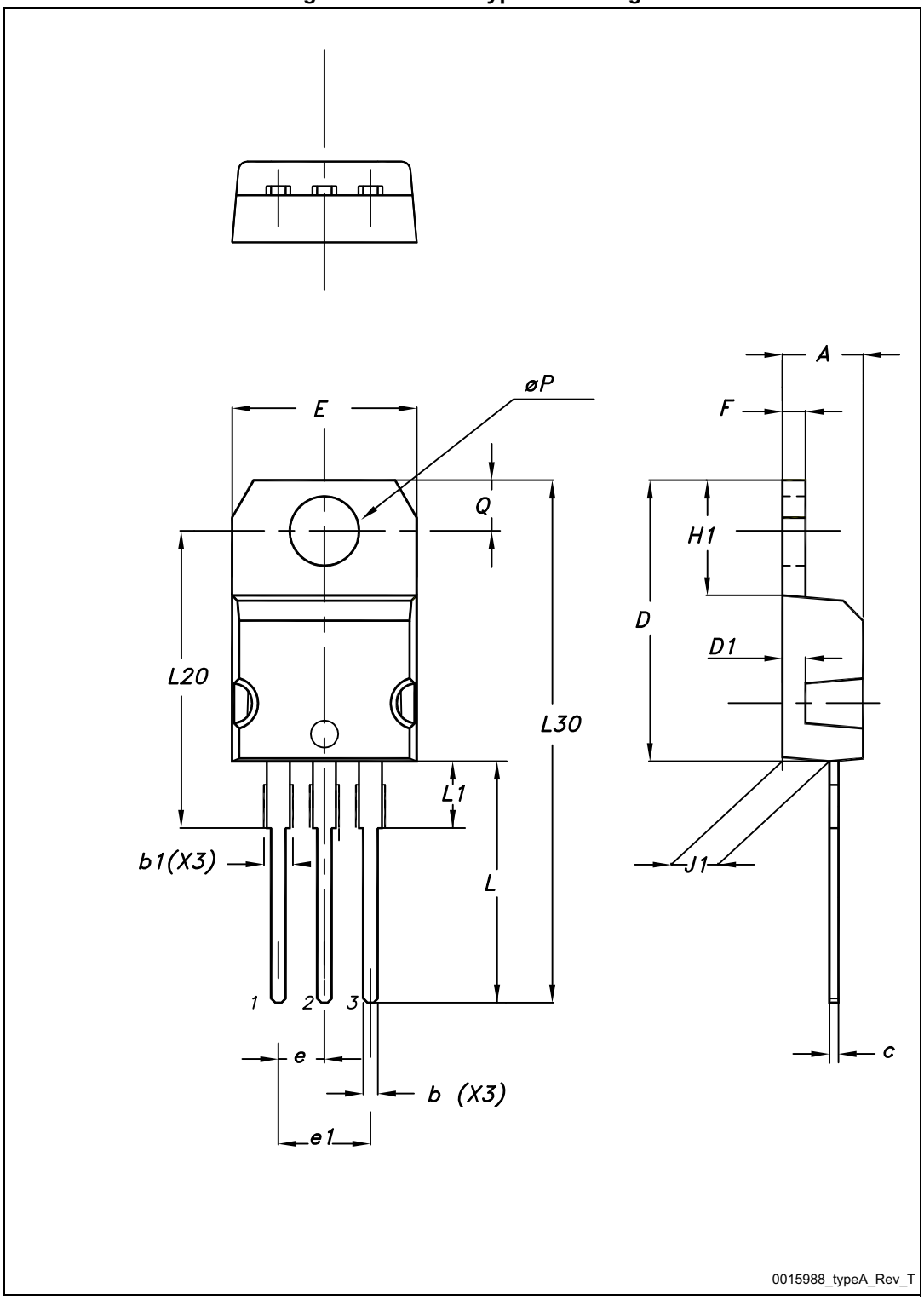


Table 8. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
øP	3.75		3.85
Q	2.65		2.95

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
18-Jul-2011	1	First release.
11-Jul-2014	2	– Modified: title and *Description* – Modified: I_D (at T_C = 100 °C) value in *Table 2* – Modified: $R_{DS(on)}$ typical value – Modified: the entire typical values in *Table 5*, *6* and *7* – Added: *Section 2.1: Electrical characteristics (curves)* – Updated: *Section 4: Package mechanical data* – Minor text changes