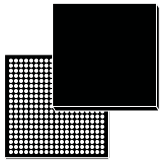
STA1095

Accordo2 dual core processor for car radio and display audio applications

Data brief



LFBGA361
(16x16x1.7, 0.8mm pitch)

GAPGPS00902

Features

Core and infrastructure

- ARM® Cortex™-R4 MCU
- Embedded SRAM
- SDRAM controller
- Serial QIO NOR interface executable in place
- Parallel NAND/NOR controller

Audio subsystem

- Sound processing DSPs
- 1x 6 stereo channels hardware Sample Rate Converter
- 6x audio DAC
- Digital audio interfaces (I2S/ multichannel ports)
- 1x single ended stereo ADC with internal switching logic
- 1x differential Mono ADC with internal switching logic

Media interfaces

- Secure-Digital Multimedia Memory Card Interfaces
- USB 2.0 Interfaces
- SPDIF with CDROM block decoder support

Display subsystem

- TFT controller
- Touch Screen Controller
- Video Input Port
- Graphics Processing Unit

Embedded secure CAN subsystem

- Dedicated ARM Cortex-M3 core
- Isolated embedded memory
- CAN ports
- Secured NOR interface

I/O interfaces

- General purpose ADCs
- I2C multi-master/slave interfaces
- UART Controllers
- Synchronous Serial Ports (SSP/SPI)
- GPIOs
- JTAG

Operating conditions

- VDD: 1.14V - 1.26V
- VDDIO: 3.3V ±10%
- VDDIOON: 3.3V ±10%,
- Ambient temperature range: -40 / +85°C

Table 1. Device summary

Order code	Package	Packing
STA1095	LFBGA361 (16x16x1.7, 0.8mm pitch)	Tray

Contents

1 Description

STA1095 is a device that provides a cost effective microprocessor solution for modern automotive car radio systems, with an embedded powerful Digital Sound Processing subsystem, as well as a MIPS efficient ARM Cortex-R4 processor.

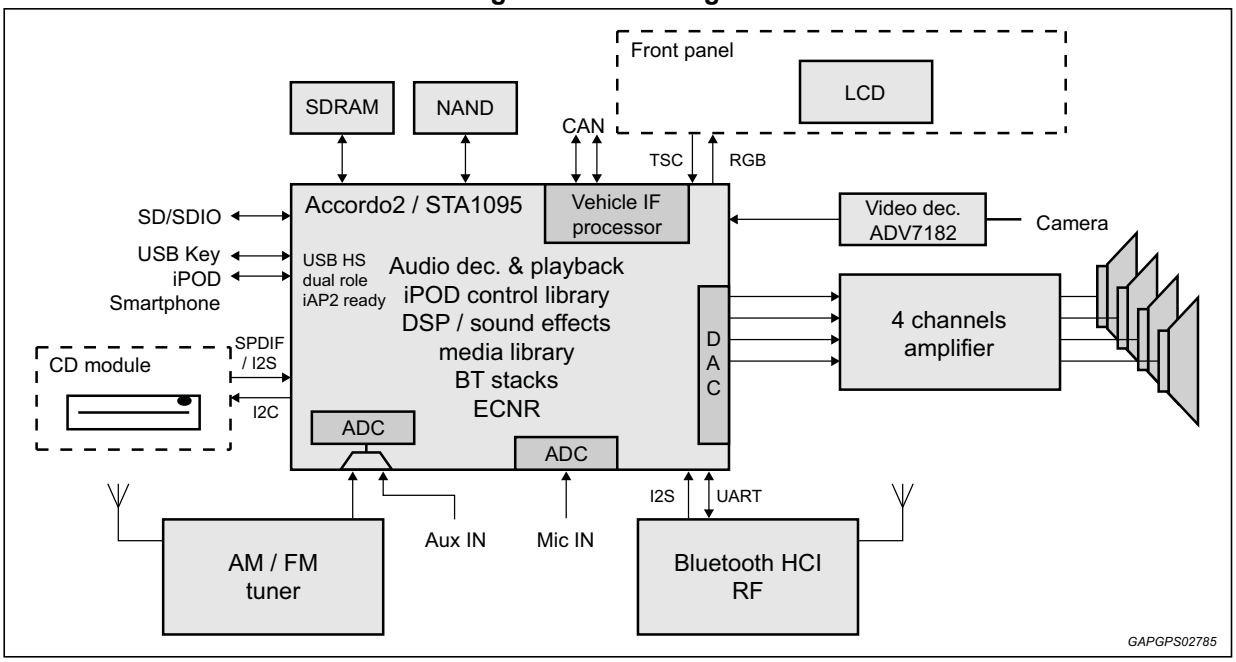
In addition, an ARM Cortex-M3 controller is dedicated for real-time CAN / Vehicle Interface Processing.

In terms of peripherals, STA1095 comes with an exhaustive set of common interfaces (UART/I2S/I2C/USB/MMC) which make the device optimal for implementing a feature rich system as well as a cost effective solution.

The solution is bundled with a complete software package, which allows a very fast system implementation.

STA1095 manages the entire audio chain from analog or digital inputs to analog or digital outputs, including digital audio media decoding, sample rate conversion among various sources, intelligent routing and audio effects / DSP post processing. With its flexible memory configuration, it allows implementing from very low cost systems based on real time OS, scaling up to demanding applications based on Linux OS.

Figure 1. Block diagram



2 System description

2.1 Processor MCU

STA1095 processing capability relies on an ARM Cortex-R4. The MCU has instruction cache and data cache, as well as TCM Memory dedicated respectively to instructions and data for high throughput and low latency tasks.

2.2 Memory controller

2.2.1 Embedded memory

STA1095 embeds SRAM memory, which can be used for data or code storage.

Embedded memory can be used in conjunction with executable in place NOR devices to implement cost effective solutions. The whole embedded memory is also cacheable and can be accessed by DMA.

2.2.2 SDRAM controller

SDRAM controller supports SDRAM JEDEC interface 16 or 32 bits wide, which allows interfacing to automotive SDRAM memory devices to handle high footprint applications.

Such memory is cacheable, and can be accessed by DMA.

2.2.3 SQI executable in place

The SQIO controller allows interfacing Serial Quad I/O flash memories.

2.2.4 Parallel memory interface

FSMC static memory controller, provides a generic parallel interface suitable to connect to NOR devices as well as SRAM and NAND devices. This peripheral allows execution in-place from NOR/SRAMs, as well as DMA accesses.

NOR memory space can be partitioned so to reserve a portion of the parallel NOR device to the Secure CAN Subsystem.

2.3 USB

STA1095 has one USB HS interfaces with embedded phy, allowing to efficiently connect to mass storage devices, as well as portable devices (phones, pads). Along with USB connectivity, STA1095 fully supports USB charger specification.

2.4 Sound subsystem

STA1095 implements a sound subsystem which allows to efficiently handle sound processing tasks, such as spatialization and equalizer, without loading the main CPU with interrupt intensive tasks.

2.4.1 Audio interfaces

A complete set of audio interfaces is provided, in order to simplify integration with amplifiers, and input sources. Each interface can be routed to the sound subsystem. A complete list of audio interfaces is provided below:

- Audio ADC
  - Shared between AUX LINE and TUNER LINE
  - ADC Inputs are single ended 3.3 V
- Voice ADC
  - Shared among Voice and TEL-IN lines with embedded multiplexer
  - Both Mic and Tel-In lines are differential inputs
- Stereo DAC
- Multiple I2S IN
- Multiple I2S OUT
- SPDIF IN for CD/CDROM input with Hardware Block Decoder for CDROM error correction.

2.4.2 Routing and sample rate converters

Each audio interface can be routed in both directions (IN/OUT) through hardware sample rate converters, which allow normalizing the sampling rate to the sound processing engine. The audio routing infrastructure is designed to deliver high quality sample rate conversion on multiple channels, allowing simultaneous audio streams, such as Bluetooth® Hands Free and audio media playback, to be handled without CPU load.

2.4.3 Sound DSP

STA1095 is equipped with multiple DSPs dedicated to sound processing, fully integrated with the sound subsystem with a specific isochronous bus. DSP is provided with an integrated sound processing library implementing effects like spatialization, balancing and equalizer, etc..

2.5 SD/MMC

STA1095 is equipped with SDMMC controllers, which allow interfacing to either mass storage devices, or to Wi-Fi modules.

2.6 DMA

DMA is designed to efficiently perform memory to memory, and memory to peripherals transfers, offloading such tasks from the processor, thus reducing interrupt handling load. DMA provides independent channels which can be dynamically assigned to different data-path. Complex Scatter/gather transfers can be implemented by programming specific DMA command linked lists.

2.7 Secure CAN Subsystem

STA1095 allows isolating critical code from main application by implementing a dedicated subsystem based on ARM Cortex-M3, along with:

256KB dedicated embedded SRAM

- Dedicated embedded SRAM
- CAN controller
- Dedicated GPIOs

In order to guarantee security of CAN network, it can be completely isolated from the rest of the system, in such a way that no application running on Cortex-R4 can access by any mean to CAN specific resources. The secure sub-system communicates with the application running on Cortex-R4 using a Hardware Mailbox interrupt based mechanism.

2.8 General Purpose ADC

STA1095 has general purpose ADCs with a resolution of 10-bits.

2.9 GPIOs

STA1095 has GPIOs which can be independently configured either as INPUT or OUTPUT. In order to make the system flexible, these IOs are multiplexed on PINs with other peripherals.

2.10 Generic Interfaces

2.10.1 UARTS

- Programmable baud rates up to3Mbps
- Hardware Flow control
- DMA capable.

2.10.2 I^2Cs

- Master/slave modes in multi-master environment
- Multiple baud rates supported: 100/400/1000/3400 Kbits/s
- DMA capable

2.10.3 SSP/SPI ports supporting

- Motorola SPI-compatible interface
- Texas Instrument synchronous serial interface
- National Semiconductor MICROWIRE® interface
- Unidirectional interface
- DMA capable

2.11 Video input port

The Video Input Port (VIP) allows to grab images from external devices, supporting parallel interface. VIP supports both interlaced and progressive modes.

The VIP is synchronized with display controller to prevent from tearing effects, and is used in conjunction with GPU to implement on the fly color conversion and bilinear interpolated re-scaling.

2.12 Smart graphics accelerator (GPU)

The aim of the Smart Graphic Accelerator (SGA) is to provide an efficient 2D and 3D primitive drawing tool that breaks down the MIPS and power consumption concerns of pixel processing.

It supports:

- Control and synchronization features
- 2D-Graphics features
- Video Overlay features
- 3D Graphics features

2.13 Display controller

The main features of the LCD Controller are:

- Supports single and dual panel monochrome STN displays with 4 or 8 bits interfaces
- Supports single and dual panel color STN displays with 8 bits interfaces
- Supports TFT color displays
- Supports AD-TFT and HR-TFT color displays
- Programmable timing for different display panels

2.14 Touch screen controller

4-wire Touch Screen Controller and a 8bit - input ADC. The Touch Screen Controller is enhanced with a movement tracking algorithm.

3 Package Information

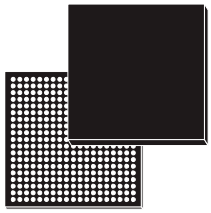
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*.

ECOPACK® is an ST trademark.

Figure 2. LFBGA361 mechanical data and package dimensions

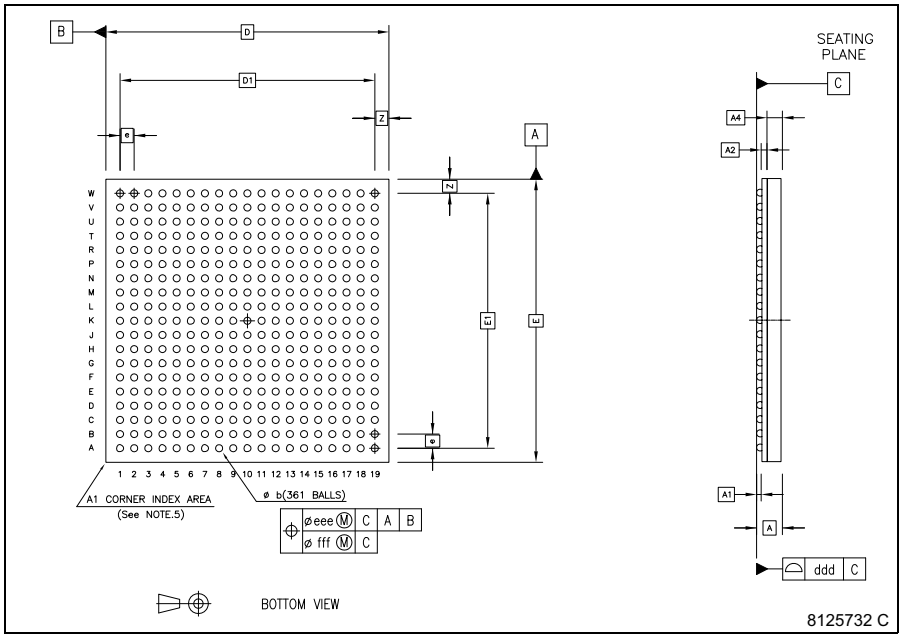
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.7			0.0669
A1	0.25			0.0098		
A2		0.3			0.0118	
A4			0.8			0.0315
b	0.35	0.40	0.48	0.0138	0.0157	0.0189
D	15.85	16.000	16.150	0.6240	0.6299	0.6358
D1		14.4			0.5669	
E	15.85	16.0	16.150	0.6240	0.6299	0.6358
E1		14.4			0.5669	
e		0.8			0.0315	
Z		0.8			0.0315	
ddd			0.1			0.0039
eee			0.15			0.0059
fff			0.08			0.0031

OUTLINE AND MECHANICAL DATA



Body: 16 x 16 x 1.7mm

LFBGA361
Low profile Fine Pitch Ball Grid Array



GAPGPS00954

4 Revision history

Table 2. Document revision history

Date	Revision	Changes
23-Oct-2014	1	Initial release.
27-Oct-2014	2	Modified the title in cover page.