Features

- **High Sensitivity and High SNR Performance Linear CCD**
- **1024, 2048 or 4096 Resolution with 10 µm Square Pixels**
- **512, 1024 or 2048 Resolution with 14 µm Square Pixels**
- **100% Aperture, Built-in Anti-blooming, No Lag**
- **CameraLink Data Format (Base Configuration)**
- **High Data Rate up to 60 Mpixels/s**
- **Flexible and Easy to Operate via Serial Control Lines:**
  - **Exposure Time: 1 to 32 000 µs**
  - **Analog Gain: -2 dB to 28 dB by Steps of 0.035 dB**
  - **Digital Gain: 0 dB to 30 dB**
  - **Output Format: 8-, 10- or 12-bit Data on One or Two Outputs**
  - **Offset (for Contrast Expansion)**
  - **Trigger Mode: Free-run or External Trigger Modes**
- **Flat-field Correction (Lens and Light Non-uniformity and FPN and PRNU Correction)**
- **Multi-camera Synchronization**
- **Single Power Supply: DC 12 to 24V**
- **Very Compact Design: 56 x 60 x 39.4 mm (w, h, l)**
- **High Reliability – CE and FCC Compliant**
- **C or F (Nikon) T2 (M42 x 0.75) or M42 x 1 Mount Adapter (Lens not Supplied)**

Description

This smarter M2 offers the best in linescan cameras, with an increasingly improved accuracy, versatility and easy implementation. The AViiVA SM2 takes advantage of all the features that made the success of the AViiVA M2, with additional flat-field correction and contrast expansion functions. The same compact mechanical design incorporates all sensors, from 512 to 4096 pixels. Atmel manages the entire manufacturing process, from the sensor to the camera. The result is a camera able to operate in up to 12 bits, with dedicated electronics offering an excellent signal to noise ratio. The programmable settings let the user work at different integration times, gains and offsets. The external clock and trigger enable synchronization of several cameras.

Applications

The performance and reliability of this camera make it well-suited for the most demanding industrial applications, from web inspection to document scanning, from surface inspection to metrology.

CameraLink™ Linescan Camera

AViiVA™ SM2

Preliminary

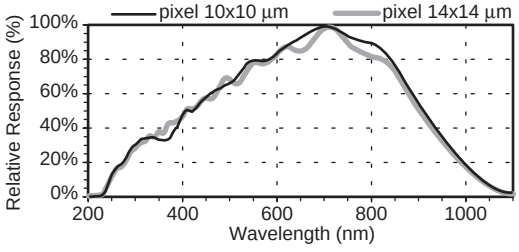
5372A–IMAGE–03/04

Typical Performances

Table 1. Typical Performances

Parameter	Value				Unit
Sensor Characteristics at Maximum Pixel Rate					
Resolution	512	1024	2048	4096	Pixels
Pixel size (square)	14 –	14 10	14 10	– 10	µm µm
Maximum line rate	98	53	28	14	kHz
Anti-blooming	x 150				–
Radiometric Performances (Maximum Pixel Rate, Tamb = 25°C)					
Output format	12 (also configurable in 8 or 10)				bit
Spectral range	250 - 1100				nm
Linearity (G = 0)	< 2				%
Gain range (step of 0.035 dB)	Gmin -2	Gnom 0	Gmax 28		dB
Peak response[1][2] with 14 µm pitch 10 µm pitch	100 50	130 65	3250 1625		LSB/(nJ/cm^2) LSB/(nJ/cm^2)
SNR	66	64	36		dB
Input RMS noise with 14 µm pitch 10 µm pitch	18 37				pJ/cm^2 pJ/cm^2
PRNU (Pixel Response Non-uniformity)	± 3% (± 10% max)				%
Mechanical and Electrical Interface					
Size (w x h x l)	56 x 60 x 39.4				mm
Lens mount	C, F, T2, M42 x 1				–
Sensor alignment (See “Sensor Alignment” on page 15)	Δx,y = ±50 – Δz = ±30 – Δtilt$_z$ = 0-35 Δθx,y = ±0.2				µm °
Power supply	DC, single 12 to 24V				V
Power dissipation	< 6.5				W
Operating temperature[3]	0 to 65 (non condensing)				°C
Storage temperature	-40 to 75 (non condensing)				°C

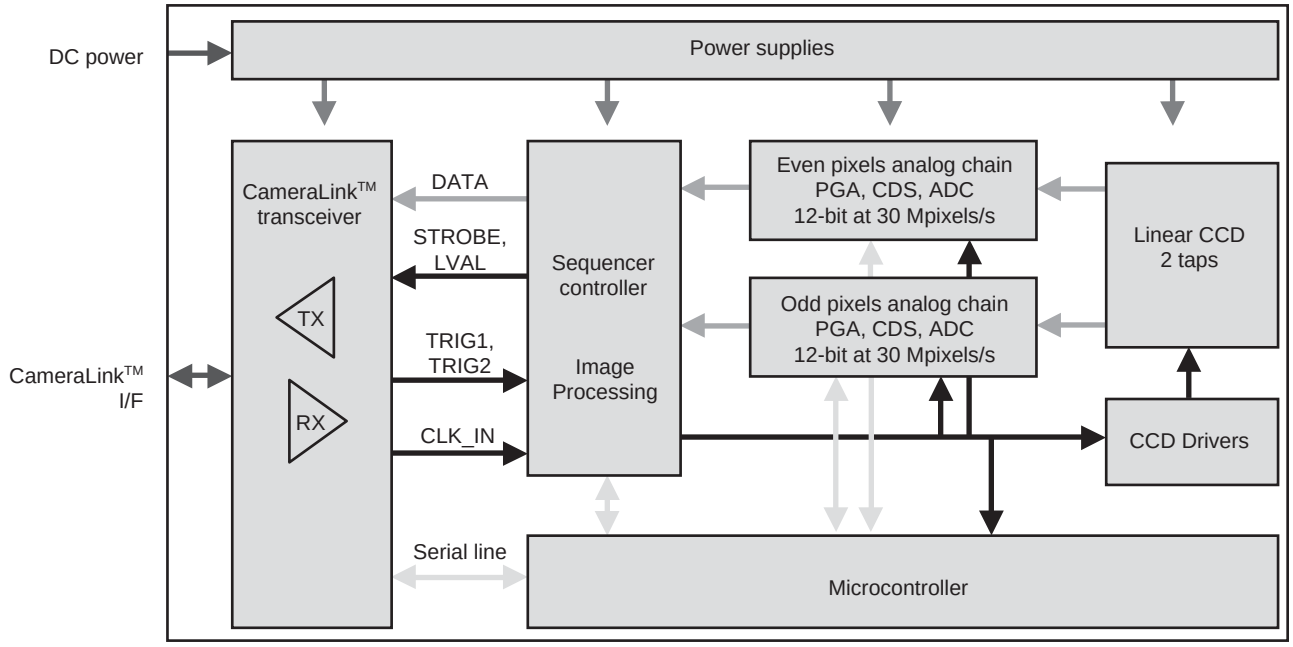
Spectral Response



Notes: 1. LSBs are given for a 12-bit configuration
2. nJ/cm^2 measured on the sensor
3. Camera’s front face temperature

Camera Description

Figure 1. Camera Synoptic



The camera is based on a two-tap linear CCD. Therefore, two analog chains process the odd and even pixel outputs of the linear sensor. The CCD signal processing encompasses the correlated double sampling (CDS), the dark level correction (dark pixel clamping), the gain (PGA) and offset correction, and finally the analog-to-digital conversion in 12 bits. An FPGA has been implemented for image processing (flat-field correction, dynamic selection and test pattern generation).

Note: PGA stands for Programmable Gain Array.

The camera is powered by a single DC power supply from 12 to 24V.

The functional interface (data and control) is provided with the CameraLink™ interface. The camera uses the base configuration of the Cameralink standard.

Note: DVAL = 1 and FVAL = 0

Data can be delivered on two channels or on a single multiplexed channel. The data format can be configured in 8, 10 or 12 bits.
The camera can be used with external triggers (TRIG1 and TRIG2 signals) in different trigger modes (see “Synchronization Mode” on page 7). The camera can also be clocked externally, allowing system synchronization and/or multi-camera synchronization.

The camera configuration and settings are done via a serial line, used for:

- Gain and offset settings
- Dynamic range data rate setting
- Trigger mode setting: free-run or external trigger modes
- Integration time setting: in free-run and external trigger mode

Standard Conformity

The AViiVA cameras have been tested using the following equipment:

- A shielded power supply cable
- A CameraLink™ data transfer cable ref. 14B26-SZLB-500-OLC (3M™)
- A linear AC-DC power supply

Atmel recommends using the same configuration to ensure compliance with the following standards.

CE Conformity

The AViiVA cameras comply with the requirements of the EMC (European) directive 89/336/CEE (EN 50081-2, EN 61000-6-2).

FCC Conformity

The AViiVA cameras further comply with Part 15 of the FCC rules, which states that:

Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Warning: Changes or modifications to this unit not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

Camera Command and Control

The camera’s configuration is set through the serial interface. Please refer to “Serial Communication” on page 11 for the serial line’s detailed protocol.

Table 2. Camera Command and Control

Setting	Command	Parameter	Description
Global gain[1]	G=	-65 to 811	Gain setting from -2 to 28 dB (~0.035 dB steps)
Even Gain[1]	A=	0 to 56	Even pixels gain adjustment (odd – even mismatch adjustment)
Odd Gain[1]	B=	0 to 56	Odd pixels gain adjustment (odd – even mismatch adjustment)
Number of outputs	D=	0 1	One tap (odd and even data multiplexed) Two taps
Data transfer[2]	H=	0 1 2 3 4 5 6	External clock (data rate = 2 x external clock)[6] External clock (data rate = external clock) External clock (data rate = external clock/2) 2 x 10 MHz data rate (20 MHz in one tap) 2 x 15 MHz data rate (30 MHz in one tap) 2 x 20 MHz data rate (40 MHz in one tap) 2 x 30 MHz data rate (60 MHz in one tap)
Output format[3]	S=	0 1 2	12-bit output data 10-bit output data 8-bit output data
Image source[4]	T=	0 1 2	Sensor row image Test pattern Sensor corrected image (flat-field correction enabled)
Configuration recall	+C=	0 1 to 4	Restore the default configuration Restore the user configuration 1 to 4
Configuration storage	-C=	1 to 4	Store the user configuration 1 to 4
FPN recall	+F=	1 to 4	Restore FPN factors from the FPN bank 1 to 4
FPN storage	-F=	1 to 4	Store the active FPN factors in the FPN bank 1 to 4
PRNU recall	+P=	1 to 4	Restore the PRNU factors from the PRNU bank 1 to 4
PRNU storage	-P=	1 to 4	Store the active PRNU factors in the PRNU bank 1 to 4
Integration time	I=	1 to 32768	Integration time (µs) in free-run or external triggered mode
Trigger mode	M=	1 2 3 4	Free-run with integration time setting (see Figure 2 on page 7) External trigger with integration time setting (see Figure 3 on page 7) Trigger and Integration time controlled (see Figure 4 on page 8) Trigger and integration time controlled by two inputs (see Figure 5 on page 8)
Even data offset[5]	O=	0 to 255	Even Offset setting from 0 to 255 LSB
Odd data offset[5]	P=	0 to 255	Odd Offset setting from 0 to 255 LSB
Contrast expansion	Q= R=	-4096 to 4095 0 to 255	Negative digital offset in LSB/12 bits Digital gain x1 to x33 (0.125 steps)
Write FPN[9]	WFP=		Send FPN values
Read FPN[10]	RFP=		Read FPN values
Write PRNU[9]	WPR=		Send PRNU values

Table 2. Camera Command and Control (Continued)

Setting	Command	Parameter	Description
Read PRNU[10]	RPR=		Read PRNU values
Special commands	!=	0	Camera identification readout
		1	User camera identification readout
		2	Software version readout
		3	Camera configuration readout
		4	Status readout
		5	Start FPN calibration[7]
		6	Start PRNU calibration[8]
		8	Software version readout
		9	Abort calibration
User camera ID	$=	String	Write user camera identification (50 characters maximum)

Notes:
1. Camera gain (dB) = G x 0.0353. A and B gain values are set during manufacturing but can be adjusted if necessary.
2. The CameraLink standard does not allow working below a 20 MHz clock frequency.
3. The pinout corresponding to this option is fully compatible with the CameraLink standard.
4. The test pattern is useful for checking if the device is correctly interfaced. The user should see a jagged image of 256 pixel steps.

5. The offset is set during manufacturing to balance both channels. The initial setting is about 130 LSB. In some cases, the user may have to change it (for example if the ambient temperature is very high).
6. To be used for multi-camera synchronisation. Refer to Figure 6 on page 9.
7. Switch off all lights before starting the FPN (dark) calibration. It must be done before the PRNU calibration.
8. Place a white reference in front of the camera before starting the PRNU (white light) calibration. The light level must be between half and full dynamic range.
9. Parameter format: <addr><size><value><value>...
   <addr> = pixel number
   <size> = amount of data sent
   <value> = parameter value (0 to 255 for FPN [0 to 255 LSB]; 0 to 16383 for PRNU [x1 to x2 gain])
   Parameters are sent from <addr> to <addr> + 5 pixels maximum
10. Parameter format: <addr><size>

Timing

Synchronization Mode

Four different modes may be defined by the user. The TRIG1 and TRIG2 signals may be used to trigger external events and control the integration time. The master clock is either an external or internal clock.

Free Run Mode with Integration Time Setting

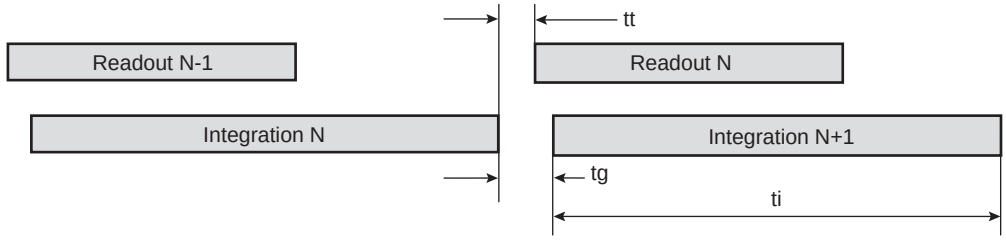
The integration and readout periods start automatically and immediately after the previous period. The readout time depends on the number of pixels and the pixel rate.

Table 3. Free Run Mode with Integration Time Setting

Label	Description	Min	Typ	Max
ti	Integration time duration	(1)	–	32 ms
tg	Consecutive integration period gap (at maximum frequency)	–	6 µs	–
tt	Integration period stop to readout start delay	–	1 µs	–

Note: 1. The integration time is set by the serial line and should be higher than the readout time (otherwise it is adjusted to the readout time).

Figure 2. Timing Diagram



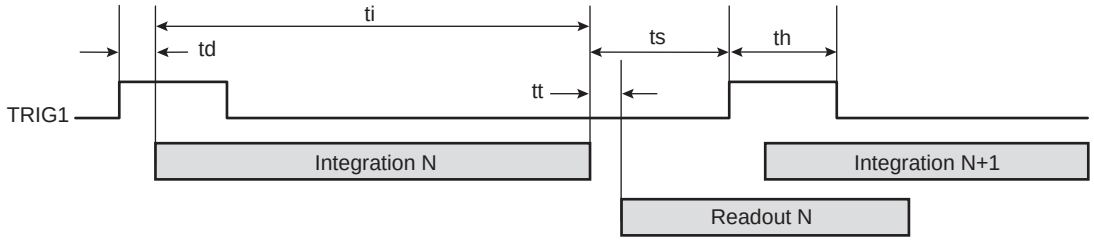
Triggered Mode with Integration Time Setting

The integration period starts immediately after the rising edge of the TRIG1 input signal and is set by the serial line. This period is immediately followed by a readout period. The readout time depends on the number of pixels and the pixel rate.

Table 4. Triggered Mode with Integration Time Setting

Label	Description	Min	Typ	Max
ti	Integration time duration	1 µs	–	32 ms
td	TRIG1 rising to integration period start delay	–	<1 µs	–
tt	Integration period stop to readout start delay	–	1 µs	–
ts	Integration period stop to TRIG1 rising set-up time	4 µs	–	–
th	TRIG1 hold time (high pulse duration)	0.1 µs	–	–

Figure 3. Timing Diagram



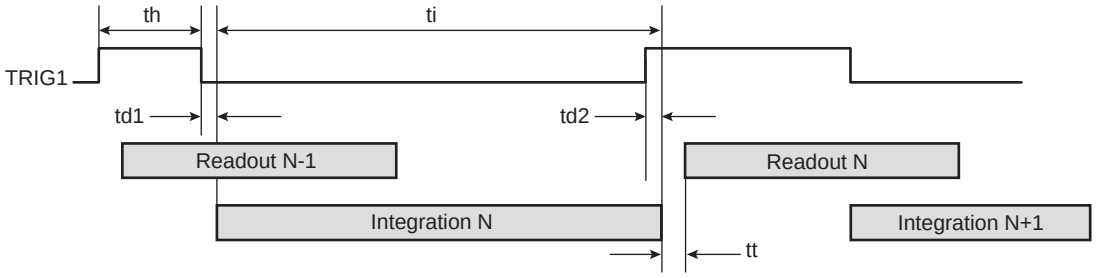
Trigger and Integration Time Controlled by One Input

The integration period starts immediately after the falling edge of the TRIG1 input signal, stops immediately after the rising edge of TRIG1 input signal, and is immediately followed by a read-out period. The readout time depends on the number of pixels and the pixel rate.

Table 5. Trigger and Integration Time Controlled by One Input

Label	Description	Min	Typ	Max
ti	Integration time duration	1 µs	–	–
td1	TRIG1 falling to integration period start delay	–	100 ns	–
td2	TRIG1 rising to integration period stop delay	–	1.3 µs	–
tt	Integration period stop to readout start delay	–	1 µs	–
th	TRIG1 hold time (high pulse duration)	0.1 µs	–	–

Figure 4. Timing Diagram



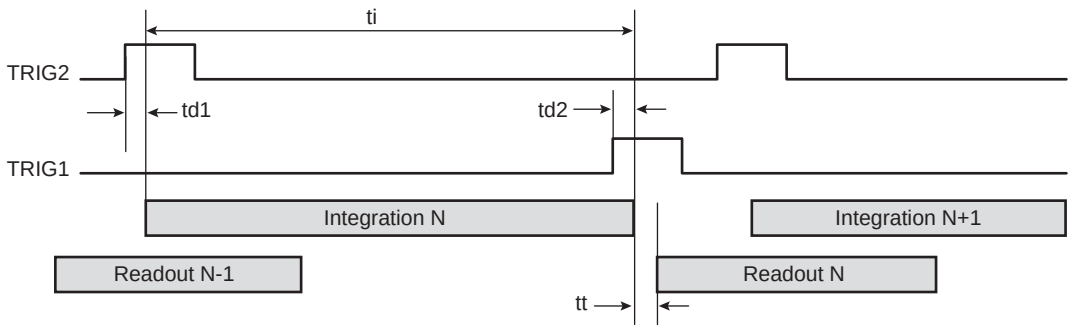
Trigger and Integration Time Controlled by Two Inputs

The TRIG2 signal's rising edge starts the integration period and the TRIG1 signal's rising edge stops the integration period. This period is immediately followed by a readout period.

Table 6. Trigger and Integration Time Controlled by Two Inputs

Label	Description	Min	Typ	Max
ti	Integration time duration	1 µs	–	–
td1	TRIG2 rising to integration period start delay	–	100 ns	–
td2	TRIG1 rising to integration period stop delay	–	1.3 µs	–
tt	Integration period stop to read-out start delay	–	1 µs	–
th	TRIG1 and TRG2 hold time (high pulse duration)	0.1 µs	–	–

Figure 5. Timing Diagram



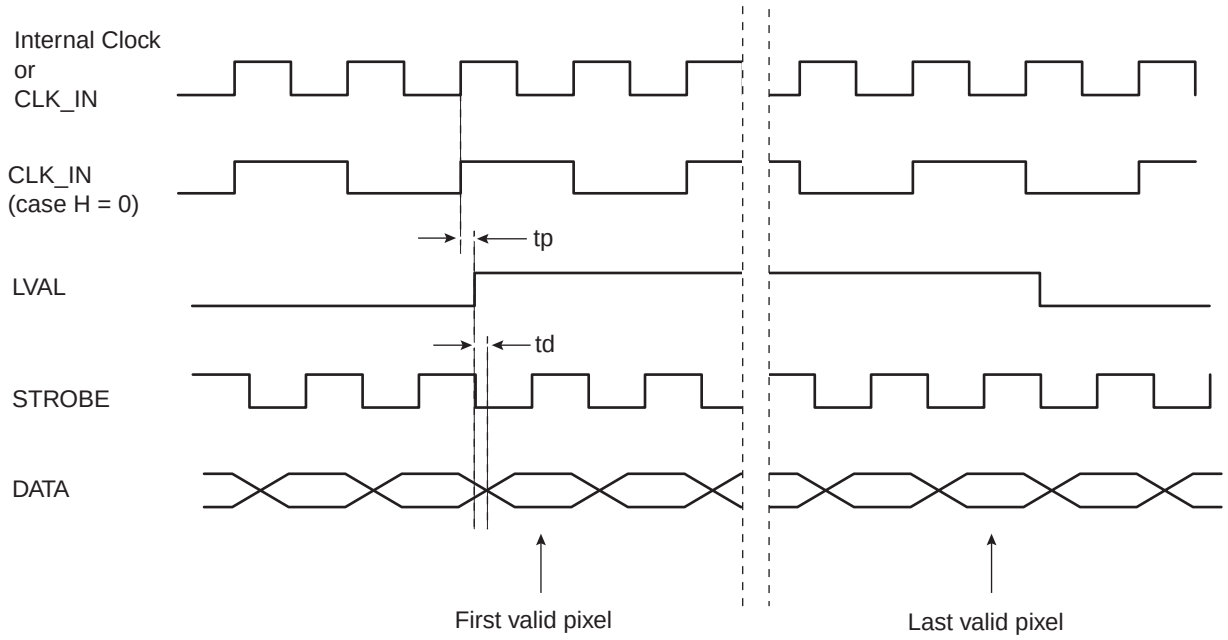
Output Data Timing

This timing corresponds to the input data of the “Chanel Link” interface. The camera’s output data is not detailed here as it is fully compliant with the CameraLink™ standard (serial high-speed interface).

Table 7. Output Data Timing

Label	Description	Min	Typ	Max
tp	Input falling edge to output clock propagation delay	–	7 ns	–
td	STROBE to synchronized signals delay	-5 ns	–	+5 ns

Figure 6. Timing Diagram



Note: The CLK_IN input frequency must be in the range of 5 to 60 MHz. Outside this range, the performances may be degraded.

If multiple cameras are synchronized (more than one camera on one acquisition board):

- The “master” camera provides DATA, STROBE and LVAL signals to the acquisition board. The others only provide DATA.
- The external clock CLK_IN must be input on each camera to guarantee perfect data synchronisation.
- The trigger input(s) (TRIG1 and/or TRIG2) must be input on each camera. We recommend synchronization of the rising edge of these signals on the CLK_IN falling edge.
- Cables must be balanced between each camera (same quality and same length) to ensure perfect camera synchronisation.
- The CLK_IN frequency must be equal to the two CCD register frequencies. This means that the user should use H = 0. Using H =1 or H = 2 clock modes provides LVAL jitters on the “slave” camera.
- Only “trigged and integration time controlled” (M = 3 or M = 4) can be used. These modes ensure perfect initiation of each camera’s readout phase.

Electrical Interface

Power Supply

It is recommended to insert a 1-amp fuse between the power supply and the camera.

Table 8. Power Supply

Signal Name	I/O	Type	Description
PWR	P	–	DC power input: +12V to +24V (±0.5V)
GND	P	–	Electrical and Mechanical ground

I = Input, O = Output, IO = Bi-directional signal, P = Power/ground, NC = Not connected

Camera Control

The CameraLink interface provides four LVDS signals dedicated to camera control (CC1 to CC4). On the AViiVA, three of them are used to synchronize the camera on external events.

Table 9. Camera Control

Signal Name	I/O	Type	Description
TRIG1	I	RS644	CC1 – Synchronization input (refer to “Synchronization Mode” on page 7)
TRIG2	I	RS644	CC2 – Start Integration period in dual synchro mode (refer to “Synchronization Mode” on page 7)
CLK_IN	I	RS644	CC4 – External clock for (multi-) camera synchronization (refer to “Synchronization Mode” on page 7)

I = Input, O = Output, IO = Bi-directional signal, P = Power/ground, NC = Not connected

Note: CC3 is not used.

Video Data

Data and enable signals are provided on the CameraLink interface.

Table 10. Video Data

Signal Name	I/O	Type	Description
ODD[11-0]	O	RS644	Odd pixel data (refer to “Output Data Timing” on page 9), ODD-00 = LSB, ODD-11 = MSB
EVEN[11-0]	O	RS644	Even pixel data (refer to “Output Data Timing” on page 9), EVEN-00 = LSB, EVEN-11 = MSB
STROBE	O	RS644	Output data clock (refer to “Output Data Timing” on page 9), data valid on the rising edge
LVAL	O	RS644	Line valid (refer to “Output Data Timing” on page 9), active high signal

I = Input, O = Output, IO = Bi-directional signal, P = Power/ground, NC = Not connected

Notes: FVAL, as defined in the CameraLink standard, is not used. FVAL is permanently tied to 0 (low) level.
DVAL is not used. DVAL is permanently tied to 1 (high) level.
In case of single output, the multiplexed data is output in place of the odd data.

Serial Communication

The CameraLink interface provides two LVDS signal pairs for communication between the camera and the frame grabber. This is an asynchronous serial communication based on the RS-232 protocol.

The serial line's configuration is:

- Full duplex/without handshaking
- 9600 bauds, 8-bit data, no parity bit, 1 stop bit

Table 11. Serial Communication

Signal Name	I/O	Type	Description
SerTFG	O	RS644	Differential pair for serial communication to the frame grabber
SerTC	I	RS644	Differential pair for serial communication from the frame grabber

Command Syntax

The valid syntax is "S=n(CR)" with:

- S: command identification as per "Camera Command and Control" on page 4.
- n: setting value
- (CR): stands for "carriage return"

No space, nor tab may be inserted between S, =, n and (CR).

Example of a valid command:

- G = 3(CR): sets the camera to gain 3 (refer to "Camera Command and Control" on page 4 for exact value calculation)

Example of non valid commands:

- G = 3(CR): spaces
- g = 3(CR): g instead of G
- G = 1040(CR): 1040 is outside of range

Command Processing

All commands received by the camera are processed:

- If the command is valid:
  - and if it is a write command, the setting is done
  - and if it is a read command, the camera returns the data separated by (CR)
  - the camera returns: >OK(CR)
- If the command is not valid:
  - nothing happens
  - the camera returns: >1 = out of range; >2 = syntax error; >4 = invalide command; others = internal error

Example: when receiving "! = 3(CR)'' the camera returns its current settings:

- A = 0(CR); B = 0(CR); ....; >OK(CR)

Storage of the Settings in EEPROM

The current settings must be saved in EEPROM before the camera is switched off. The maximum number of write cycles allowed for EEPROM is 100 000.

Connector Description

All connectors are on the rear panel.

Note: cables for digital signals must be shielded twisted pairs.

Power Supply

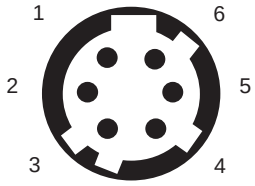
Camera connector type: Hirose HR10A-7R-6PB (male).

Cable connector type: Hirose HR10A-7P-6S (female).

Table 12. Power Supply Connector Pinout

Signal	Pin	Signal	Pin
PWR	1	GND	4
PWR	2	GND	5
PWR	3	GND	6

Figure 7. Receptacle Viewed from Rear Face of Camera



CameraLink Connector

A standard CameraLink cable must be used to ensure full electrical compatibility.

The camera connector type is MDR-26 (female) ref. 10226-2210VE.

The cable connector type is a standard CameraLink cable (3M - 14B26-SZLB-x00-OLC).

Table 13. CameraLink Connector Pinout

Signal	Pin	Signal	Pin	Signal	Pin
GND	1	CC2+	10	X3+	19
X0-	2	CC3-	11	SerTC-	20
X1-	3	CC4+	12	SerTFG+	21
X2-	4	GND	13	CC1+	22
Xclk-	5	GND	14	CC2-	23
X3-	6	X0+	15	CC3+	24
SerTC+	7	X1+	16	CC4-	25
SerTFG-	8	X2+	17	GND	26
CC1-	9	Xclk+	18		

Bit Assignments

The following bit assignments are compliant with the CameraLink Specification in the base configuration.

In “single-output” mode (multiplexed), data is output on the ODD-xx bit.

Table 14. Bit Assignments When Used With12-bit Data (S = 0)

Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name
ODD-00	Tx0	ODD-07	Tx5	EVEN-02	Tx19	EVEN-09	Tx14
ODD-01	Tx1	ODD-08	Tx7	EVEN-03	Tx20	EVEN-10	Tx10
ODD-02	Tx2	ODD-09	Tx8	EVEN-04	Tx21	EVEN-11	Tx11
ODD-03	Tx3	ODD-10	Tx9	EVEN-05	Tx22	STROBE	TxCLK
ODD-04	Tx4	ODD-11	Tx12	EVEN-06	Tx16	LVAL	Tx24
ODD-05	Tx6	EVEN-00	Tx15	EVEN-07	Tx17		
ODD-06	Tx27	EVEN-01	Tx18	EVEN-08	Tx13		

Table 15. Bit Assignments When Used With 10-bit Data (S = 1)

Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name
ODD-00	Tx0	ODD-07	Tx5	EVEN-02	Tx19	EVEN-09	Tx14
ODD-01	Tx1	ODD-08	Tx7	EVEN-03	Tx20	NC	Tx10
ODD-02	Tx2	ODD-09	Tx8	EVEN-04	Tx21	NC	Tx11
ODD-03	Tx3	NC	Tx9	EVEN-05	Tx22	STROBE	TxCLK
ODD-04	Tx4	NC	Tx12	EVEN-06	Tx16	LVAL	Tx24
ODD-05	Tx6	EVEN-00	Tx15	EVEN-07	Tx17		
ODD-06	Tx27	EVEN-01	Tx18	EVEN-08	Tx13		

Table 16. Bit Assignments When Used With 8-bit Data (S = 2)

Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name	Bit	DS90CR285 Pin Name
ODD-00	Tx0	ODD-07	Tx5	NC	Tx19	EVEN-05	Tx14
ODD-01	Tx1	EVEN-00	Tx7	NC	Tx20	EVEN-06	Tx10
ODD-02	Tx2	EVEN-01	Tx8	NC	Tx21	EVEN-07	Tx11
ODD-03	Tx3	EVEN-02	Tx9	NC	Tx22	STROBE	TxCLK
ODD-04	Tx4	EVEN-03	Tx12	NC	Tx16	LVAL	Tx24
ODD-05	Tx6	NC	Tx15	NC	Tx17		
ODD-06	Tx27	NC	Tx18	EVEN-04	Tx13		

Mechanical Characteristics

Weight

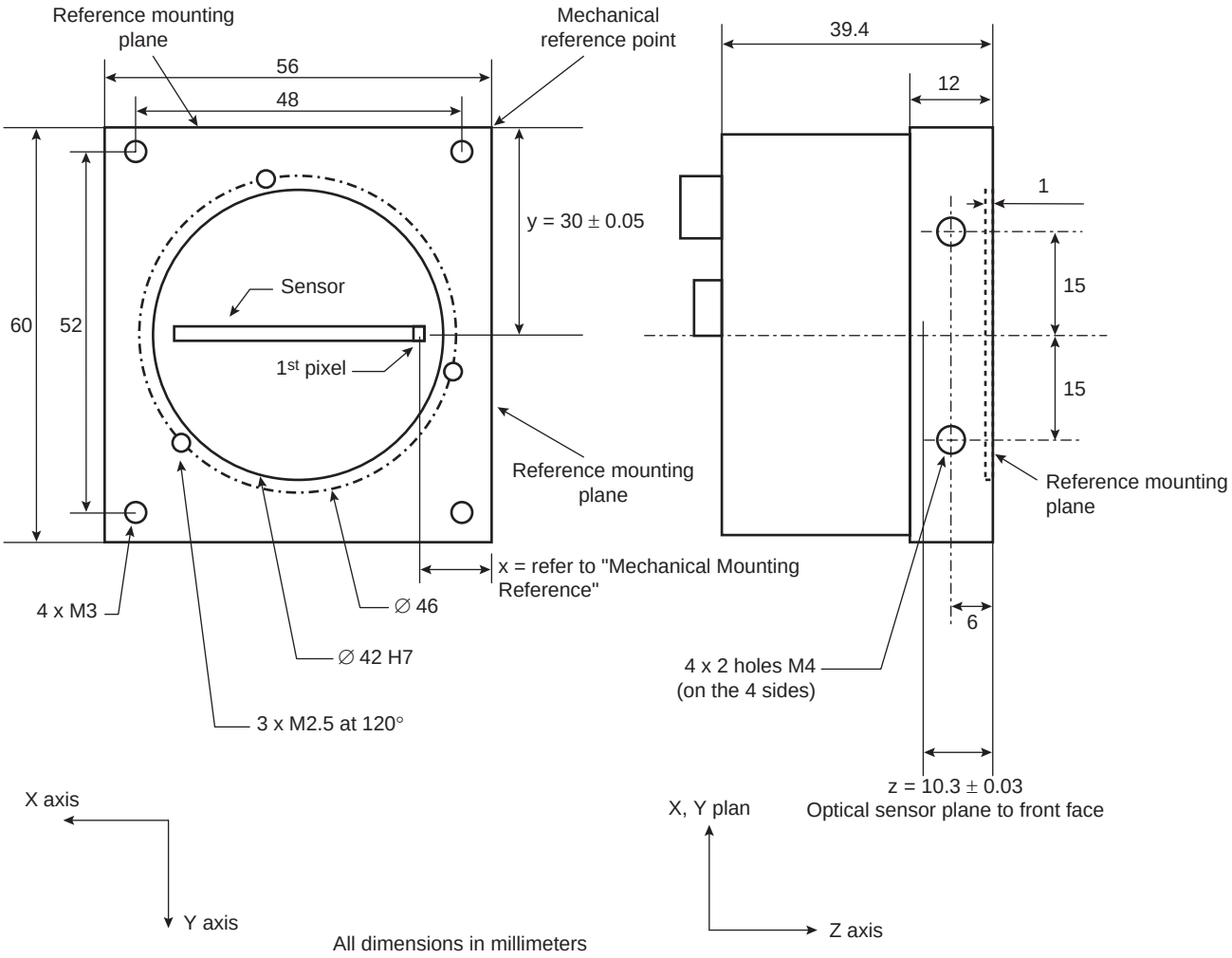
The camera's typical weight (without lens nor lens adapter) is 220g or 7.7 ounces.

Dimensions

The camera's dimensions (without lens) are:

- 56 mm width
- 60 mm height
- 39.4 mm length

Figure 8. Mechanical Box Drawing and Dimensions



Mechanical Mounting Reference

The front panel's mechanical part is designed to support mounting of the camera. Three surfaces on this mechanical area are considered as mounting reference surfaces. This implies

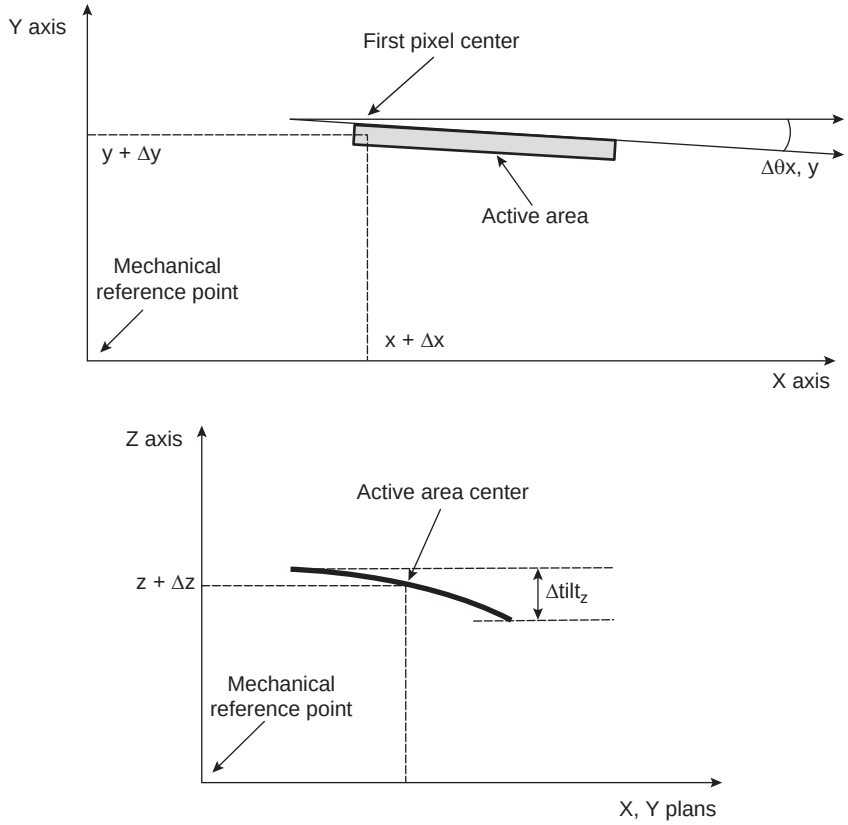
that the distance between these surfaces and the first active pixel are very precise (better than ±50 µm).

Table 17. Mechanical Mounting Reference

Number of Pixels	512	1024	2048	4096
x with 14 µm sensor (nm)	24.416	20.832	13.664	–
x with 10 µm sensor (nm)	–	22.880	17.760	7.520

Sensor Alignment

Figure 9. Sensor Alignment Diagram



Mounting of Lens (Lens Not Supplied)

The camera can be provided with three different lens adapters, corresponding to three different options. The user must select the appropriate adapter. The following table gives recommendations according to the sensor size.

Table 18. Lens Mounting

Number of Pixels	512/14 µm	1024/10 µm	1024/14 µm	2048/10 µm	2048/14 µm	4096/10 µm
C mount	OK	OK	~OK(1)	~OK(1)	not usable	not usable
F mount	OK	OK	OK	OK	OK	OK
T2 (M42 x 0.75) mount	OK	OK	OK	OK	OK	OK
M42 x 1 mount	OK	OK	OK	OK	OK	OK

Note: 1. Depends on lens quality.

Heat Sink Mounting

In order to improve power dissipation, the camera can be delivered with a heat sink to be mounted by the user on the side faces of the camera. Delivery of the heat sink is an option.

Ordering Code

Table 19. Ordering Code

Part Number	Resolution	Pixels Size	Description
AT71SM2CL1010-BA0	1K	10 µm	AViiVA M2 CL 1010
AT71SM2CL2010-BA0	2K	10 µm	AViiVA M2 CL 2010
AT71SM2CL4010-BA0	4K	10 µm	AViiVA M2 CL 4010
AT71SM2CL0514-BA0	512	14 µm	AViiVA M2 CL 0514
AT71SM2CL1014-BA0	1K	14 µm	AViiVA M2 CL 1014
AT71SM2CL2014-BA0	2K	14 µm	AViiVA M2 CL 2014
AT71KFPAVIVA-ABA	–	–	F mount (NIKON)
AT71KFPAVIVA-AKA	–	–	T2 mount (M42 x 0.75)
AT71KFPAVIVA-ADA	–	–	M42 x 1 mount
AT71KFPAVIVA-ACA	–	–	C mount
AT71KAVIVAP2C0D3A0	–	–	Cable kit: 10-meter power supply and 5-meter CameraLink cables

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44306 Nantes Cedex 3, France
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Fax: (33) 2-40-18-19-60

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