MN74HC166/MN74HC166S

8-Bit Parallel-Input/Serial-Output Shift Register

■ Outline

The MN74HC166/MN74HC166S is a high speed 8-bit parallel-input/serial-output shift register.

Each data is transmitted at the rise of CLK. When the level of CLR was set to "L", all the outputs become the low level irrespectively of the CLK and the data.

Owing to the silicon gate CMOS process, this shift register has realized low power consumption and high noise immunity equivalent to those of a standard CMOS and the operation speed as high as of an LS TTL, and can directly drive ten LS TTL inputs.

To protect the input and output against electrostatic breakdown, a reistor and a diode are used for the V_{CC} and the GND. The pin configuration and the function are the same as those of the standard 54LS/74LS logic family.
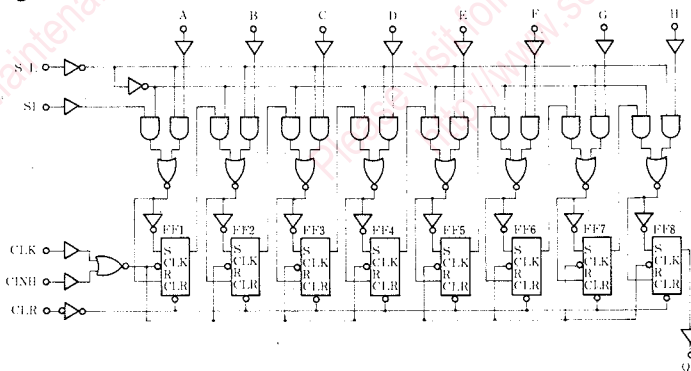
P-3

16-pin plastic DIL package

P-4

16-pin PANAFLAT package (SO-16D)

■ Truth Table

Input						Internal Stages		Output
CLR	S/L	CINH	CLK	SI	Parallel A···H	QA	QB	QH
L	×	×	×	×	×	L	L	L
H	×	L	L	×	×	QA0	QB0	QH0
H	L	L	⌐⌐	×	a···h	a	b	h
H	H	L	⌐⌐	H	×	H	QAn	QGn
H	H	L	⌐⌐	L	×	L	QAn	QGn
H	×	H	⌐⌐	×	×	QA0	QB0	QH0

Note) 1. × : "H" or "L"
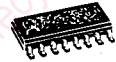2. ⌐⌐ : Leading from "L" to "H"

Pin Configuration

SI	1		16	Vcc
A	2		15	S/L
B	3		14	H
C	4		13	QH
D	5		12	G
CINH	6		11	F
CLK	7		10	E
GND	8		9	CLR

8-Bit Parallel-Input Serial-Output Shift Register

■ Logic Diagram
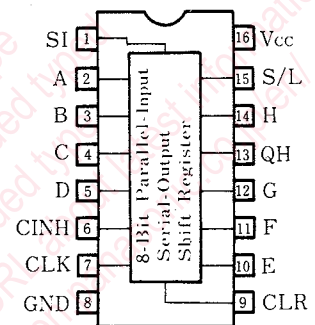
■ Absolute Maximum Ratings

Item			Symbol	Rating	Unit
Supply voltage			V_{CC}	$-0.5 \sim +7.0$	V
Input voltage			V_I	$-0.5 \sim V_{CC}+5$	V
Output voltage			V_O	$-0.5 \sim V_{CC}+5$	V
Input protective diode current			I_{IK}	± 20	mA
Output parasitic diode current			I_{OK}	± 20	mA
Output current			I_O	± 25	mA
Supply current			I_{CC}, I_{GND}	± 50	mA
Storage temperature			T_{stg}	$-65 \sim +150$	°C
Power dissipation	MN74HC166	Ta=$-40 \sim +60$°C	P_D	400	mW
		Ta=$+60 \sim +85$°C		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC166S	Ta=$-40 \sim +60$°C	P_D	275	mW
		Ta=$+60 \sim +85$°C		Decrease to 200mW at the rate of 3.8mW/°C	

■ Recommended Operating Conditions

Item	Symbol	V_{CC}(V)	Rating	Unit
Operating power supply voltage	V_{CC}		$1.4 \sim 6.0$	V
Input voltage	V_I		$0 \sim V_{CC}$	V
Output voltage	V_O		$0 \sim V_{CC}$	V
Operating temperature	T_A		$-40 \sim +85$	°C
Input rise, fall time	t_r, t_f	2.0	$0 \sim 1000$	ns
		4.5	$0 \sim 500$	ns
		6.0	$0 \sim 400$	ns

■ DC Characteristics (GND=0V)

Item	Symbol	V_{CC} (V)	Test Condition V_I	Test Condition V_O	Unit	Temperature Ta=25°C min.	Temperature Ta=25°C typ.	Temperature Ta=25°C max.	Temperature Ta=$-40 \sim +85$°C min.	Temperature Ta=$-40 \sim +85$°C max.	Unit
Input voltage high level	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input voltage low level	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output voltage high level	V_{OH}	2.0	V_{IH} or V_{IL}	-20.0 μA	μA	1.9	2.0		1.9		V
		4.5		-20.0 μA	μA	4.4	4.5		4.4		
		6.0		-20.0 μA	μA	5.9	6.0		5.9		
		4.5		-4.0 mA	mA	3.98			3.84		
		6.0		-5.2 mA	mA	5.48			5.34		
Output voltage low level	V_{OL}	2.0	V_{IH} or V_{IL}	20.0 μA	μA	0.0	0.1			0.1	V
		4.5		20.0 μA	μA	0.0	0.1			0.1	
		6.0		20.0 μA	μA	0.0	0.1			0.1	
		4.5		4.0 mA	mA		0.26			0.33	
		6.0		5.2 mA	mA		0.26			0.33	
Input leakage current	I_I	6.0	$V_I = V_{CC}$ or GND				± 0.1			± 1.0	μA
Static supply current	I_{CC}	6.0	$V_I = V_{CC}$ or GND, $I_O = 0$				8.0			80.0	μA

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## ■ AC Characteristics (GND=0V, Input transition time≦6ns, C_L=50pF)

Item	Symbol	V_{CC} (V)	Test Condition	Temperature					Unit
				Ta=25°C			Ta=−40~+85°C		
				min.	typ.	max.	min.	max.	
Output rise time	t_{TLH}	2.0			21	75		95	ns
		4.5			8	15		19	
		6.0			7	13		16	
Output fall time	t_{THL}	2.0			18	65		80	ns
		4.5			7	13		16	
		6.0			6	11		14	
Propagation time CLK→QH (L→H)	t_{PLH}	2.0			53	180		225	ns
		4.5			20	36		45	
		6.0			17	31		38	
Propagation time CLK→QH (H→L)	t_{PHL}	2.0			49	175		220	ns
		4.5			19	35		44	
		6.0			16	30		37	
Propagation time CLR→QH (H→L)	t_{PHL}	2.0			49	190		240	ns
		4.5			21	38		48	
		6.0			18	32		41	
Minimum pulse width CLR	t_w	2.0			16	70		90	ns
		4.5			8	14		18	
		6.0			7	12		15	
Minimum set-up time	t_{su}	2.0			13	100		125	ns
		4.5			3	20		25	
		6.0			2	17		21	
Minimum hold time	t_h	2.0			—	0		0	ns
		4.5			—	0		0	
		6.0			—	0		0	
Minimum recovery time	t_{rem}	2.0			5	75		95	ns
		4.5			3	15		19	
		6.0			1	13		16	
Maximum clock frequency	f_{max}	2.0		6	30		4		MHz
		4.5		30	70		24		
		6.0		35	80		28		

● Switching time measuring circuit and waveforms

1. Measuring circuit
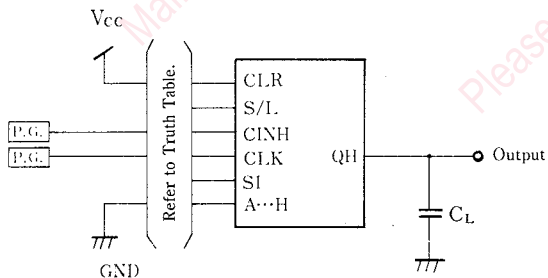
2. Switching waveforms
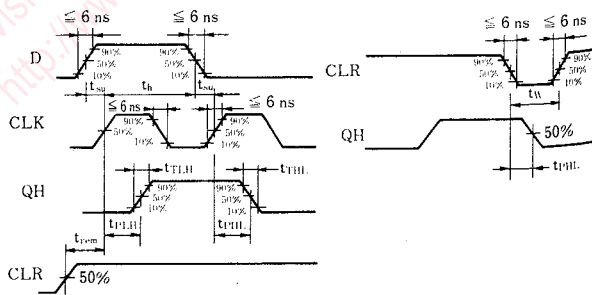
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