AT&T

Advance

DATA SHEET

LC1092AP/BP AC PLASMA DISPLAY COLUMN DRIVERS

DESCRIPTION

The LC1092AP and LC1092BP are high-voltage CMOS (HV-CMOS) integrated circuits that are assembled in 44-pin plastic J-leaded chip carriers. The LC1092BP pinout alignment is the mirror image of the LC1092AP pinout alignment (see Figures 2 and 3 for details).

The devices contain a 32-bit shift register which can accept serial data at clock rates up to 10 MHz. A LOAD feature is supplied to allow parallel transfer of the shift register data to a 32-bit latch. Data is transferred on a high-to-low transition of the LOAD signal. The contents of the latch are transferred in parallel to the high-voltage output buffers by means of the STROBE input. These high-voltage buffers will deliver voltage swings of ⩽100 volts. Serial data output from the shift register may be used to cascade shift registers. This output is not affected by either the LOAD or STROBE inputs. The LB1092AP/BP can also be operated in a pulsed HV_{POS} mode (100-volt swing) with a minimum rise time (10 to 90%) of 0.3 μsec and a minimum fall time (10 to 90%) of 0.5 μsec.

FEATURES

- **32-BIT SHIFT REGISTER**
- **32-BIT LATCH**
- **100-VOLT PUSH-PULL CMOS OUTPUTS**
- **10 MHz DATA CLOCK RATE**
- **EACH DEVICE DRIVES 32 LINES**

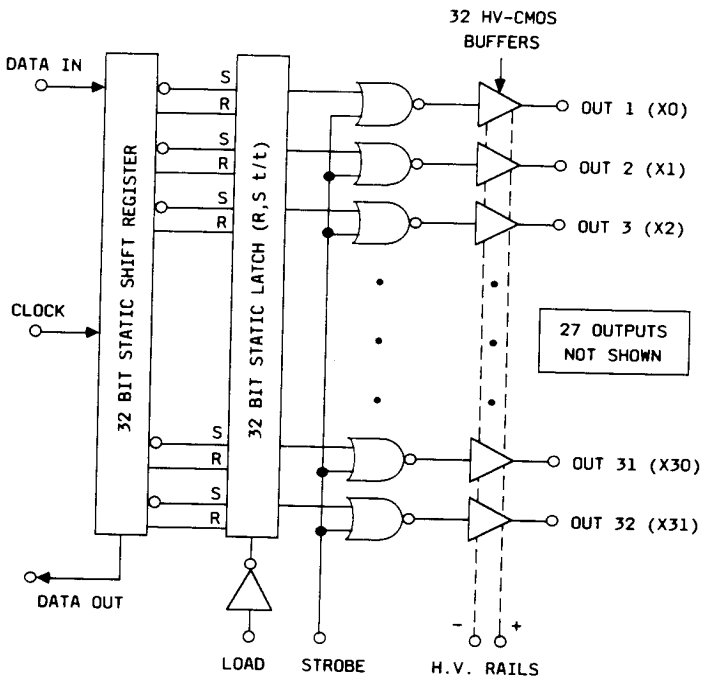


Fig. 1—Functional Diagram

NOVEMBER 1986

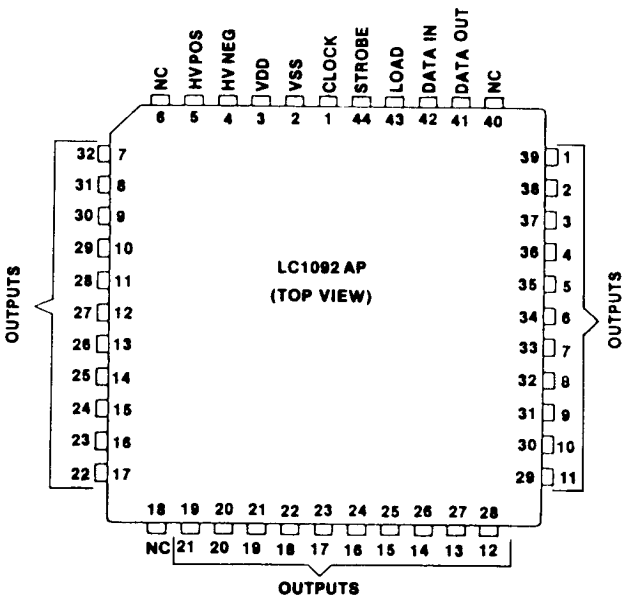


Fig. 2—LC1092AP Package Pinout

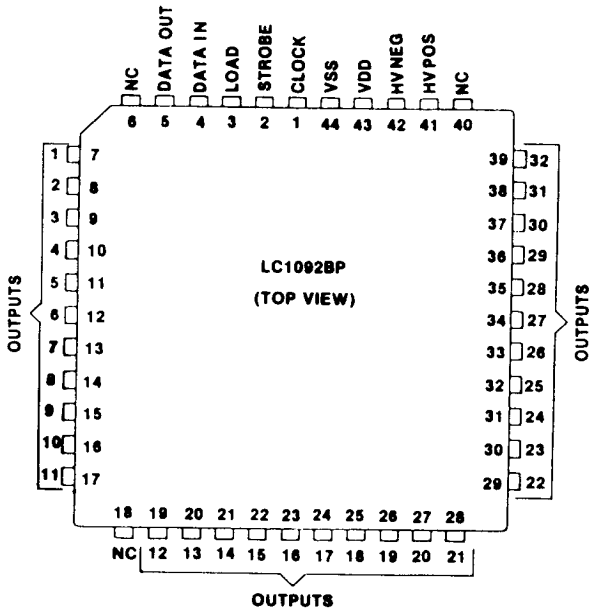


Fig. 3—LC1092BP Package Pinout

MAXIMUM RATINGS (At 25°C unless otherwise specified)	
Ambient Operating Temperature Range	0 to +60°C
Storage Temperature Range	−65 to +150°C
Lead Soldering Temperature (t = 10 sec. max.)	260°C
Supply Voltage (HV_{POS})①	+100 V
Supply Voltage (HV_{NEG})①	−95 V
Logic Supply Voltage (VDD)	+5.5 V
INPUT Voltage	VDD plus 0.5 V
Current (Each Driver Output)	4.0 mA
Power Dissipation	200 mW

Stresses in excess of those listed under "Maximum Ratings" may cause permanent damage to the device. This is an absolute stress rating only. Functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this Data Sheet is not implied. Exposure to maximum rating conditions for extended periods of time may affect device reliability.

①The difference between HV_{POS} and HV_{NEG} must never exceed 100 volts. HV_{POS} must always be positive with respect to HV_{NEG}.

PIN DESCRIPTION AND TIMING REQUIREMENTS

SYMBOL	NAME/FUNCTION
CLOCK	Input for clocking functions. The leading edge of CLOCK must come ≥20 nsec after valid DATA. Clock must remain high for ≥30 nsec.
DATA IN	Input for data stream. DATA must be valid for 12 nsec after CLOCK goes high.
DATA OUT	Serial data output from the Shift Register may be used to cascade shift registers.
STROBE	STROBE can go low ≥20 nsec after LOAD goes low.
LOAD	LOAD can go low ≥30 nsec after CLOCK goes high.
NC	No connection. This terminal should not be used as a tie point for external circuitry.
VDD	Logic supply voltage. Normal operating voltage is +5.0 V (±0.25 V).
VSS	Logic common (not necessarily system or physical ground).
HV_{POS}	External power supply. HV_{POS} must always be positive with respect to HV_{NEG}. The difference between HV_{POS} and HV_{NEG} must never exceed 100 volts.
HV_{NEG}	External power supply. HV_{NEG} must always be negative with respect to HV_{POS}. The difference between HV_{POS} and HV_{NEG} must never exceed 100 volts.
OUT *XX*	High-voltage CMOS outputs numbered 1 through 32.

SIMPLIFIED INPUT AND OUTPUT DIAGRAMS

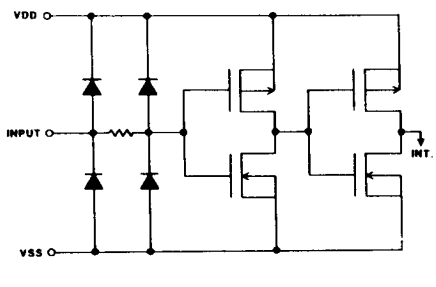


Fig. 4—Typical Input

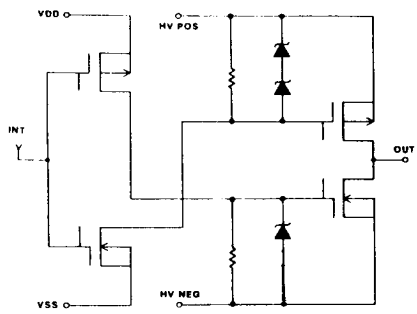


Fig. 5—Typical of All Outputs

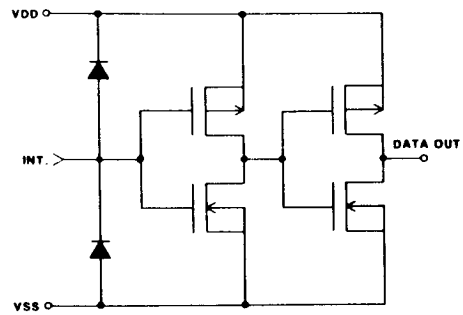
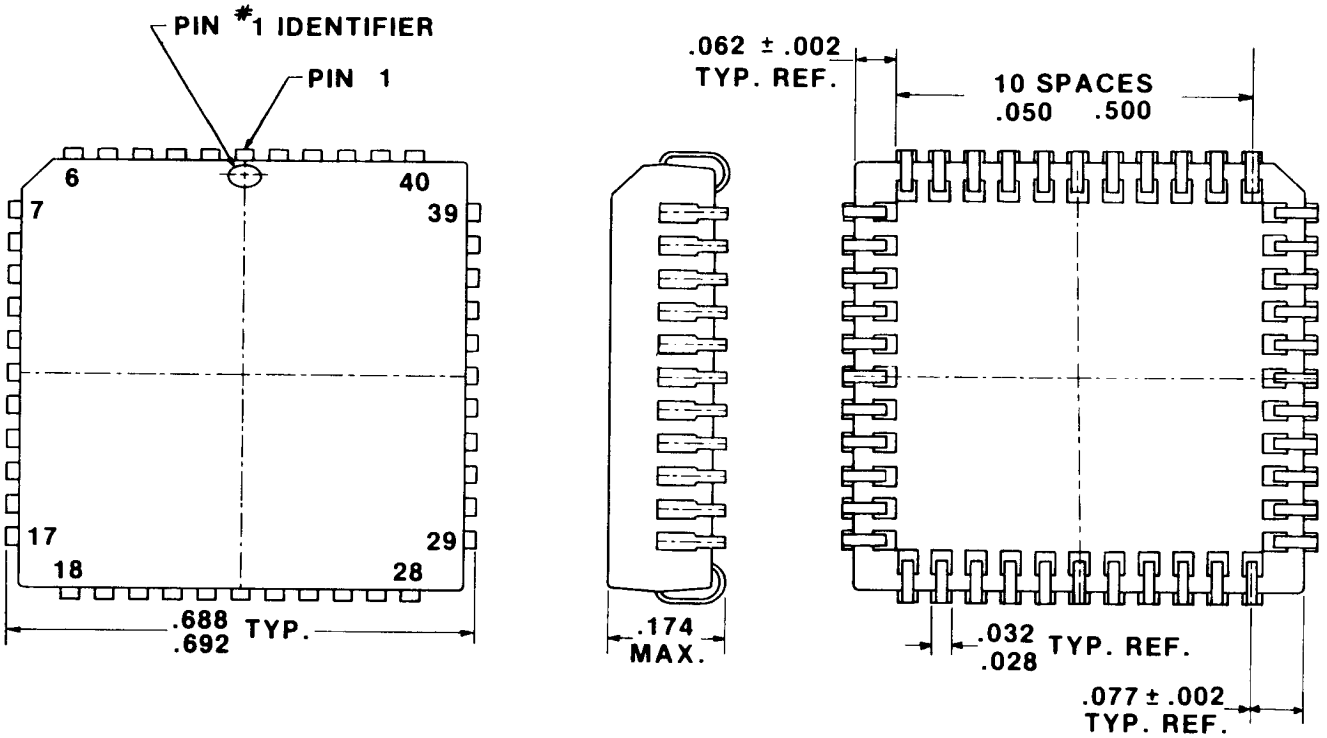


Fig. 6—Typical Data Output

OUTLINE DRAWINGS (Dimensions in Inches)



NOTE: The recommended chip carrier socket is Yamaichi #IC 51-0444-400 or equivalent.

ORDERING INFORMATION:

DEVICE	COMCODE
LC1092AP	104401492
LC1092BP	104401518

For additional information contact your AT&T Account Manager, or call:

☐ AT&T Technologies, 555 Union Boulevard, Dept. 50AL203140, Allentown, PA 18103
1-800-372-2447

TYPICAL OPERATING SEQUENCE

A typical operation sequence (Figure 7) is to clock data into the serial shift register at a clock rate of ≤10 mHz. This data is then transferred in parallel to the 32-bit latch. The information in the latch is transferred to the high-voltage output buffers by means of the STROBE which operates at a rate of ≤16 kHz. A data high input will yield a high-voltage high on the corresponding output, during the time that STROBE is low.

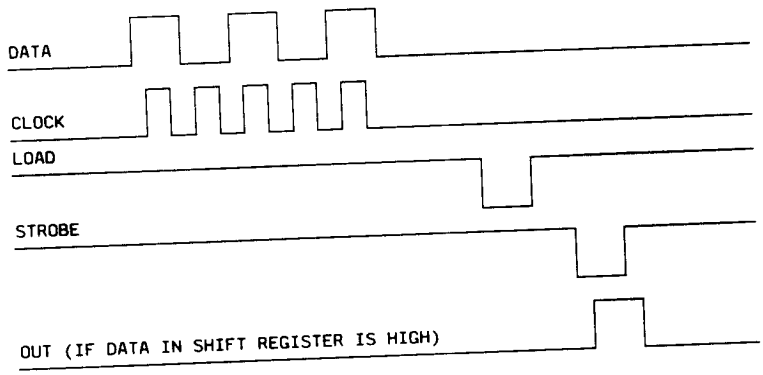
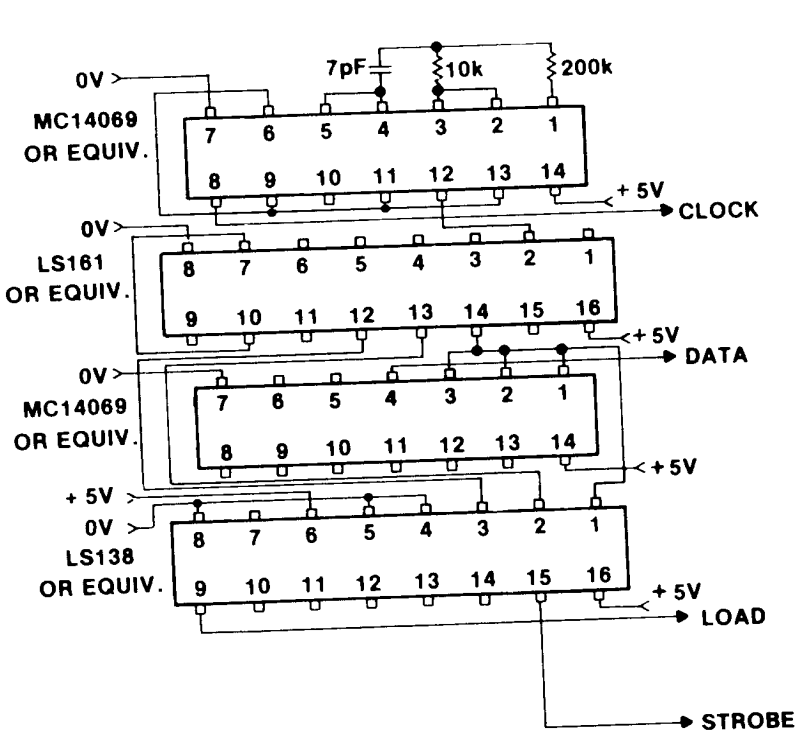


Fig. 7—Typical Operating Sequence Diagram

TYPICAL EVALUATION TEST CIRCUIT (With Unloaded Outputs)



VOLTAGE LEVELS	
+ 5V	VDD
0V	VSS
+ 100V	HV_{POS}
0V	HV_{NEG}

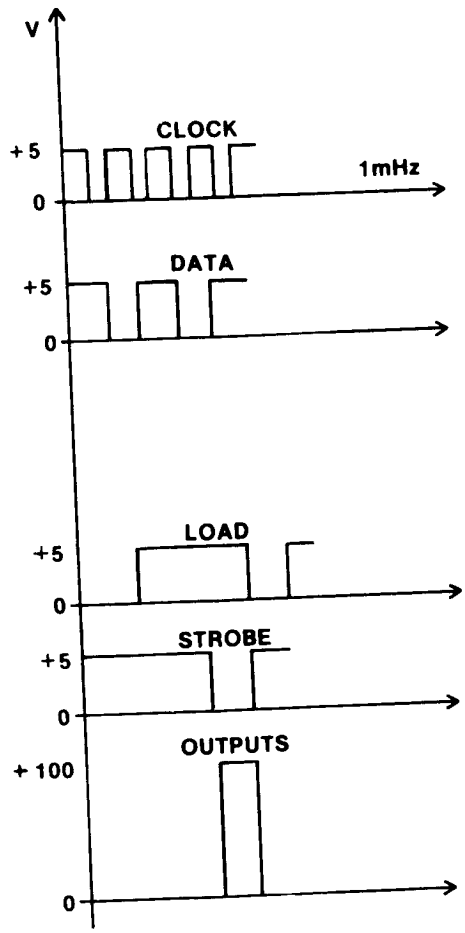


Fig. 8—LC1092A/B Typical Evaluation Test Circuit

TYPICAL AND RECOMMENDED OPERATING CHARACTERISTICS

(At 25°C unless otherwise specified)

CHARACTERISTICS	MIN.	TYP.	MAX.	UNIT
Supply Voltage (HV_{POS}) Supply Voltage (HV_{NEG})	VDD Gnd	— Gnd	100 Gnd	V V
Logic Supply Voltage (VDD)	4.75	5.00	5.25	V
Logic Common Voltage (VSS)	Gnd	Gnd	Gnd	V
High-Level Input Voltage	VDD-0.5	5.0	VDD+0.5	V
Low-Level Input Voltage	VSS	VSS	VSS+0.5	V
CLOCK Frequency	—	—	10	MHz
CLOCK Pulse Width Duration (Low or High Logic)	30	—	—	nsec
LOAD Pulse Width Duration	30	—	—	nsec
STROBE Frequency Frequency; 75 pf load on output	—	16	—	kHz
STROBE Duty Cycle; 75 pf load on output	—	25	—	%
Setup Time (See Figure 7) Data Inputs Before CLOCK Transition High Data Inputs After CLOCK Transition High Load Input After CLOCK Transition Low STROBE Input Low After LOAD Transition Low	 20 60 30 30	 — — — —	 — — — —	 nsec nsec nsec nsec
OUTPUT Rise Time 10% to 90%; 0 V to +100 V; Load Capacitance = 35 pF	—	—	0.5	μsec
OUTPUT Fall Time 10% to 90%; +100 V to 0 V; Load Capacitance = 35 pF	—	—	3.0	μsec
Pulsed Mode Supply Voltage (HV_{POS}): Voltage Frequency Supply Voltage (HV_{NEG}): Voltage Frequency	 VDD — −95 —	 — — — —	 +100 16 Gnd 16	 V kHz V kHz

FUNCTIONAL TABLE

Table 1.

FUNCTION	INPUTS				SHIFT REGISTER			DATA	LATCH			OUTPUTS		
	DATA	CLOCK	LOAD	STROBE	R1	R2	R3 . . . . . R32	OUT	L1	L2	L3 . . . . . L32	X0	X1	X2 . . X31
DATA IN	H	↑	H	H	H	$R1_n$	$R2_n$ . . . $R31_n$	$R32_n$	$L1_n$	$L2_n$	$L3_n$ . . . $L32_n$	L	L	L L
	L	↑	H	H	L	$R1_n$	$R2_n$ . . . $R31_n$	$R32_n$	$L1_n$	$L2_n$	$L3_n$ . . . $L32_n$	L	L	L L
LOAD	X	L	↓	H	R1	R2	R3 . . . . . R32	R32	$\overline{R1}$	$\overline{R2}$	$\overline{R3}$ . . . . . $\overline{R32}$	L	L	L L
STROBE	X	L	H	L	R1	R2	R3 . . . . . R32	R32	L1	L2	L3 . . . . . L32	$\overline{L1}$	$\overline{L2}$	$\overline{L3}$ . . $\overline{L32}$

H = High level. L = Low level. X = Don't care. ↑ = Low-to-high level transition. ↓ = High-to-low level transition.

R1 . . . R32 = Levels currently at internal outputs of shift register.

$R1_n$ . . . $R32_n$ = Levels at shift-register internal outputs (R1 . . . R32 respectively) before the most recent clock transition.

L1 . . . L32 = Levels currently at internal outputs of Latch.

$L1_n$ . . . $L32_n$ = Levels at Latch internal outputs (L1 . . . L32 respectively) before the most recent Load transition.