1.1W Mono Low-Voltage Audio Power Amplifier

Features

- **Operating Voltage : 2.6V-5.5V**
- **APA0713 Compatible with TPA751**
- **Supply Current**
  - **– I_{DD}=1.3mA at V_{DD}=5V ,BTL mode**
  - **– I_{DD}=0.9mA at V_{DD}=3.3V ,BTL mode**
- **Low Shutdown Current**
  - **– I_{DD}=0.1μA**
- **Low Distortion**
  - **– 630mW, at V_{DD}=5V, BTL, R_L=8Ω THD+N=0.15%**
  - **– 280mW, at V_{DD}=3.3V, BTL, R_L=8Ω THD+N=0.15%**
- **Output Power at 1% THD+N**
  - **– 900mW, at V_{DD}=5V, BTL, R_L=8Ω**
  - **– 400mW, at V_{DD}=3.3V, BTL, R_L=8Ω**

  at 10% THD+N
  - **– 1.1W at V_{DD}=5V, BTL, R_L=8Ω**
  - **– 480mW at V_{DD}=3.3V, BTL, R_L=8Ω**
- **Depop Circuitry Integrated**
- **Thermal Shutdown Protection and Over Current Protection Circuitry**
- **High supply voltage ripple rejection**
- **Surface-Mount Packaging**
  - **– 8 pin SOP**
- **Lead Free Available (RoHS Compliant)**

General Description

The APA0713 is a bridged-tied load (BTL) audio power amplifier developed especially for low-voltage applications where internal speakers operation is required. Operating with a 5V supply, the APA0713 can deliver 1.1W of continuous power into a BTL 8Ω load at 10% THD+N throughout voice band frequencies. Although this device is characterized out to 20kHz, its operation is optimized for narrow band applications such as wireless communications. The BTL configuration eliminates the need for external coupling capacitors on the output in most applications, which is particularly important for small battery-powered equipment. This device features a shutdown mode for power-sensitive applications with special depop circuitry to eliminate speaker noise when exiting shutdown mode. The APA0713 is available in8-pin SOP.

Applications

- **Mobil Phones**
- **PDAs**
- **Digital Cameras**
- **Portable Electronic Devices**

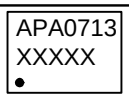
Ordering and Marking Information

APA0713 □□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

Package Code
K : SOP-8
Temperature Range
I : -40 to 85 °C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APA0713 K :



XXXXX - Date Code

Note : ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines “Green” to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

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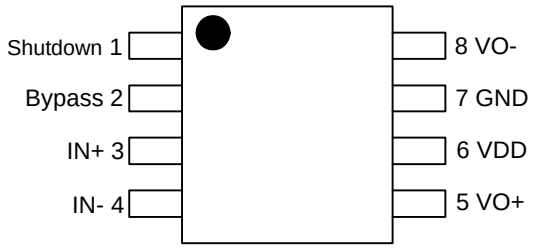
Pin Configuration



SOP-8

Absolute Maximum Ratings

(Over operating free-air temperature range unless otherwise noted.)

Symbol	Parameter	Rating	Unit
V_{DD}	Supply Voltage	-0.3 to 6	V
V_{IN}	Input Voltage Range, Shutdown, SE/$\overline{BTL}$	-0.3 to V_{DD}+0.3	V
T_A	Operating Ambient Temperature Range	-40 to 85	°C
T_J	Maximum Junction Temperature	Internally Limited*[1]	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_{SDR}	Lead Soldering Temperature, 10 seconds	260	°C
P_D	Power Dissipation	Internally Limited	W

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2 : APA0713 starts its internal thermal shutdown protection when junction temperature ramps up to 170°C.

Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{DD}	Supply Voltage		2.6	5.5	V
V_{IH}	High-Level Voltage	Shutdown	2.2		V
V_{IL}	Low-Level Voltage	Shutdown		0.4	V

Thermal Characteristics

Symbol	Parameter	Value	Unit
R_{THJA}	Thermal Resistance from Junction to Ambient in Free Air SOP-8 (Note 2)	200	°C/W

Note 2: 3.42in^2 printed circuit board with 20z trace and copper.

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Electrical Characteristics

Electrical Characteristics at Specified Free - Air Temperature

V_{DD} = 3.3V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA0713			Unit
			Min.	Typ.	Max.	
V_{OS}	Output Offset Voltage	R_L = 8Ω, R_F = 10kΩ			20	mV
I_{DD}	Supply Current	BTL mode, R_F = 10kΩ		0.9	1.8	mA
$I_{DD(SD)}$	Supply Current, Shutdown Mode	R_F = 10kΩ		0.1	2	µA
|IH|		Shutdown, $V_I = V_{DD}$			1	µA
|IL|		Shutdown, V_I = 0V			1	µA
Operating characteristic, V_{DD} = 3.3V, T_A = 25°C, RL = 8W						
P_O	Output Power (Note 3)	THD+N = 1%, BTL mode, R_L = 8Ω		400		mW
		THD+N = 1%, BTL mode, R_L = 4Ω		600		
THD+N	Total Harmonic Distortion Plus Noise (Note 1)	P_O = 280mW, BTL mode, R_L = 8Ω		0.15		%
Bom	Maximum Output Power Bandwidth	Gain = 2, THD+N = 2%		20		KHz
B1	Unity-Gain Bandwidth	Open Loop		2		MHz
PSRR	Power Supply Rejection Ratio (Note1)	C_B = 1µF, BTL mode, R_L = 8Ω		74		dB
Vn	Noise Output Voltage	Gain = 1, C_B = 0.1µF		28		µV(rms)
T_{WU}	Wake-up time	C_B = 1µF		380		ms

V_{DD} = 5V, T_A = 25°C (unless otherwise noted)

Symbol	Parameter	Test Conditions	APA0713			Unit
			Min.	Typ.	Max.	
V_{OS}	Output Offset Voltage	R_L = 8Ω, R_F = 10KΩ			20	mV
I_{DD}	Supply Current	BTL mode, R_F = 10 KΩ		1.3	2.6	mA
		SE mode, R_F = 10 KΩ		0.75	1.5	
$I_{DD(SD)}$	Supply Current, Shutdown Mode	R_F = 10 KΩ		0.1	2	µA
|IH|		Shutdown, $V_I = V_{DD}$			1	µA
|IL|		Shutdown, V_I = 0V			1	µA
Operating characteristic, V_{DD} = 5V, T_A = 25°C, R_L = 8W						
P_O	Output Power (Note 3)	THD+N = 1%, BTL mode, R_L = 8Ω		900		mW
		THD+N = 1%, BTL mode, R_L = 4Ω		1.5		W
THD+N	Total Harmonic Distortion Plus Noise (Note 3)	P_O = 630mW, BTL mode, R_L = 8Ω		0.15		%
Bom	Maximum Output Power Bandwidth	Gain = 2, THD+N = 2%		20		KHz
B1	Unity-Gain Bandwidth	Open Loop		2		MHz
PSRR	Power Supply Rejection Ratio (Note 3)	C_B = 1µF, BTL mode, R_L = 8Ω		74		dB
Vn	Noise Output Voltage	Gain = 1, C_B = 0.1µF		28		µV(rms)
Twu	Wake-up time	C_B = 1µF		400		ms

Note 3 : Output power is measured at the output terminals of device at f=1KHz.

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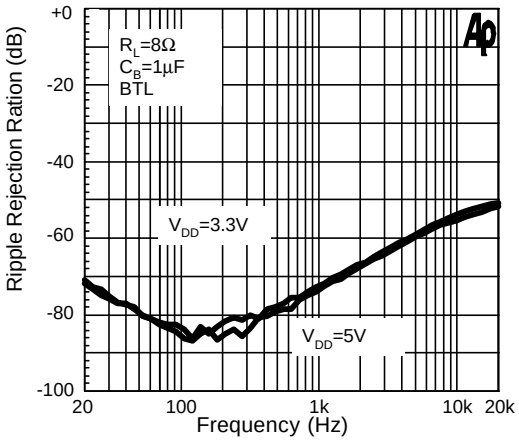
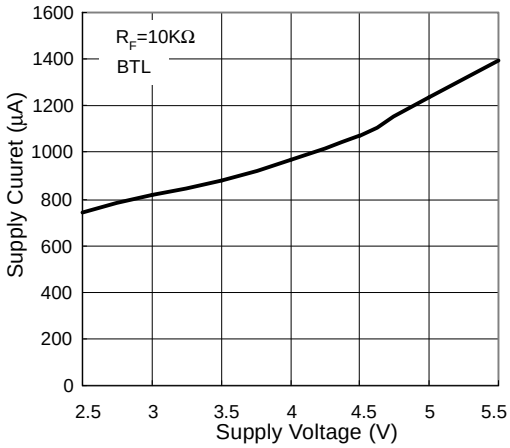
Typical Operating Characteristics

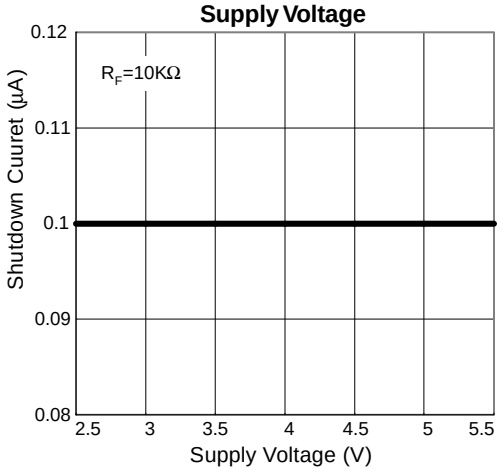
PSRR vs. Frequency



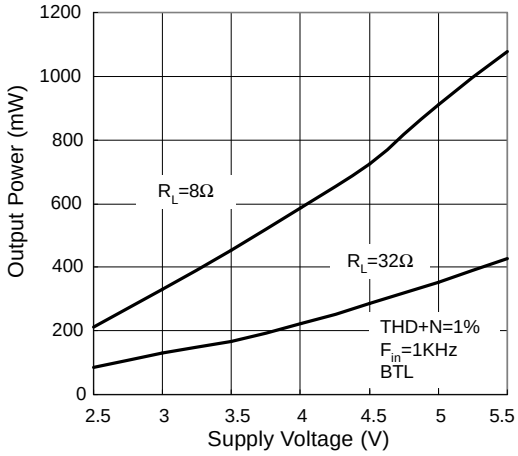
Supply Current vs. Supply Voltage



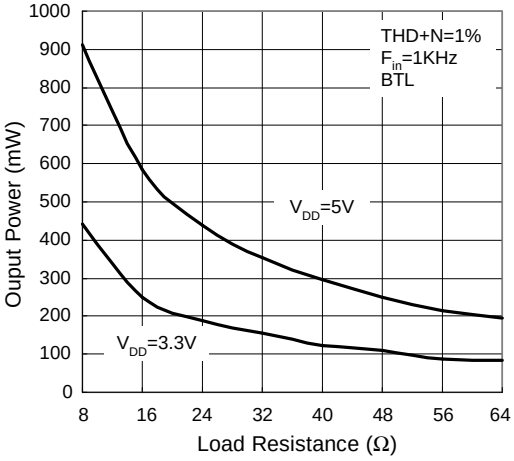
Shutdown Current vs. Supply Voltage



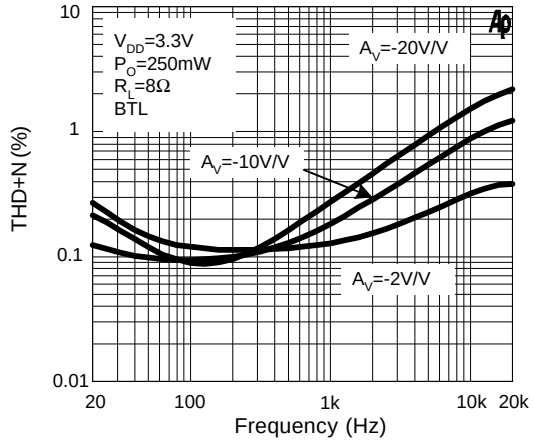
Output Power vs. Supply Voltage



Output Power vs. Load Resistance

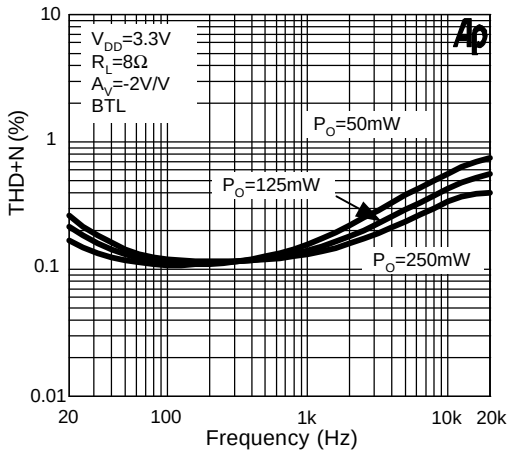


THD+N vs. Frequency

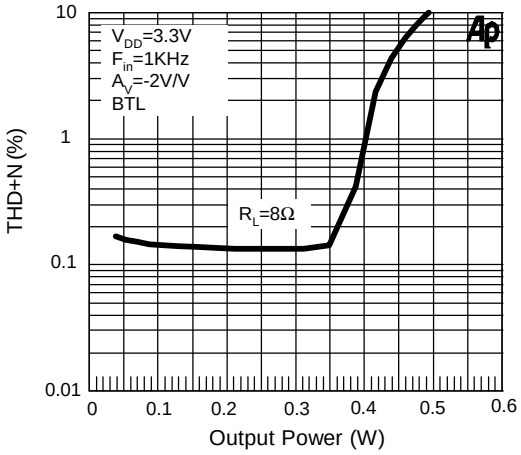


Typical Operating Characteristics (Cont.)

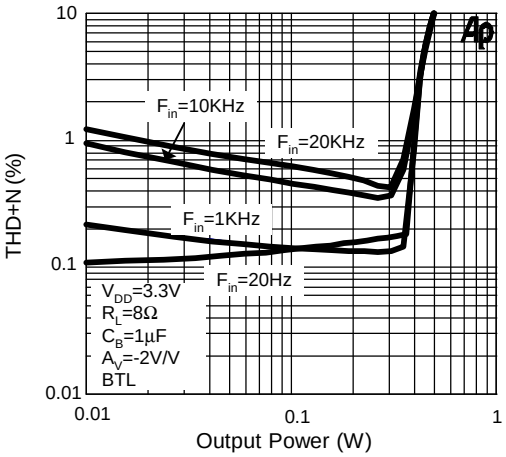
THD+N vs. Frequency



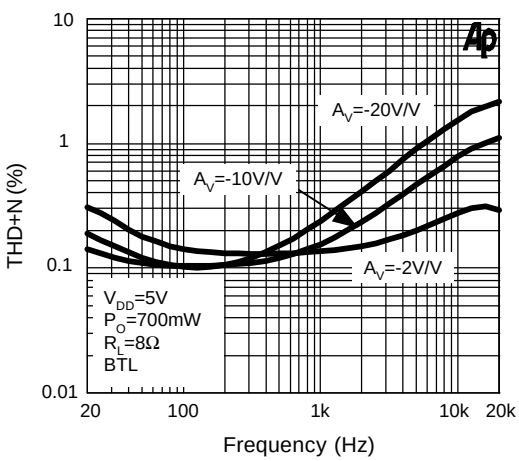
THD+N vs. Output Power



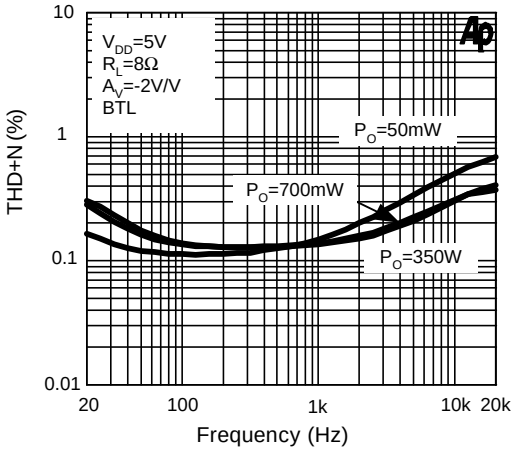
THD+N vs. Output Power



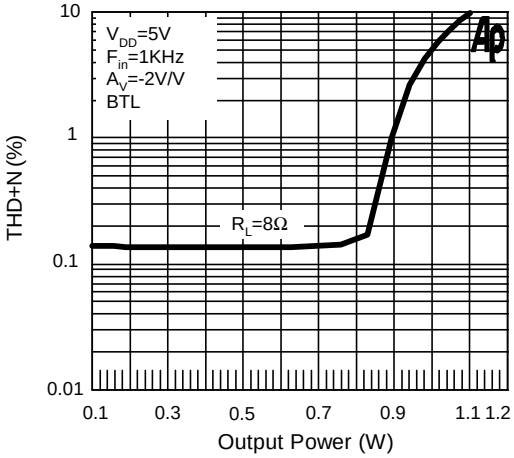
THD+N vs. Frequency



THD+N vs. Frequency



THD+N vs. Output Power



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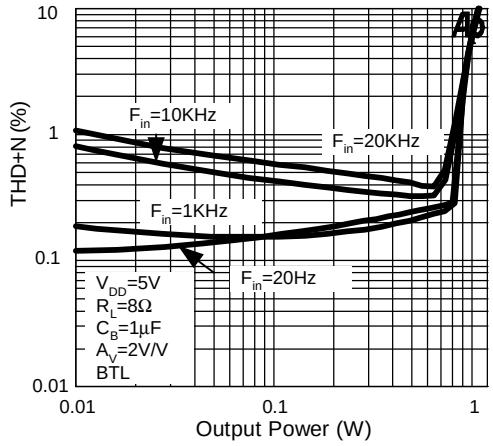
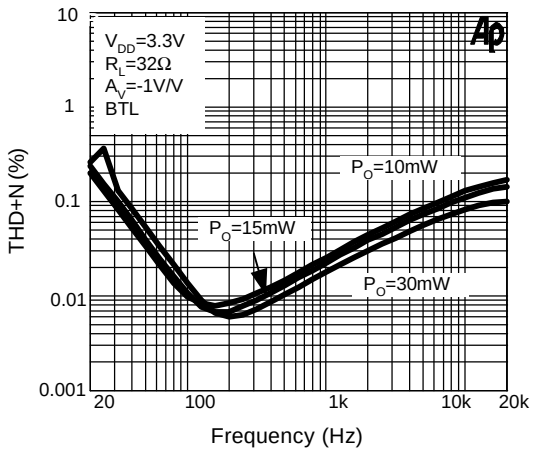
Typical Operating Characteristics (Cont.)

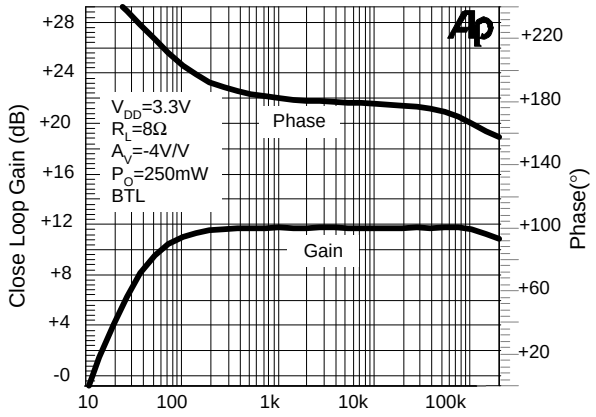
THD+N vs. Output Power



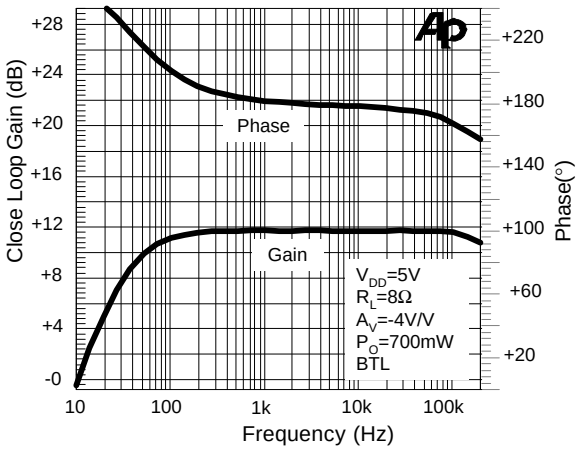
THD+N vs. Frequency



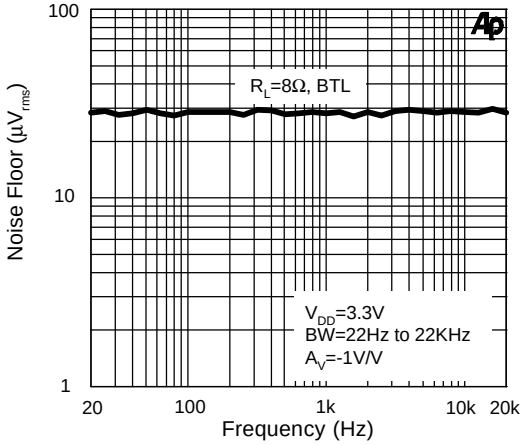
Close Loop Gain and Phase vs. Frequency



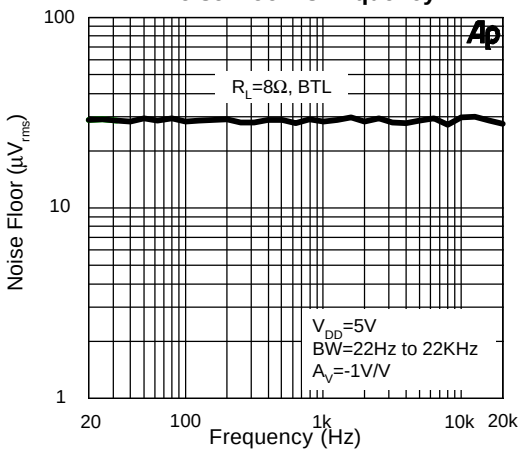
Close Loop Gain and Phase vs. Frequency



Noise Floor vs. Frquency

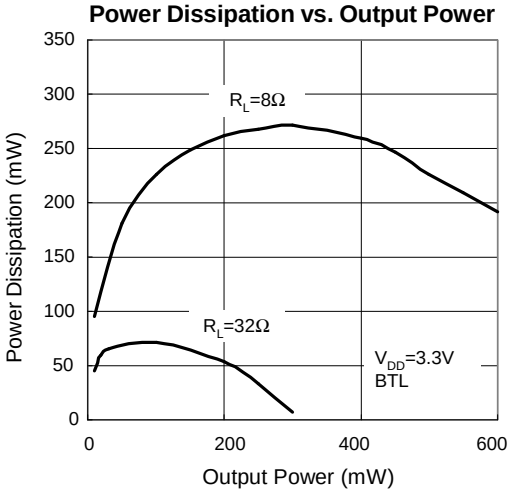


Noise Floor vs. Frquency

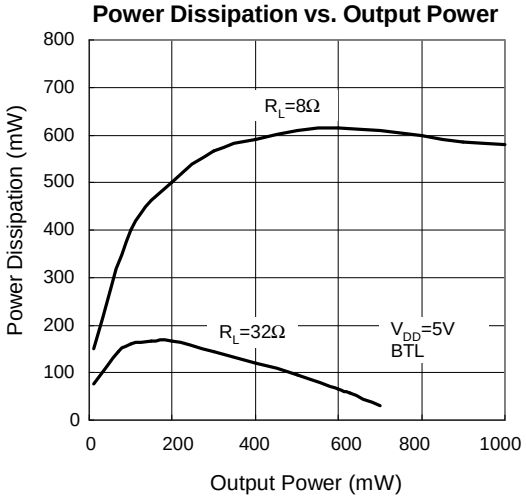


Typical Operating Characteristics (Cont.)

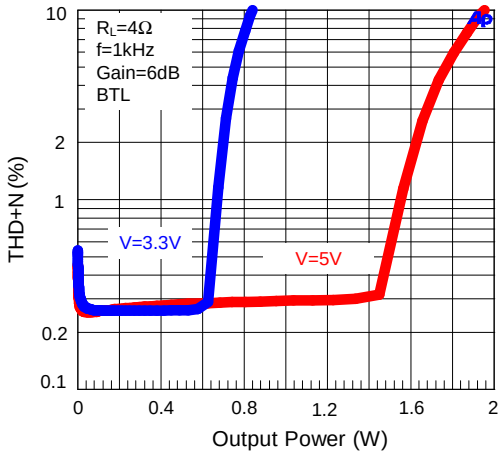
Power Dissipation vs. Output Power



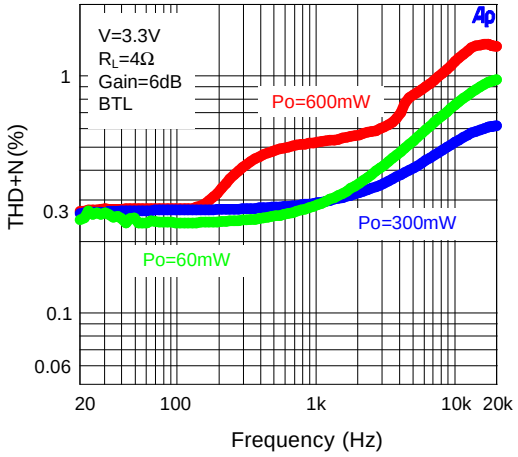
Power Dissipation vs. Output Power



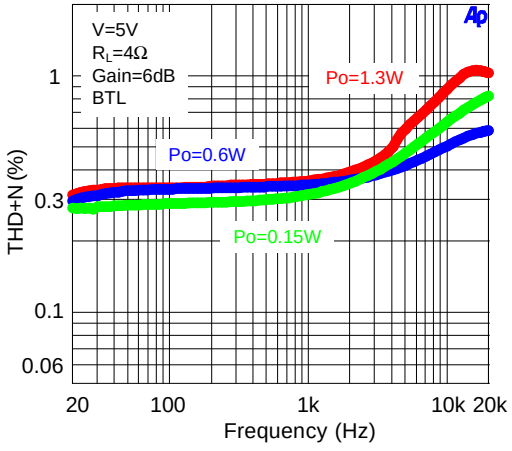
THD+N vs. Output Power



THD+N vs. Frequency



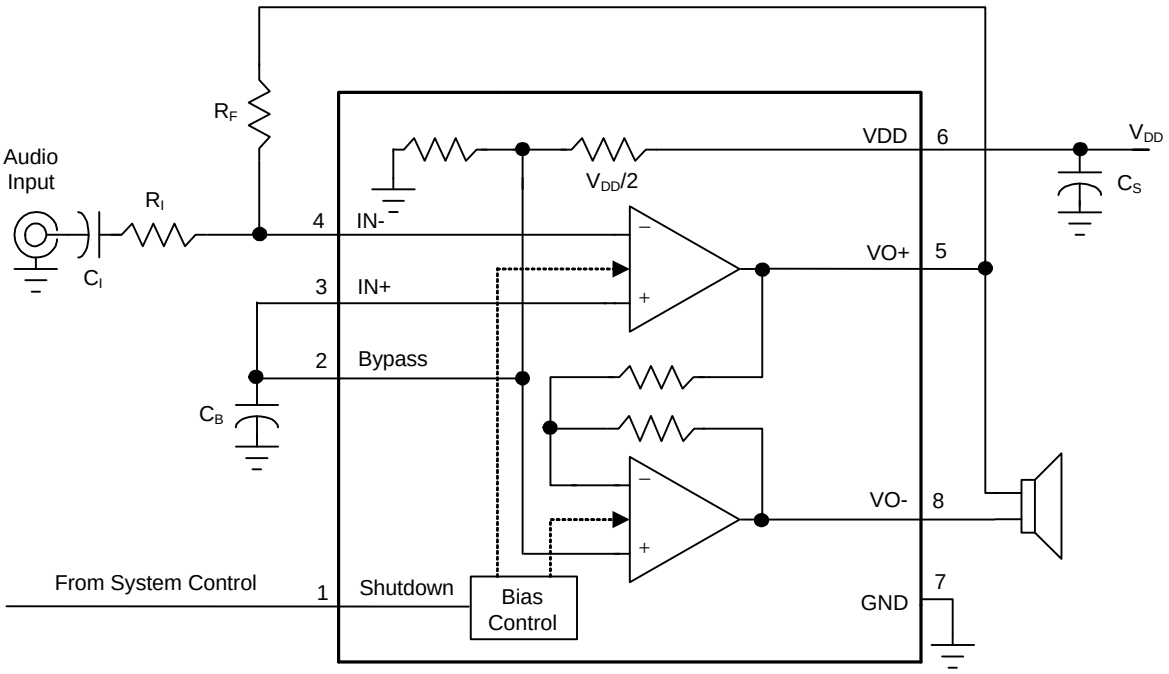
THD+N vs. Frequency



Pin Descriptions

Pin		I/O	Description
Name	No		
Shutdown	1	I	Shutdown mode control signal input, place entire IC in shutdown mode when held high.
Bypass	2	I	Bypass pin
IN+	3	I	IN+ is the non-inverting input. IN+ is typically tied to the Bypass terminal.
IN-	4	I	IN- is the inverting input. IN- is typically used as the audio input terminal.
VO+	5	O	VO+ is the positive BTL output.
VDD	6		Supply voltage input pin.
GND	7		Ground connection for circuitry.
VO-	8	O	VO- is the negative BTL output.

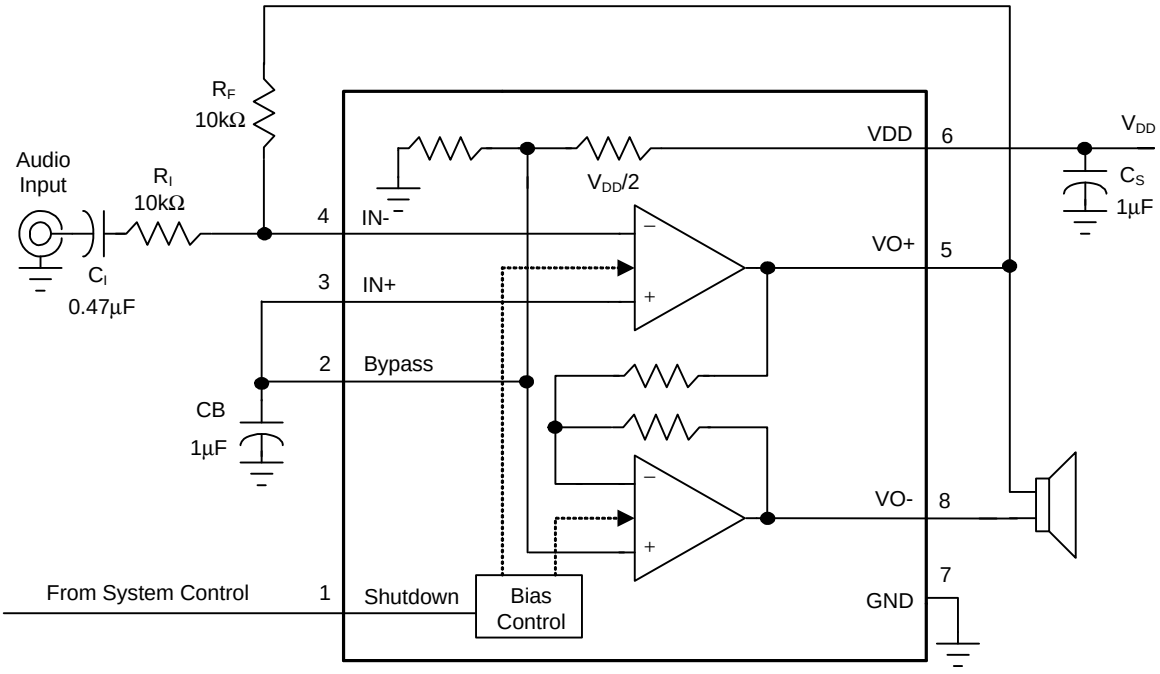
Block Diagram



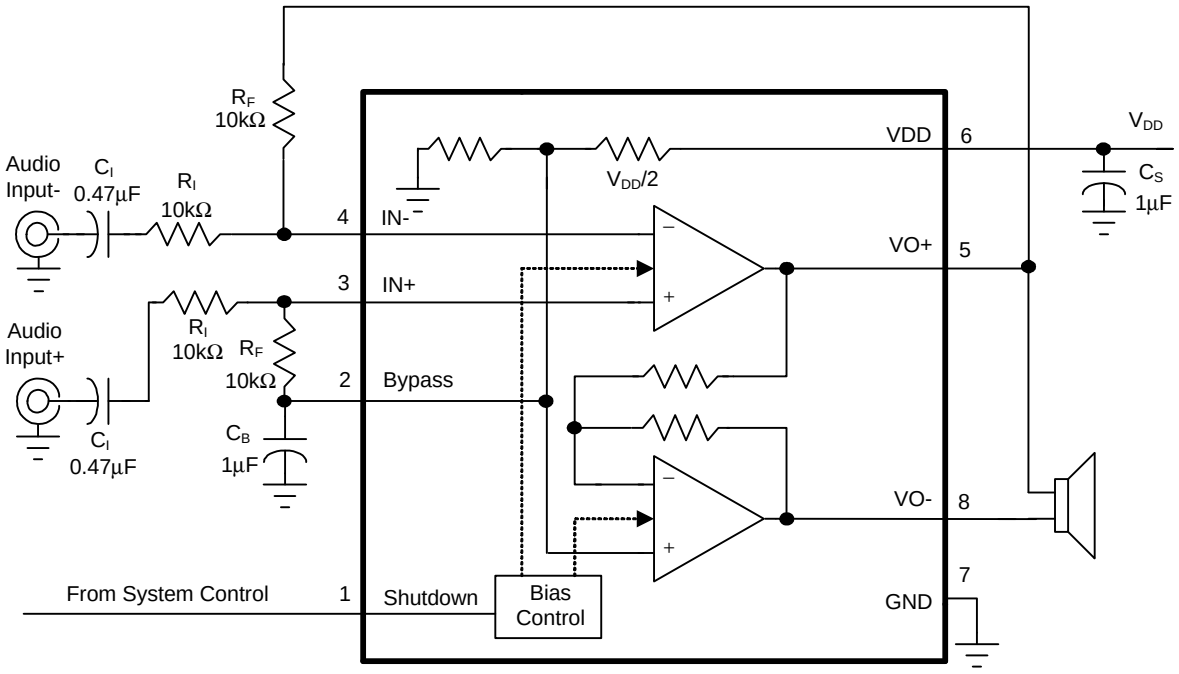
APA0713

Typical Application Circuits

For Single-ended Input Application



For Differential Input Application



Application Information

BTL Operation

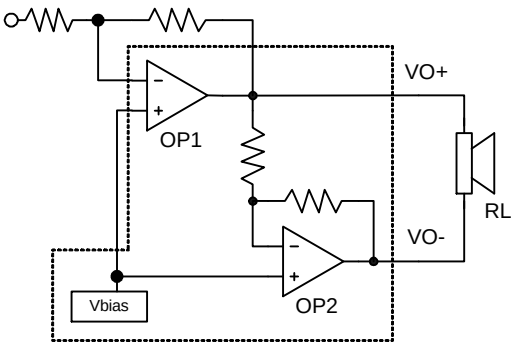


Figure 1: APA0713 power amplifier internal configuration

The power amplifier OP1 gain is set by external gain setting, while the second amplifier OP2 is internally fixed in a unity-gain, inverting configuration. Figure 1 shows that the output of OP1 is connected to the input to OP2, which results in the output signals of with both amplifiers with identical in magnitude, but out of phase 180°. Consequently, the differential gain for each channel is 2X (Gain of SE mode).

By driving the load differentially through outputs VO+ and VO-, an amplifier configuration commonly referred to as bridged mode is established. The BTL mode operation is different from the classical single-ended SE amplifier configuration where one side of its load is connected to ground.

The BTL amplifier design has a few distinct advantages over the SE configuration, as it provides differential drive to the load, thus doubling the output swing for a specified supply voltage.

Four times the output power is possible as compared with a SE amplifier under the same conditions. A BTL configuration, such as the one used in the APA0713, also creates a second advantage over SE amplifiers. Since the differential outputs, VO+ and VO-, are biased at half-supply, no need DC voltage exists across the load. This eliminates the need for an output coupling capacitor which is required in a single supply, SE configuration.

Input Capacitor, C_I

In the typical application, an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper DC level for optimum operation. In this case, C_I and the minimum input impedance R_I from a high-pass filter with the corner frequency are determined in the following equation :

$$F_C(highpass) = \frac{1}{2\pi R_I C_I} \quad (1)$$

The value of C_I is important to consider as it directly affects the low frequency performance of the circuit. Consider the example where R_I is 100KΩ and the specification calls for a flat bass response down to 40Hz. Equation is reconfigured as followed :

$$C_I = \frac{1}{2\pi R_I F_C} \quad (2)$$

Consider input resistance variation, the C_I is 0.04µF so one would likely choose a value in the range of 0.1µF to 1.0µF.

A further consideration for this capacitor is the leakage path from the input source through the input network (R_I+R_F, C_I) to the load.

This leakage current creates a DC offset voltage at the input to the amplifier that reduces useful headroom, especially in high gain applications. For this reason, a low-leakage tantalum or ceramic capacitor is the best choice. When polarized capacitors are used, the positive side of the capacitor should face the amplifier input in most applications as the DC level there is held at $V_{DD}/2$, which is likely higher than the source DC level. Please note that it is important to confirm the capacitor polarity in the application.

Effective Bypass Capacitor, C_{bypass}

As other power amplifiers, proper supply bypassing is critical for low noise performance and high power supply rejection.

The capacitors located on the bypass and power supply pins should be as close to the device as possible. The effect of a larger half supply bypass capacitor will improve

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Application Information (Cont.)

Effective Bypass Capacitor, C_{bypass} (Cont.)

PSRR due to increased half-supply stability. Typical application employs a 5V regulator with 1.0µF and a 0.1µF bypass as supply filtering. This does not eliminate the need for bypassing the supply nodes of the APA0713. The selection of bypass capacitors, especially C_{bypass}, thus depends upon desired PSRR requirements, click- and-pop performance.

To avoid start-up pop noise occurred, the bypass voltage should rise slower than the input bias voltage and the relationship shown in equation (4) should be maintained.

$$\frac{1}{C_{bypass} \times 80K\Omega} << \frac{1}{(R_I + R_F) \times C_I} \quad (3)$$

The bypass capacitor is fed from a 80KΩ resistor inside the amplifier. Bypass capacitor, C_{bypass}, values of 0.1µF to 2.2µF ceramic or tantalum low-ESR capacitors are recommended for the best THD+N and noise performance.

The bypass capacitance also effects to the start up time. It is determined in the following equation :

$$T_{startup} = 5 \times (C_{bypass} \times 80K\Omega) \quad (4)$$

Power Supply Decoupling, C_S

The APA0713 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD+N) is as low as possible. Power supply decoupling also prevents the oscillations causing by long lead length between the amplifier and the speaker. The optimum decoupling is achieved by using two different types of capacitors that target on different types of noise on the power supply leads. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1µF, is placed as close as possible to the device's VDD lead, which is for the best performance. For filtering lower-frequency noise signals, a large aluminum electrolytic capacitor of 10µF or greater placed near the audio power amplifier is recommended.

Optimizing Depop Circuitry

Circuitry has been included in the APA0713 to minimize the amount of popping noise at power-up and when coming out of shutdown mode. Popping occurs whenever a voltage step is applied to the speaker. In order to eliminate click-and-pop, all capacitors must be fully discharged before turn-on. Rapid on/off switching of the device or the shutdown function will cause the click-and-pop circuitry. The value of C_I will also affect turn-on pops (refer to Effective Bypass Capacitance). The bypass voltage rise up should be slower than input bias voltage.

Although the bypass pin current source cannot be modified, the size of C_{bypass} can be changed to alter the device turn-on time and the amount of click-and-pop. By increasing the value of C_{bypass}, turn-on pop can be reduced. However, the tradeoff for using a larger bypass capacitor is to increase the turn-on time for this device. There is a linear relationship between the size of C_{bypass} and the turn-on time.

In the most cases, choosing a small value of C_I in the range of 0.33µF to 1µF, C_{bypass} being equal to 1µF should produce a virtually clickless and popless turn-on.

A high gain amplifier intensifies the problem as the small delta in voltage is multiplied by the gain. Hence, it is advantageous to use low-gain configurations.

Shutdown Function

In order to reduce power consumption while not in using, the APA0713 contains a shutdown function to externally turn off the amplifier bias circuitry. This shutdown feature turns the amplifier off when a logic low on the Shutdown pin for APA0713.

The trigger point between a logic high and logic low level is typically $0.4V_{DD}$. It's better to switch between ground and the supply voltage V_{DD} to provide maximum device performance.

By switching the Shutdown pin to high level, the amplifier enters a low-current state, I_{DD} for APA0713. APA0713 is in shutdown mode. In normal operation, APA0713's Shutdown pin should be pulled to low level to keep the IC

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Application Information (Cont.)

Shutdown Function (Cont.)

out of the shutdown mode. The Shutdown pin should be tied to a definite voltage to avoid unwanted state changes.

BTL Amplifier Efficiency

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency} = \frac{P_O}{P_{SUP}} \quad (5)$$

Where

$$P_O = \frac{V_{orms} \times V_{orms}}{R_L} = \frac{(V_P \times V_P)}{2R_L}$$

$$V_{orms} = \frac{V_P}{\sqrt{2}} \quad (6)$$

$$P_{SUP} = V_{DD} \times L_{DD,AVG} = V_{DD} \times \frac{2V_P}{\pi R_L} \quad (7)$$

Efficiency of a BTL configuration :

$$\frac{P_O}{P_{SUP}} = \frac{(\frac{V_P \times V_P}{2R_L})}{(V_{DD} \times \frac{2V_P}{\pi R_L})} = \frac{\pi V_P}{4V_{DD}} \quad (8)$$

Po (W)	Efficiency (%)	V_P(V)	P_D (W)
0.125	33.6	1.41	0.26
0.25	47.6	2.00	0.29
0.375	58.3	2.45*	0.28

*High peak voltages cause the THD+N to increase.

Table 1. Efficiency vs. Output Power in 3.3V/8Ω BTL Systems.

Table 1 employs equation 8 to calculate efficiencies for three different output power levels when load is 8Ω.

The efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a mono 900mW audio system with 8Ω loads and a 5V supply, the maximum draw on the power supply is almost 1.5W.

A final point to remember about linear amplifiers (either SE or BTL) is how to manipulate the terms in the efficiency equation to utmost advantage when possible. Note that in equation8, V_{DD} is in the denominator.

This indicates that as V_{DD} goes down, efficiency goes up. In other words, the efficiency analysis is used to choose the correct supply voltage and speaker impedance for the application.

Power Dissipation

Whether the power amplifier is operated in BTL or SE modes, power dissipation is a major concern. In equation9 states the maximum power dissipation point for a SE mode operating at a given supply voltage and driving a specified load.

$$\text{SE mode}: P_{D,MAX} = \frac{V_{DD}^2}{2\pi^2 R_L} \quad (9)$$

In BTL mode operation, the output voltage swing is doubled as in SE mode. Thus the maximum power dissipation point for a BTL mode operating at the same given conditions is 4 times as in SE mode.

$$\text{BTL mode}: P_{D,MAX} = \frac{4V_{DD}^2}{2\pi^2 R_L} \quad (10)$$

Since the APA0713 is a mono channel power amplifier, the maximum internal power dissipation is equal to the both of equations depending on the mode of operation. The power dissipation from equation10, assuming a 5V-power supply and an 8Ω load, must not be greater than the power dissipation that results from the equation11:

$$P_{D,MAX} = \frac{T_{J,MAX} - T_A}{\theta_{JA}} \quad (11)$$

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Application Information (Cont.)

Power Dissipation (Cont.)

For SOP-8 package, the thermal resistance (θ_{JA}) is equal to 200°C/W, respectively.

Since the maximum junction temperature ($T_{J,MAX}$) of APA0713 is 170°C and the ambient temperature (T_A) is defined by the power system design, the maximum power dissipation which the IC package is able to handle can be obtained from equation 11. Once the power dissipation is greater than the maximum limit ($P_{D,MAX}$), either the supply voltage (V_{DD}) must be decreased, the load impedance (R_L) must be increased, or the ambient temperature should be reduced.

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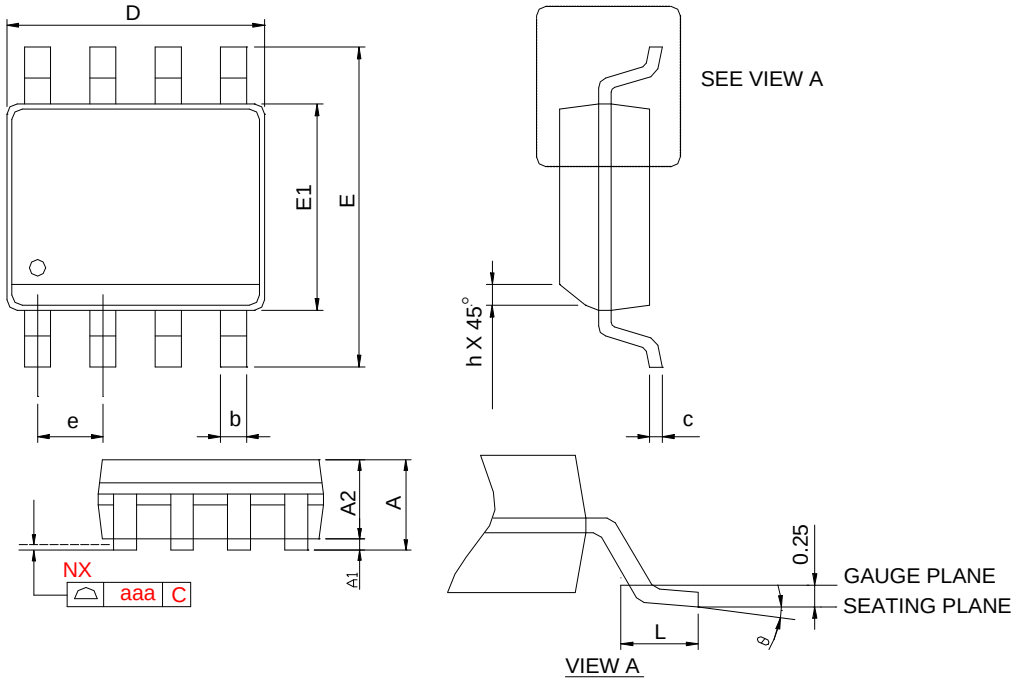
Package Information

SOP-8



SYMBOL	SOP-8			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A		1.75		0.069
A1	0.10	0.25	0.004	0.010
A2	1.25		0.049	
b	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
h	0.25	0.50	0.010	0.020
L	0.40	1.27	0.016	0.050
θ	0°	8°	0°	8°
aaa	0.10		0.004	

Note: 1. Follow JEDEC MS-012 AA.
2. Dimension “D” does not include mold flash, protrusions or gate burrs.
Mold flash, protrusion or gate burrs shall not exceed 6 mil per side.
3. Dimension “E” does not include inter-lead flash or protrusions.
Inter-lead flash and protrusions shall not exceed 10 mil per side.

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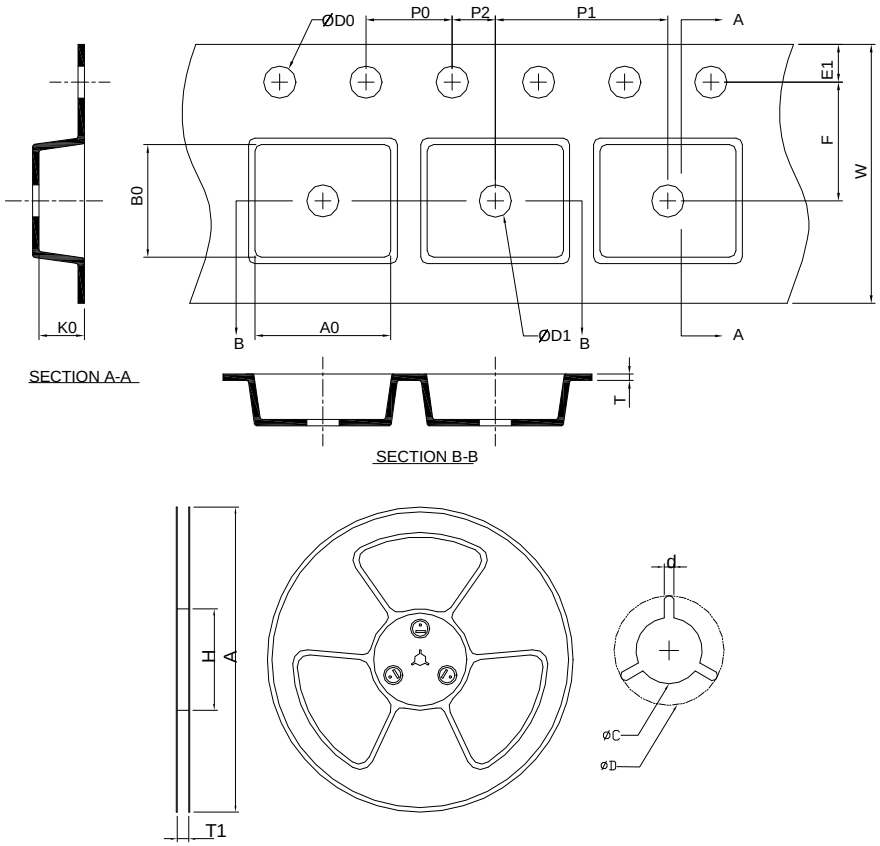
Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
SOP-8	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	6.40±0.20	5.20±0.20	2.10±0.20

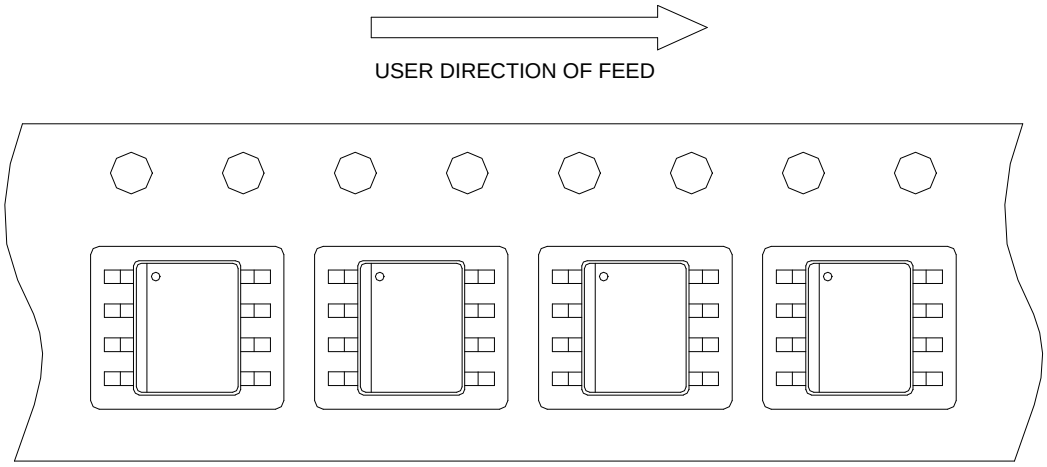
(mm)

Devices Per Unit

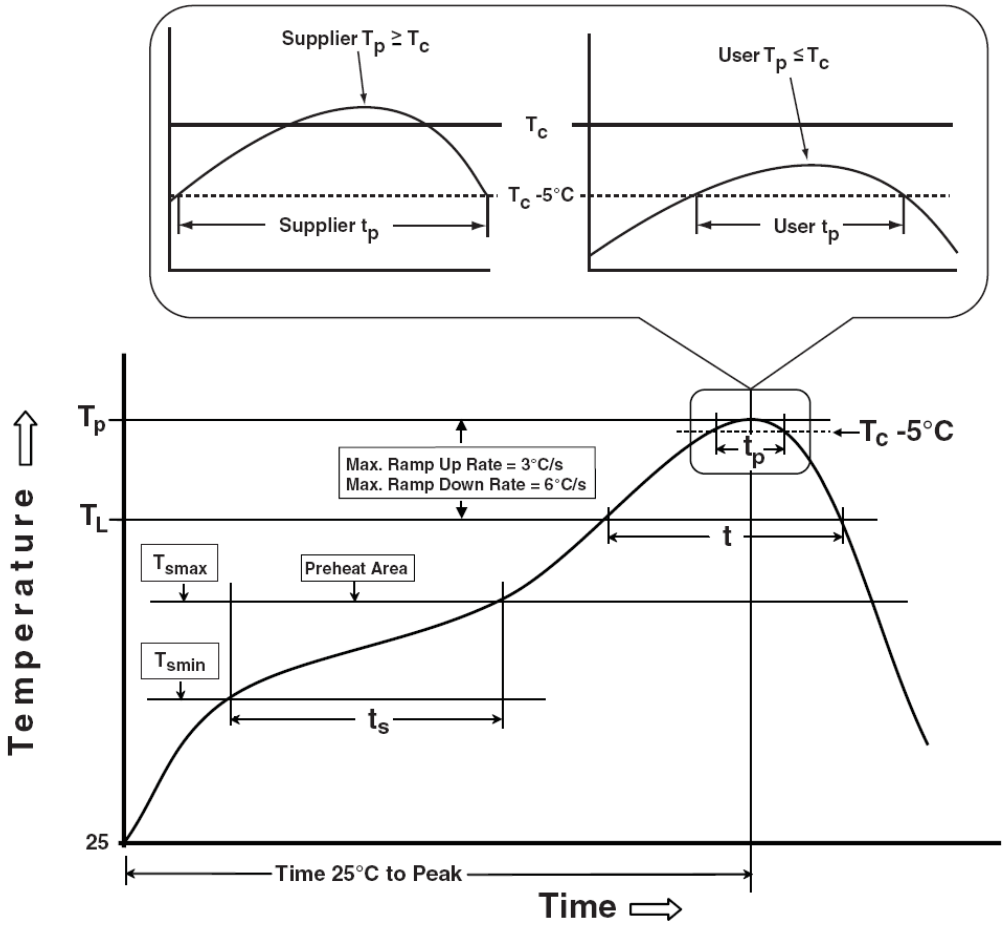
Package Type	Unit	Quantity
SOP-8	Tape & Reel	2500

Taping Direction Information

SOP-8



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	 100 °C 150 °C 60-120 seconds	 150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ Tj=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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