LH57256/J

CMOS 256K (32K × 8) OTPROM/EPROM

FEATURES

- 32,768 × 8 bit organization
- Access times:
  LH57256J: 120/150 ns
  LH57256: 150 ns
- Single +5 V power supply
- High speed programming:
  t_{PW} = 0.1 ms (V_{PP} = 12.75 V) or
  t_{PW} = 1 ms (V_{PP} = 12.5 V)
  Compatible to INTEL quick pulse programming™ algorithm
  (4 second programming)
- Low power consumption :
  Operating: 165 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully static operation
- Three-state outputs
- TTL compatible I/O
- Pin compatible with i27256
- Packages:
  EPROM
  28-pin, 600-mil CERDIP
  OTPROM
  28-pin, 600-mil DIP
  28-pin, 300-mil SK-DIP
  28-pin, 450-mil SOP
- JEDEC standard pinout (CERDIP/DIP)

DESCRIPTION

The LH57256J is a CMOS UV erasable and electrically programmable read-only-memory organized as 32,768 × 8 bits. It is pin compatible with the Intel i27256, and designed to have fast access time.

The LH57256 is a one-time PROM packaged in plastic DIP.

PIN CONNECTIONS

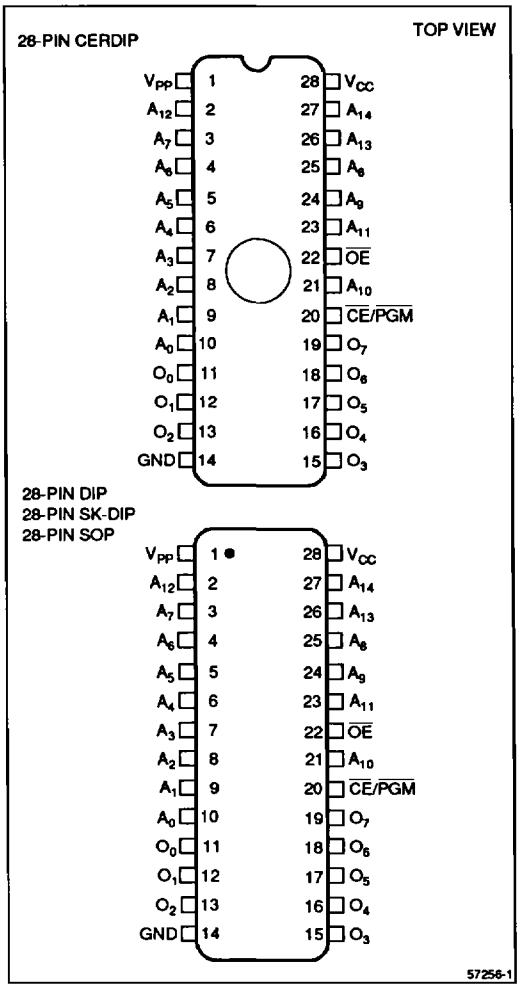

Figure 1. Pin Connections for CERDIP, DIP, SK-DIP, and SOP Packages

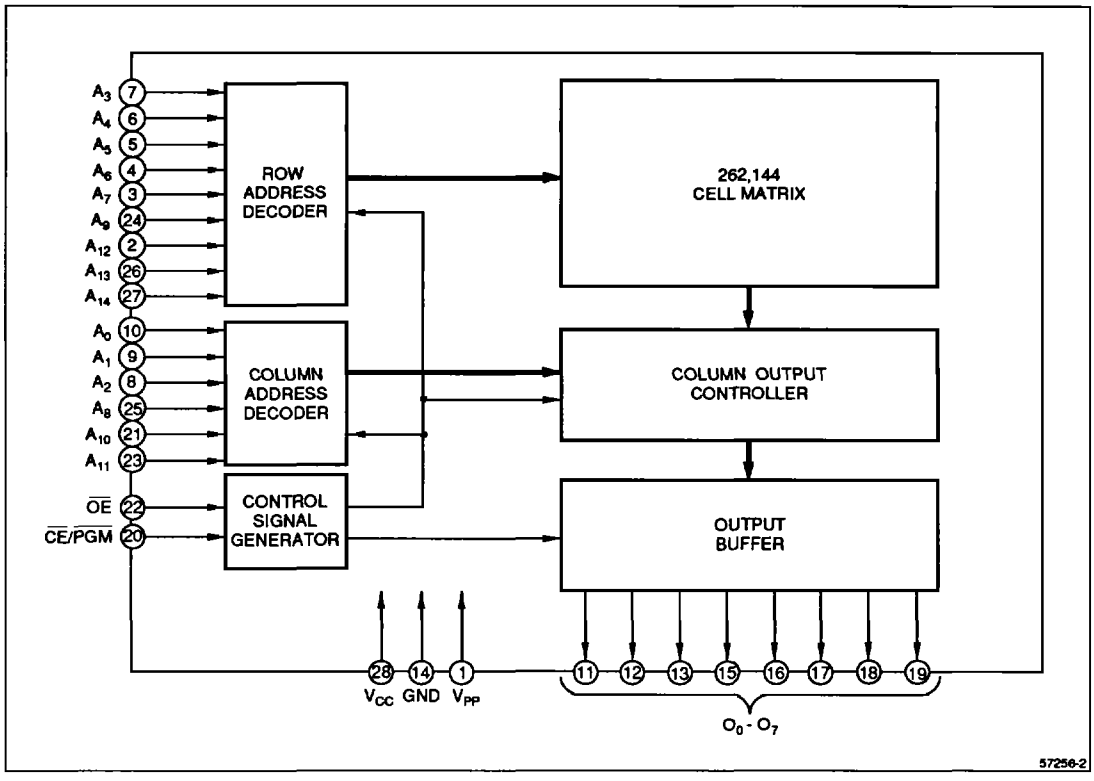

Figure 2. LH57256/J Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{14}	Address input	
O_0 - O_7	Data output (input)	1
$\overline{CE}/\overline{PGM}$	Chip Enable/Program input	
$\overline{OE}$	Output Enable input	

SIGNAL	PIN NAME	NOTE
V_{PP}	Program power	
V_{CC}	Power supply	
GND	Ground	

NOTE:
1. O_0 - O_7 pins are also used to input data to the column output controller through input buffers in programming mode.

TRUTH TABLE

MODE		O_0 - O_7	$\overline{CE}/\overline{PGM}$	$\overline{OE}$	V_{CC}	V_{PP}
Read	Read	Data out	L	L	+5 V	+5 V
	Output disable	High-Z	L	H	+5 V	+5 V
	Standby	High-Z	H	X	+5 V	+5 V
Program	Program	Data in	L	H	+6.25 V	+12.75 V
	Program verify	Data out	H	L	+6.25 V	+12.75 V
	Program inhibit	High-Z	H	H	+6.25 V	+12.75 V

NOTE:
X = H or L, H = V_{IH}, L = V_{IL}

ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.6 to +7.0	V	1
	V_{PP}	-0.6 to +13.5		
	V_{IN}, V_{OUT}	-0.6 to +7.0		
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-65 to +150	°C	2
		-55 to +150		3

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
   Maximum ratings are those values beyond which damage to the device may occur.
2. Applied to ceramic package.
3. Applied to plastic package.

RECOMMENDED OPERATING CONDITIONS (Read Mode) (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	V_{PP}	4.5	5.0	5.5	
Input "Low" voltage	V_{IL}	-0.1		0.8	V
Input "High" voltage	V_{IH}	2.2		V_{CC} +0.3	V

DC CHARACTERISTICS (Read Mode) (V_{CC} = 5 V ± 10%, V_{PP} = V_{CC}, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.1		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	I_{LI}	V_{IN} = GND or V_{CC}	-10		10	µA	
Output leakage current	I_{LO}	V_{OUT} = GND or V_{CC}	-10		10	µA	
V_{CC} operating current	I_{CC1}	$\overline{CE}/\overline{PGM}$ = GND ± 0.3 V			30	mA	1, 2
	I_{CC2}	$\overline{CE}/\overline{PGM}$ = V_{IL}			30	mA	1, 3
V_{PP} supply current	I_{PP}	V_{PP} = V_{CC}			100	µA	
V_{PP} pin voltage	V_{PP}		V_{CC} - 0.4		V_{CC}	V	
V_{CC} standby current	I_{SB1}	$\overline{CE}/\overline{PGM}$ = V_{CC} ± 0.3 V			100	µA	
	I_{SB2}	$\overline{CE}/\overline{PGM}$ = V_{IH}			2	mA	

NOTES:
1. Minimum cycle time, I_{OUT} = 0 mA
2. CMOS level: V_{IN} = GND ± 0.3 V or V_{CC} ± 0.3 V
3. TTL level: V_{IN} = V_{IL} or V_{IH}

AC CHARACTERISTICS (Read Mode) (V_{CC} = V_{PP} = 5 V ± 10%. T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH57256J-12		LH57256J-15 LH57256-15		UNIT
		MIN.	MAX.	MIN.	MAX.	
Address to output delay	t_{ACC}		120		150	ns
$\overline{CE}$ to output delay	t_{CE}		120		150	ns
$\overline{OE}$ to output delay	t_{OE}		25		30	ns
Output enable high to output float	t_{DF}	0	25	0	30	ns
Address to output hold	t_{OH}	0		0		ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.45 V to 2.4 V
Input rise/fall time	≤ 10 ns
Input reference level	1 V, 2 V
Output reference level	0.8 V, 2 V

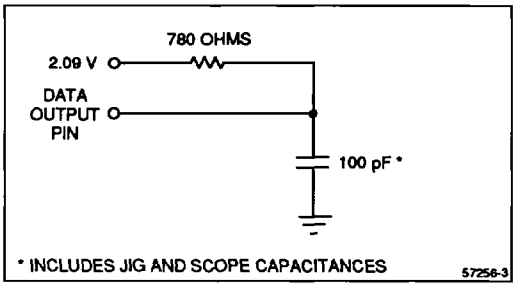

Figure 4. Output Load Circuit

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V		4	6	pF
Output capacitance	C_{OUT}	V_{OUT} = 0 V		8	12	pF

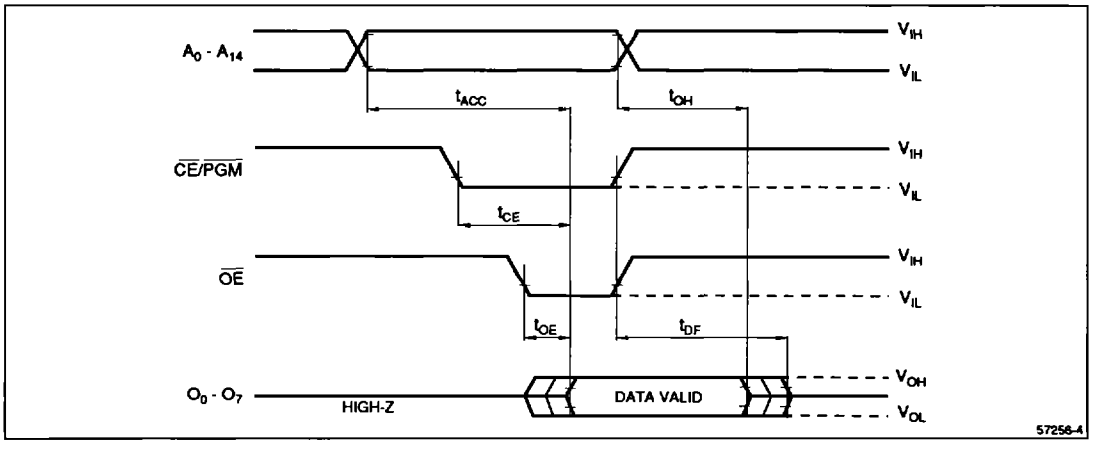

Figure 3. Timing Diagram (Read Mode)

RECOMMENDED OPERATING CONDITIONS (Program Mode) (T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	5.75	6.25	6.5	V
	V_{PP}	12.2	12.75	13.0	
Input "Low" voltage	V_{IL}	-0.1		0.45	V
Input "High" voltage	V_{IH}	2.4		V_{CC} + 0.3	V

DC CHARACTERISTICS (Program Mode)

(V_{CC} = 5.75 V to 6.5 V, V_{PP} = 12.2 V to 13 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	I_{LI}	$V_{IN} = V_{CC}$ or 0.45 V	-10		10	µA
V_{CC} supply current	I_{CC}				30	mA
V_{PP} supply current	I_{PP}	$\overline{CE}/\overline{PGM} = V_{IL}$			30	mA
Input "Low" voltage	V_{IL}		-0.1		0.45	V
Input "High" voltage	V_{IH}		2.4		V_{CC} + 0.3	V
Output "Low" voltage	V_{OL}	I_{OL} = 2.1 mA			0.45	V
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V

AC CHARACTERISTICS (Program mode)

(V_{CC} = 6.25 V ± 0.25 V, V_{PP} = 12.75 V ± 0.25 V, T_A = 25°C ± 5°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Address setup time	t_{AS}	2			µs	
Data setup time	t_{DS}	2			µs	
Output enable setup time	t_{OES}	2			µs	
Address hold time	t_{AH}	0			µs	
Data hold time	t_{DH}	2			µs	
Output enable time	t_{OE}			150	ns	
Output disable time	t_{DF}	0		150	ns	
V_{PP} setup time	t_{VPS}	2			µs	
V_{CC} setup time	t_{VCS}	2			µs	
Program pulse width	t_{PW}	95	100	105	µs	1,2
Program pulse count	N	1		25	TIMES	

NOTES:

1. Programmable under conditions of add. program pulse count 3-N, V_{CC} = 6 V ± 0.25 V, V_{PP} = 12.5 V ± 0.3 V, t_{pw} = 1 ms ± 0.05 ms
2. This width is defined by the Program Flowchart (Figure 6).

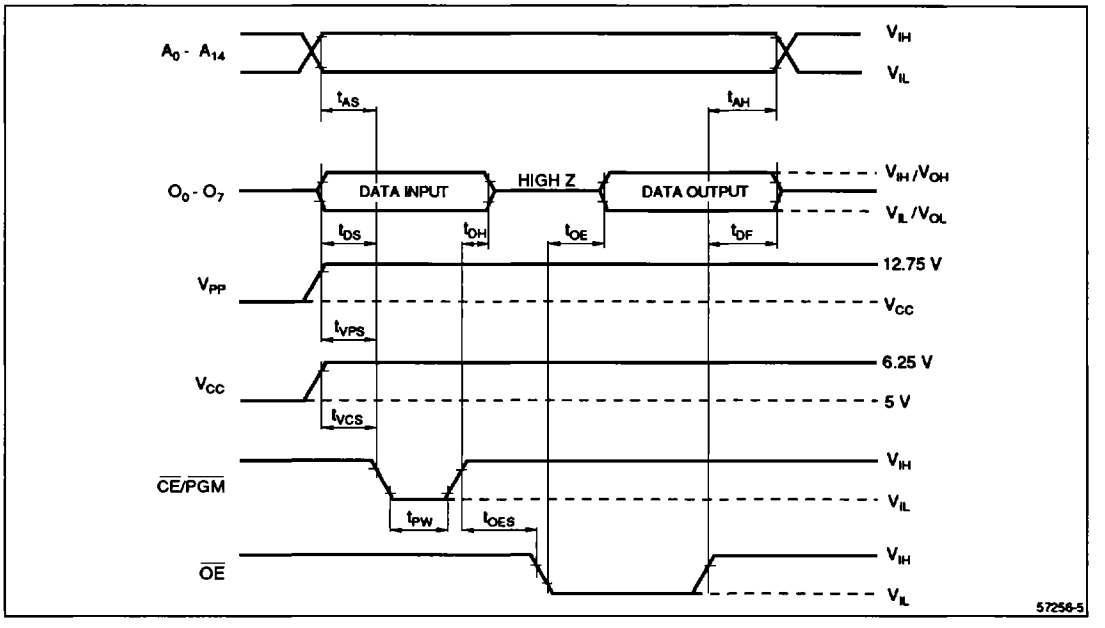

Figure 5. Timing Diagram (Program Mode)

PROGRAMMING

Upon delivery from SHARP or after each erasure (see erasure section), the LH57256 and LH57256J have all 32,768 × 8 bits in the "1", or high state. "0's" are loaded into the LH57256 and LH57256J through the procedure of programming.

The programming mode is entered when +12.75 V is applied to the V_{PP} pin and $\overline{CE}/\overline{PGM}$ is at V_{IL}. A 0.1 µF capacitor between V_{PP} and GND is needed to prevent excessive voltage transients, which could damage the device. The address to be programmed is applied to the proper address pins. 8-bit patterns are placed on the respective data pins. The voltage levels should be standard TTL levels.

ERASURE

In order to clear all locations of their programmed contents, it is necessary to expose the LH57256J to an ultra-violet light source. A dosage of 15 W-second/cm^2 is required to completely erase an LH57256J. This dosage can be obtained by exposure to an ultra-violet lamp (wave-length of 2,537 Angstroms (Å)) with intensity of 12,000 µW/cm^2 for 20 to 30 minutes. The LH57256J should be about one inch from the source and all filters should be removed from the UV light source prior to erasure.

It is important to note that the LH57256J and similar devices will erase with light sources having wave-length shorter than 4,000 Å. Although erasure times will be much longer than with UV sources at 2,537 Å, the exposure to fluorescent light and sunlight will eventually erase the LH57256J and exposure to them should be prevented to realize maximum system reliability. If used in such an environment, the package windows should be covered by an opaque label or substance.

CAUTION

Fluorescent light and sunlight contain UV rays which will erase the EPROM. To prevent deterioration of EPROM data due to UV rays, it is recommended that EPROMs should not be left under direct sunlight or fluorescent light, or the package window should be covered with an opaque material.

Care must be taken to avoid friction between package window and plastics or the like, as the resulting static-electric build-up may cause faulty operation.

1. V_{CC} must be applied either coincidently or before V_{PP} and removed either coincidently or after V_{PP}.

2. V_{PP} must not be greater than 13.5 volts including overshoot.

3. During $\overline{CE} = \overline{PGM} = V_{IL}$, V_{PP} must not be switched from V_{CC} to 12.75 volts or vice-versa.

4. Removing or inserting the device while 12.75 volts is supplied may harm the reliability of the device.

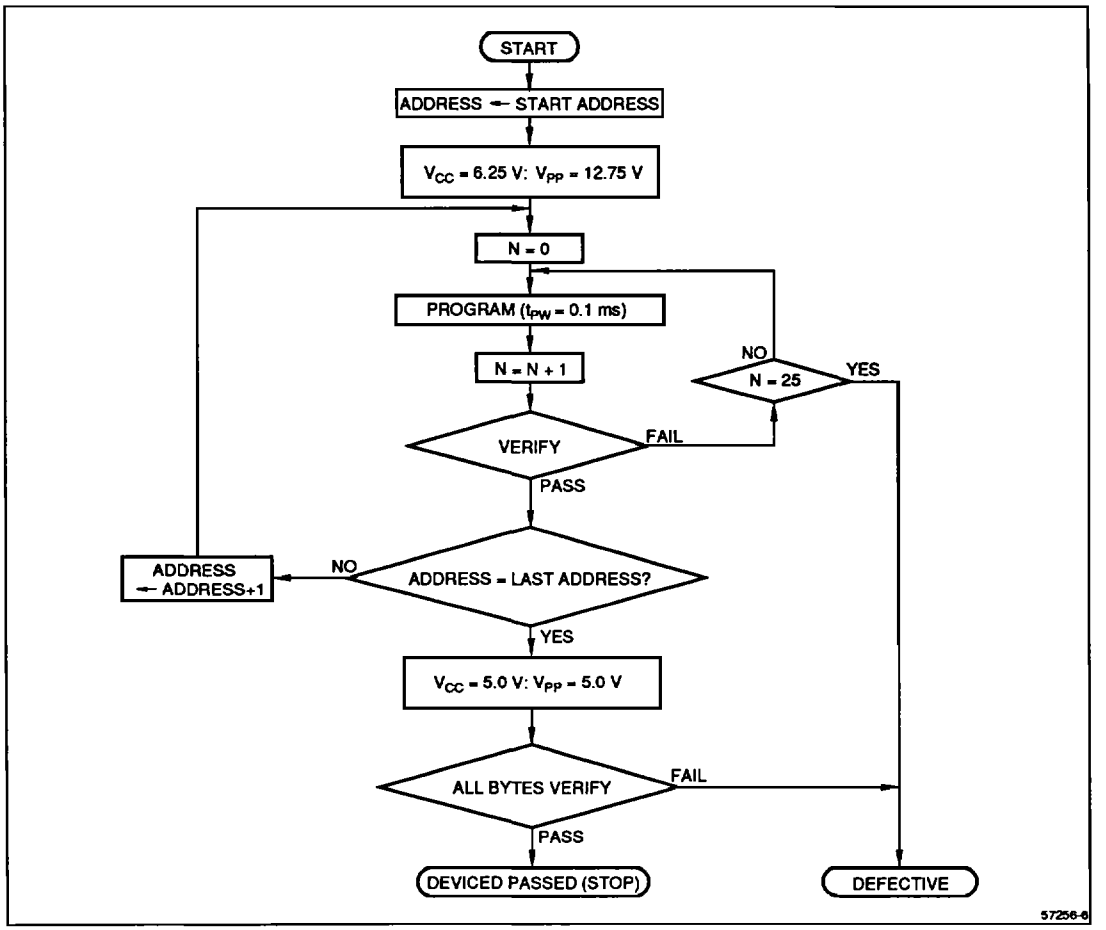

Figure 6. Programming Flowchart
(V_{CC} = 6.25 V, V_{PP} = 12.75 V, t_{PW} = 0.1 ms)

ORDERING INFORMATION