

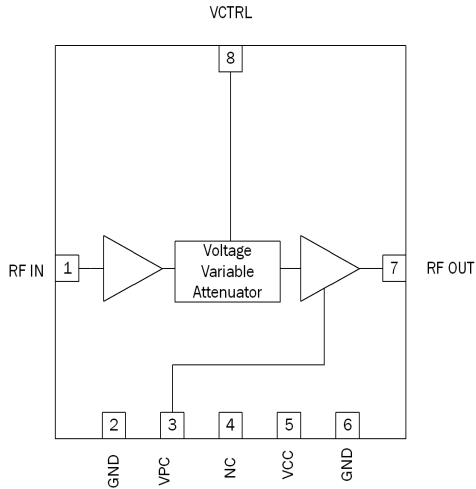


Features

- 1750 MHz to 2250 MHz Operation
- Gain = 24 dB Typical
- Gain Adjustment Range > 20 dB
- ACPR ≥ -66 dBc Typ. at +12 dBm P_{OUT} (Dual Carrier WCDMA)
- Small 7 mm x 7 mm, Multi-Chip Module

Applications

- Cellular, 3G Infrastructure
- WiBro, WiMax, LTE
- Microwave Radio
- High Linearity Power Control



Functional Block Diagram

Product Description

RFMD's RVA2007L is a fully integrated analog controlled variable gain amplifier featuring exceptional linearity over a greater than 20dB gain control range. This variable gain amplifier is controlled by a single 0V to 3.3V positive supply voltage. The RVA2007L is packaged in a small 7 mm x 7 mm leadless laminate MCM which contains thermal vias for ultra low thermal resistance. This module is internally matched to 50Ω and is easy to use with no external matching components required.

Optimum Technology Matching® Applied

- | | | | |
|---|--------------------------------------|--|-----------------------------------|
| <input type="checkbox"/> GaAs HBT | <input type="checkbox"/> SiGe BiCMOS | <input checked="" type="checkbox"/> GaAs pHEMT | <input type="checkbox"/> GaN HEMT |
| <input type="checkbox"/> GaAs MESFET | <input type="checkbox"/> Si BiCMOS | <input type="checkbox"/> Si CMOS | <input type="checkbox"/> RF MEMS |
| <input checked="" type="checkbox"/> InGaP HBT | <input type="checkbox"/> SiGe HBT | <input type="checkbox"/> Si BJT | <input type="checkbox"/> LDMOS |

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Absolute Maximum Ratings

Parameter	Rating	Unit
Max Device Current	770	mA
Max Device Voltage	5.5	V
Max Control Line Voltage	6	V
Max RF Input Power*	25	dBm
Max Junction Temp (T _J)	+150	°C
Max Storage Temp	+150	°C
Thermal Resistance (junction to backside of module)	14.8	°C/W
ESD	Class 1C (1000V min)	

*Load condition: Z_L = 50Ω



Caution! ESD sensitive device.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

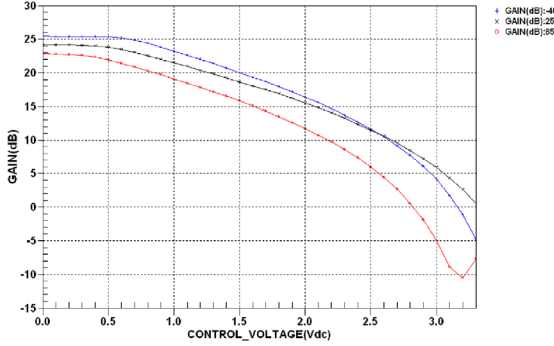
RoHS status based on EU Directive 2002/95/EC (at time of this document revision).

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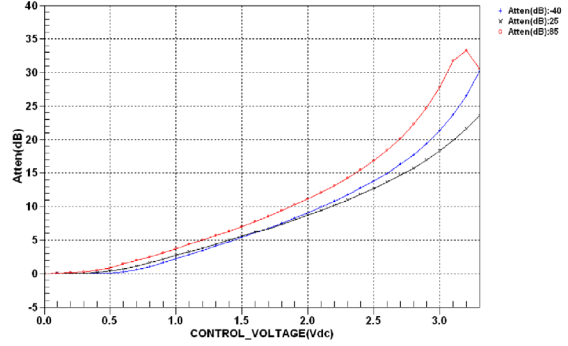
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
					All specifications for -40 °C to +85 °C, 4.75V to 5.25V, and process variations unless otherwise stated.
Frequency	2110		2170	MHz	
Temperature Range	-40	25	85	°C	Operating Range
Gain	23.5	24.5	25.5	dB	Min attenuator setting, 5V, 25C
Gain	22	24.5	26.5	dB	Over All Conditions
Nominal Operating Output Power		12		dBm	Operating power for ACPR rating
Output IP3	42	45	48	dBm	In high gain setting
P1dB	28	29.5		dBm	Max gain setting
ACPR	-60	-66	-68	dBc	Dual carrier WCDMA, 7.5 dB CF at nominal operating power; over full attenuation range
Gain Flatness		0.2	0.6	dB	Over 50MHz BW
Gain Adjustment Range	20	23.5	35	dB	
Control Voltage Range	0		3.3	V	
Noise Figure		3.8	5.0	dB	Min attenuator setting
Impedance		50		Ω	
Input Return Loss	15	20		dB	Over attenuation range
Output Return Loss	14	15		dB	Over attenuation range
Supply Voltage	4.75	5.0	5.25	V	
Supply Current (VPC=0V)	300	460	600	mA	Max current at -40 °C
Supply Current (VPC=0V)	120	126	140	mA	Output amplifier shutdown total current

Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
					All specifications for -40 °C to +85 °C, 4.75V to 5.25V, and process variations unless otherwise stated.
Frequency	1750		2250	MHz	
Temperature Range	-40	25	85	°C	Operating Range
Gain	21.5	24.5	25.5	dB	Min attenuator setting, 5V, 25C
Gain	20	24.5	26.5	dB	Over All Conditions
Nominal Operating Output Power		12		dBm	Operating power for ACPR rating
Output IP3	39	43	47	dBm	In high gain setting
P1dB	28	29.5		dBm	Max gain setting
ACPR	-60	-66	-68	dBc	Dual carrier WCDMA, 7.5dB CF at nominal operating power; over full attenuation range
Gain Flatness		0.2	0.9	dB	Over 50MHz BW
Gain Adjustment Range	20	23.5	35	dB	
Control Voltage Range	0		3.3	V	
Noise Figure		3.8	5.2	dB	Min attenuator setting
Impedance		50		Ω	
Input Return Loss	10	20		dB	Over attenuation range
Output Return Loss	9	15		dB	Over attenuation range

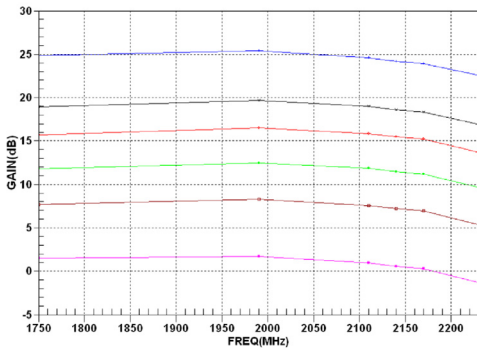
GAIN VS. CONTROL VOLTAGE VS. TEMPERATURE @ 2140 MHz



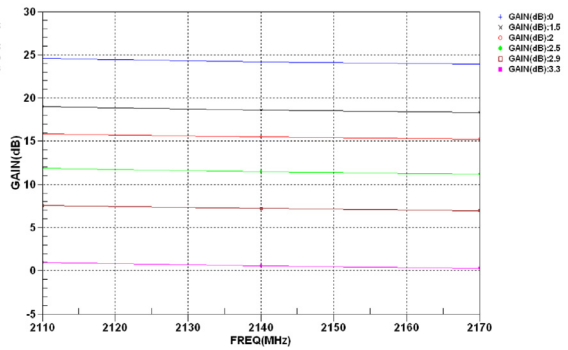
ATTENUATION VS. CONTROL VOLTAGE VS. TEMPERATURE @ 2140 MHz



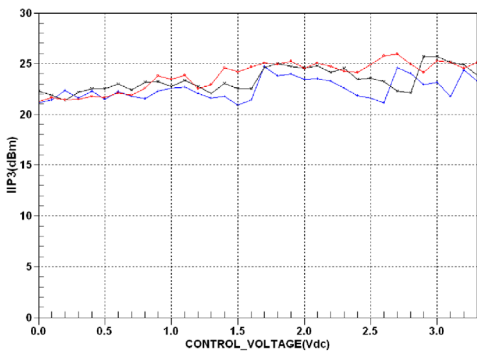
GAIN VS. FREQUENCY VS. CONTROL VOLTAGE



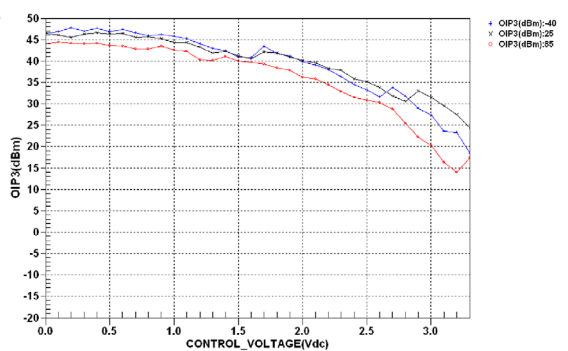
GAIN VS. FREQUENCY VS. CONTROL VOLTAGE



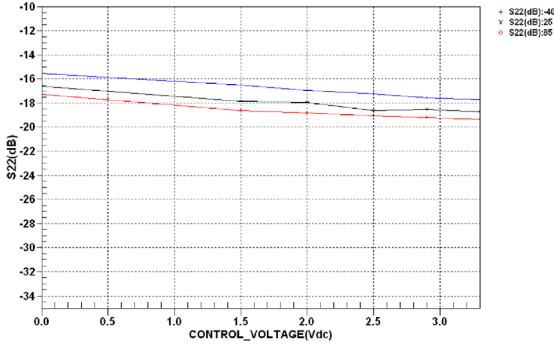
INPUT IP3 VS. CONTROL VOLTAGE VS. TEMPERATURE @ 2140 MHz



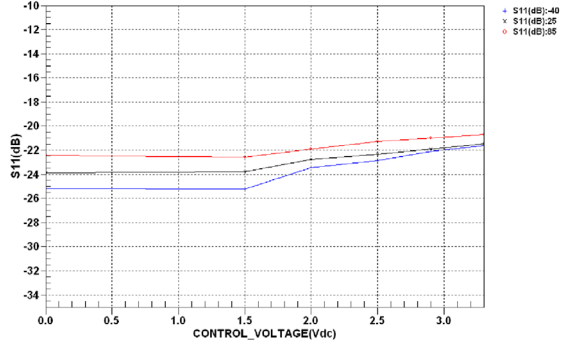
OUTPUT IP3 VS. CONTROL VOLTAGE VS. TEMPERATURE @ 2140 MHz



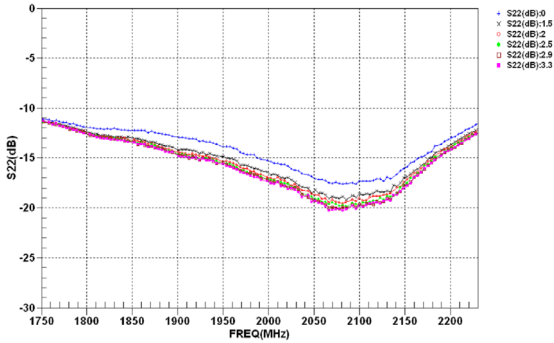
OUTPUT RETURN LOSS VS. CONTROL VOLTAGE VS. TEMPERATURE @ 2140 MHz



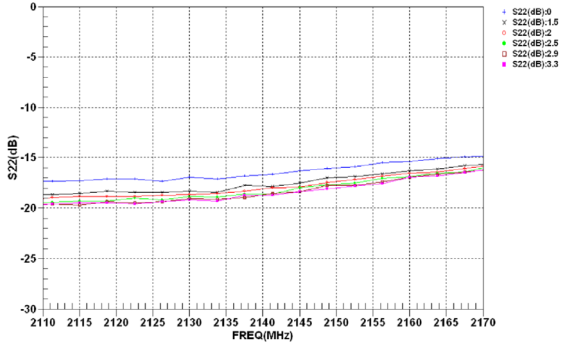
INPUT RETURN LOSS VS. CONTROL VOLTAGE VS. TEMPERATURE @ 2140 MHz



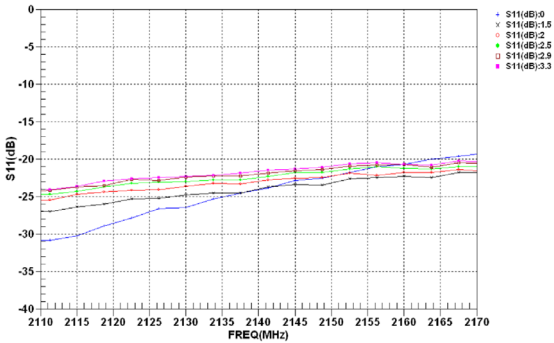
OUTPUT RETURN LOSS VS. FREQUENCY VS. CONTROL VOLTAGE



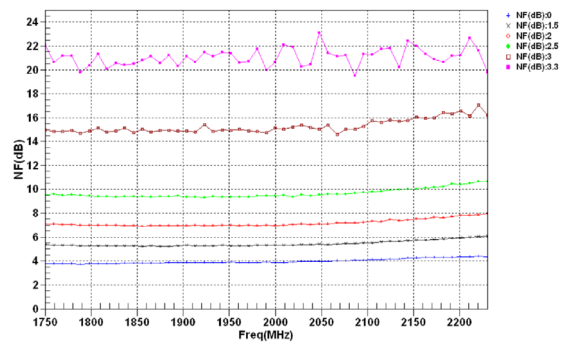
OUTPUT RETURN LOSS VS. FREQUENCY VS. CONTROL VOLTAGE



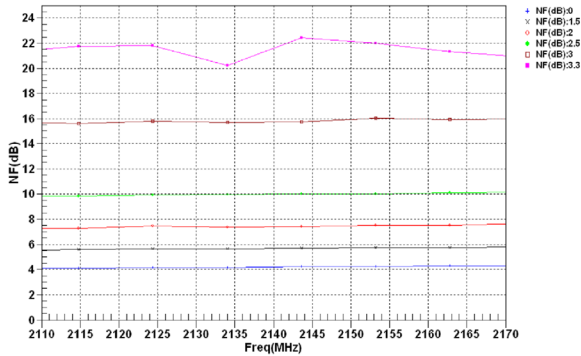
INPUT RETURN LOSS VS. FREQUENCY VS. CONTROL VOLTAGE



NOISE FIGURE VS. FREQUENCY VS. CONTROL VOLTAGE



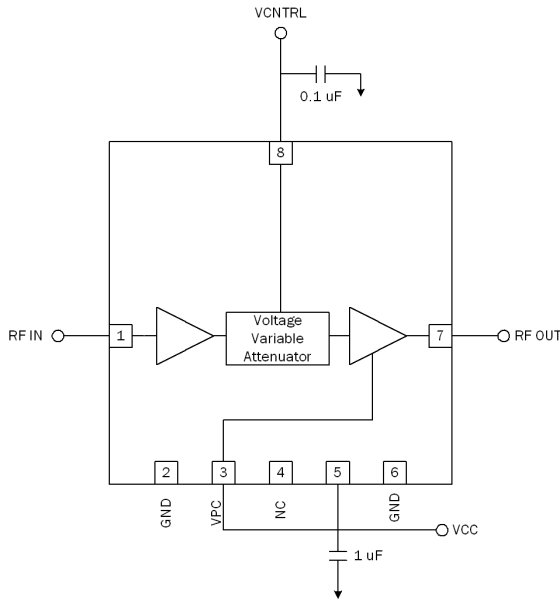
NOISE FIGURE VS. FREQUENCY VS. CONTROL VOLTAGE



Pin	Function	Description
1	RFIN	RF input pin. Internal DC-block.
2	GND	Ground pin.
3	VPC	Power up/down control for 2nd stage amplifier. Apply V_{CC} to power on 2nd stage amplifier. Apply 0V to disable 2nd stage amplifier. Do not exceed $V_{CC} + 0.5V$. Connect to V_{CC} if not needed. Decoupling capacitor may be desired on application board for control line noise.
4	NC	No connection.
5	VCC	Power supply for the module. Recommending $1\mu F$ decoupling cap on the application board.
6	GND	Ground pin.
7	RFOUT	RF output pin. Internal DC-block.
8	VCTRL	Gain control voltage; 0V to 3.3V range. Maximum gain at 0V. Recommending $0.1\mu F$ decoupling on the application board.
Center Pad	GND	Center ground pads need to have a good thermal path on the application board. Use solder stencil pattern shown in the document to define solder paste during assembly.

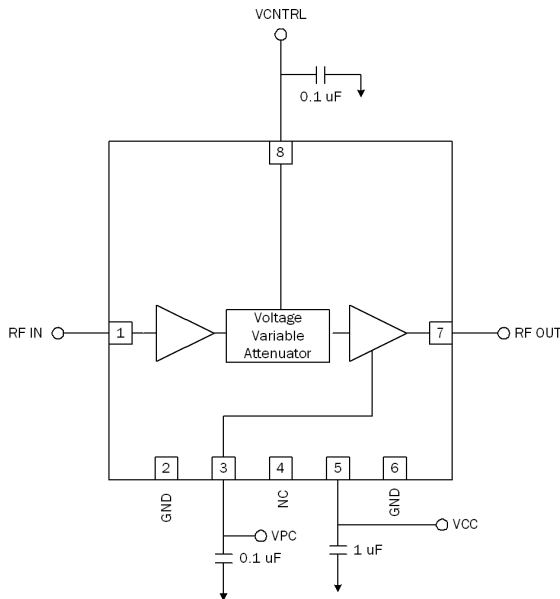
Application Schematic

(Without using final stage amplifier power down control)

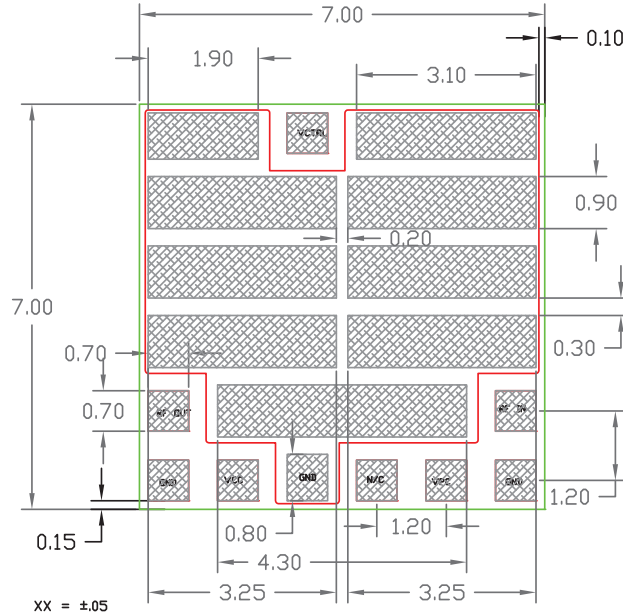


Application Schematic

(Using final stage amplifier power down control)



PCB Design Requirements



Note: This solder stencil pattern is required to prevent solder voiding that may impact thermal dissipation.

Ordering Information

Ordering Code	Description
RVA2007LSQ	Sample bag with 25 pieces
RVA2007LSR	7" Reel with 100 pieces
RVA2007LTR7	7" Reel with 1500 pieces
RVA2007LTR13	13" Reel with 2500 pieces
RVA2007LPCK-410	1750MHz to 2250MHz PCBA with 5-piece sample bag