



PMZ950UPE

20 V, P-channel Trench MOSFET

8 May 2014

Product data sheet

1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1006-3 (SOT883) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Trench MOSFET technology
- Leadless ultra small and ultra thin SMD plastic package: $1.0 \times 0.6 \times 0.48$ mm
- ElectroStatic Discharge (ESD) protection > 1 kV HBM
- Drain-source on-state resistance $R_{DS(on)} = 1.02 \Omega$

3. Applications

- Relay driver
- High-speed line driver
- High-side load switch
- Switching circuits

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25^\circ\text{C}$		-	-	-20	V
V_{GS}	gate-source voltage			-8	-	8	V
I_D	drain current	$V_{GS} = -4.5$ V; $T_{amb} = 25^\circ\text{C}$	[1]	-	-	-500	mA
Static characteristics							
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = -4.5$ V; $I_D = -500$ mA; $T_j = 25^\circ\text{C}$		-	1.02	1.4	Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm^2 .

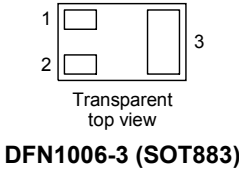
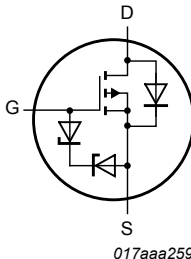


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5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 Transparent top view DFN1006-3 (SOT883)	 017aaa259
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMZ950UPE	DFN1006-3	DFN1006-3: leadless ultra small plastic package; 3 solder lands	SOT883

7. Marking

Table 4. Marking codes

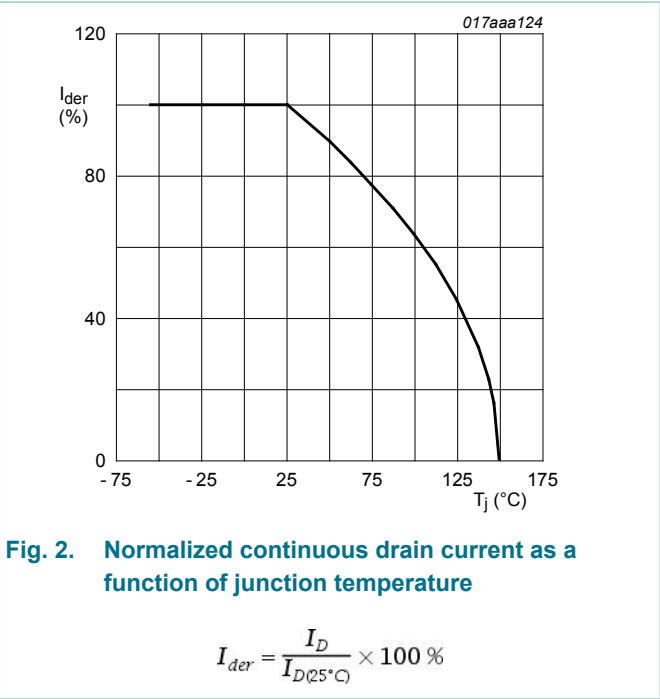
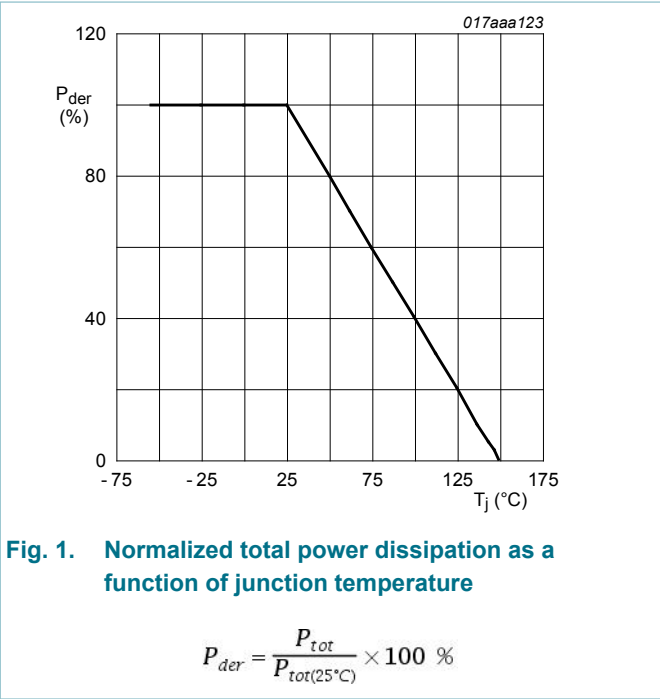
Type number	Marking code
PMZ950UPE	ZT

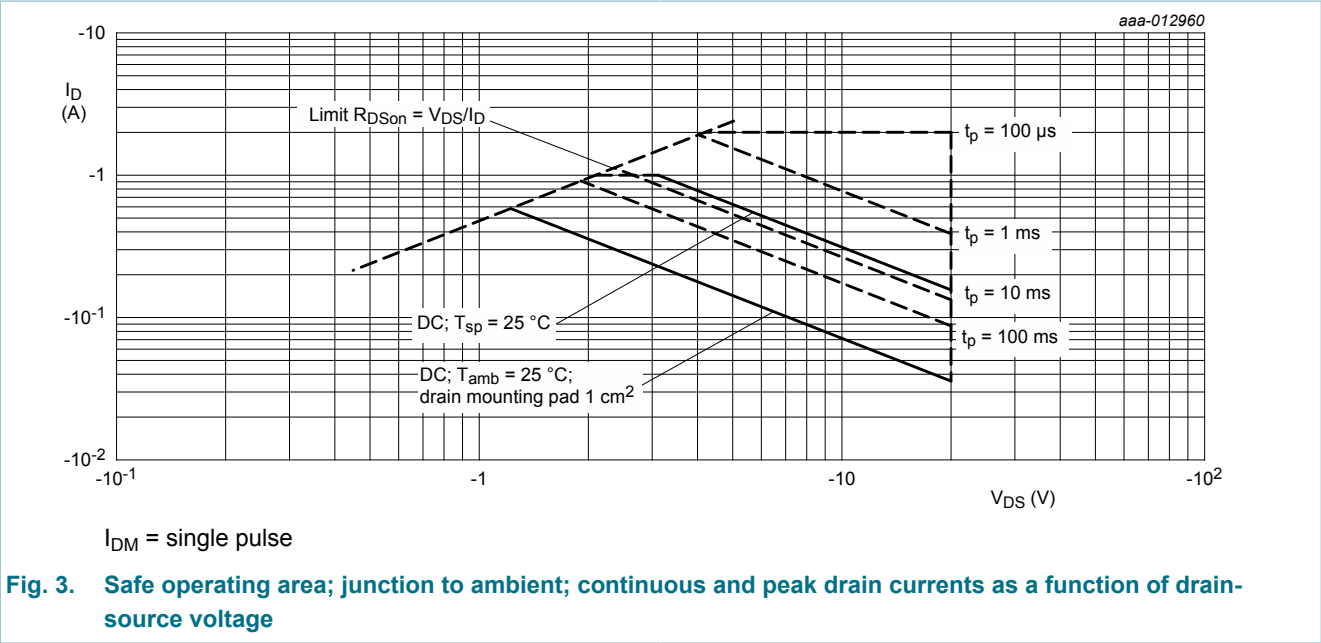
8. Limiting values

Table 5. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	-20	V
V _{GS}	gate-source voltage			-8	8	V
I _D	drain current	V _{GS} = -4.5 V; T _{amb} = 25 °C	[1]	-	-500	mA
		V _{GS} = -4.5 V; T _{amb} = 100 °C	[1]	-	-300	mA
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	-2	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	360	mW
			[1]	-	715	mW
		T _{sp} = 25 °C		-	2700	mW
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	-350	mA

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 1 cm².
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



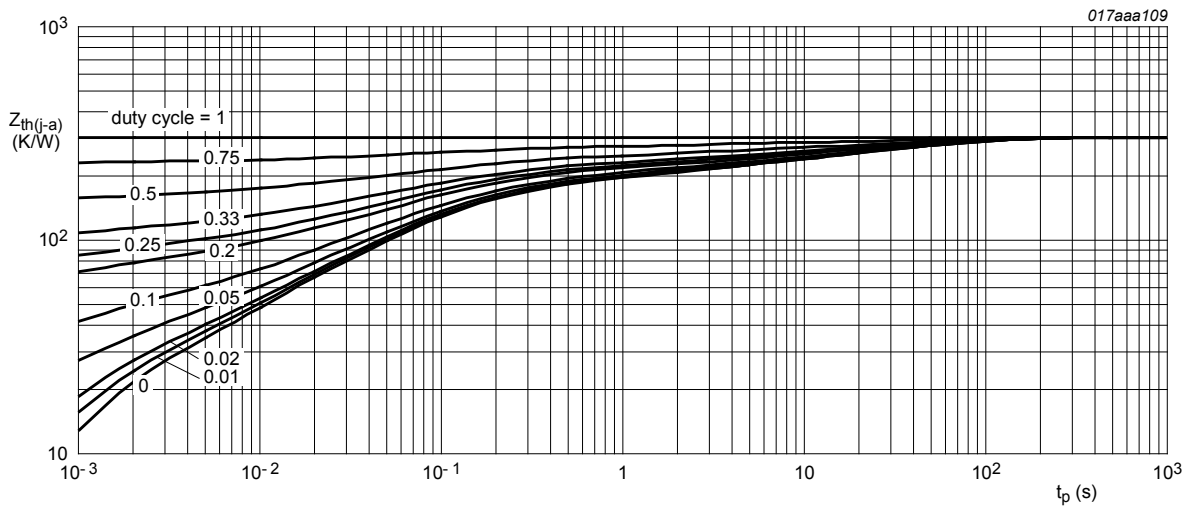


9. Thermal characteristics

Table 6. Thermal characteristics

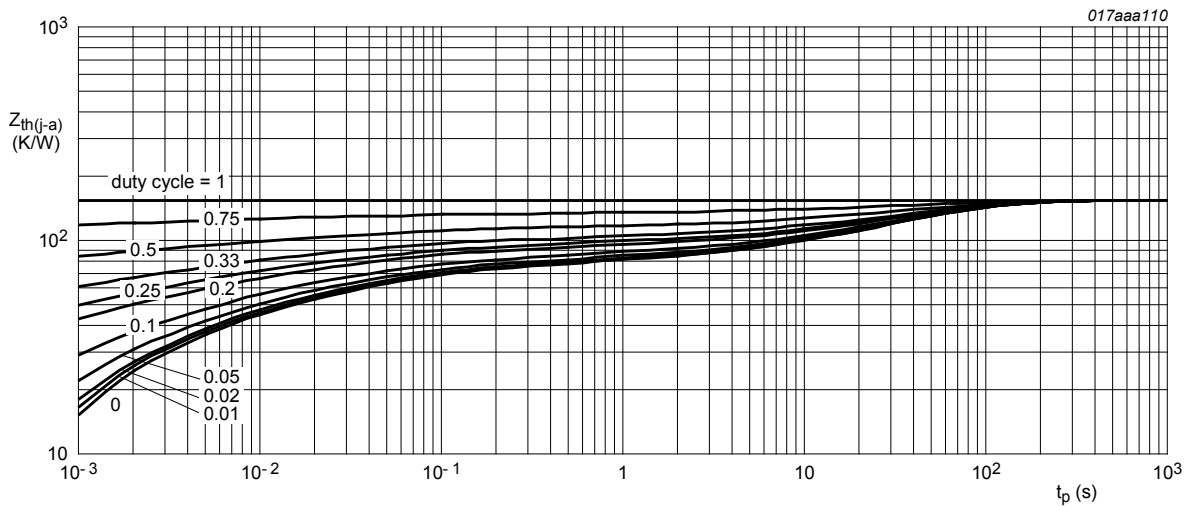
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	305	360	K/W
			[2]	-	150	175	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	-	40	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 1 cm^2 .



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 1 cm²

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 25 ^\circ C$	-0.45	-0.7	-0.95	V
I_{DSS}	drain leakage current	$V_{DS} = -20 V$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	-	-	-1	μA
		$V_{DS} = -20 V$; $V_{GS} = 0 V$; $T_j = 150 ^\circ C$	-	-	-10	μA
I_{GSS}	gate leakage current	$V_{GS} = 8 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	-	10	μA
		$V_{GS} = -8 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	-	-10	μA
		$V_{GS} = -4.5 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	-	-1	μA
		$V_{GS} = 4.5 V$; $V_{DS} = 0 V$; $T_j = 25 ^\circ C$	-	-	1	μA
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5 V$; $I_D = -500 mA$; $T_j = 25 ^\circ C$	-	1.02	1.4	Ω
		$V_{GS} = -4.5 V$; $I_D = -500 mA$; $T_j = 150 ^\circ C$	-	1.54	2.1	Ω
		$V_{GS} = -2.5 V$; $I_D = -200 mA$; $T_j = 25 ^\circ C$	-	1.27	2.2	Ω
		$V_{GS} = -1.8 V$; $I_D = -40 mA$; $T_j = 25 ^\circ C$	-	1.7	3.3	Ω
		$V_{GS} = -1.5 V$; $I_D = -10 mA$; $T_j = 25 ^\circ C$	-	2.3	5	Ω
		$V_{GS} = -1.2 V$; $I_D = -1 mA$; $T_j = 25 ^\circ C$	-	3.5	-	Ω
g_{fs}	forward transconductance	$V_{DS} = -10 V$; $I_D = -500 mA$; $T_j = 25 ^\circ C$	-	480	-	mS
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -10 V$; $I_D = -450 mA$; $V_{GS} = -4.5 V$; $T_j = 25 ^\circ C$	-	1.19	2.1	nC
Q_{GS}	gate-source charge		-	0.17	-	nC
Q_{GD}	gate-drain charge		-	0.1	-	nC
C_{iss}	input capacitance	$V_{DS} = -10 V$; $f = 1 MHz$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	-	43	-	pF
C_{oss}	output capacitance		-	14	-	pF
C_{rss}	reverse transfer capacitance		-	8	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -10 V$; $I_D = -0.45 A$; $R_L = 22 \Omega$; $V_{GS} = -4.5 V$; $R_{G(ext)} = 6 \Omega$; $T_j = 25 ^\circ C$	-	2.3	-	ns
t_r	rise time		-	5	-	ns
$t_{d(off)}$	turn-off delay time		-	13.5	-	ns
t_f	fall time		-	6	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = -115 mA$; $V_{GS} = 0 V$; $T_j = 25 ^\circ C$	-	-0.7	-1.2	V

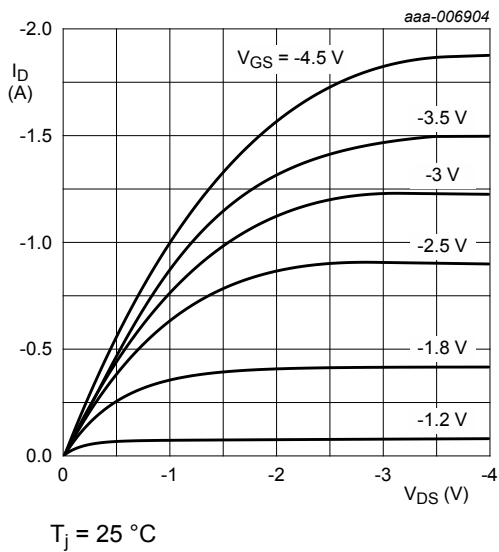


Fig. 6. TR2: output characteristics; drain current as a function of drain-source voltage; typical values

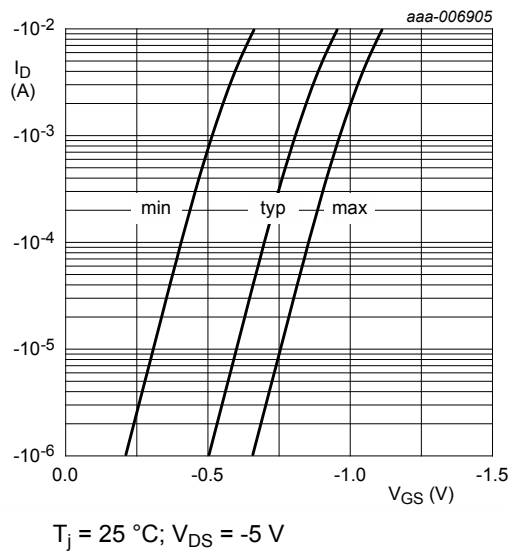


Fig. 7. TR2: sub-threshold drain current as a function of gate-source voltage

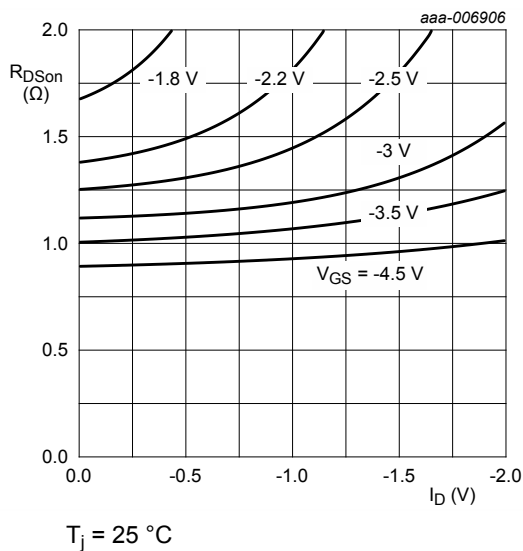


Fig. 8. TR2: drain-source on-state resistance as a function of drain current; typical values

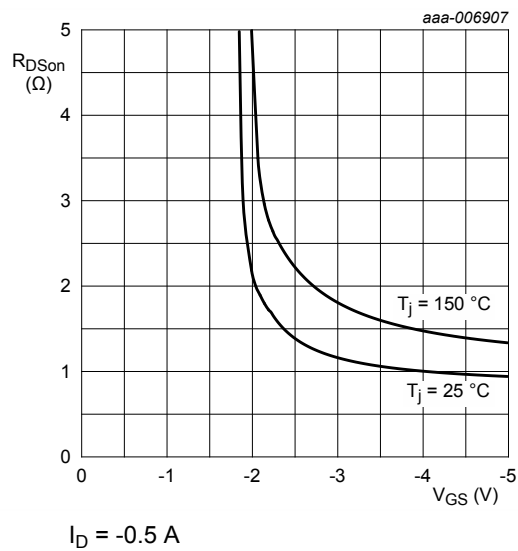


Fig. 9. TR2: drain-source on-state resistance as a function of gate-source voltage; typical values

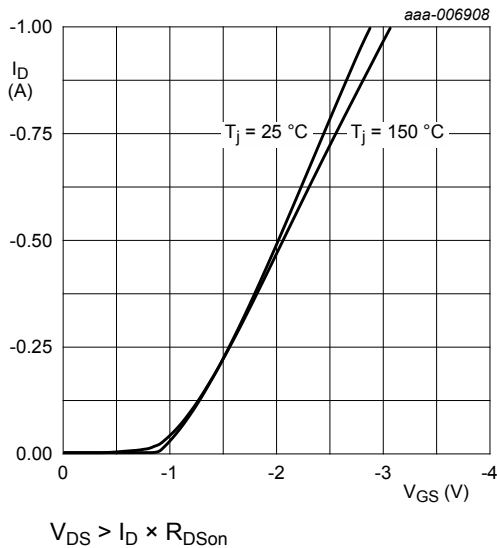


Fig. 10. TR2: transfer characteristics; drain current as a function of gate-source voltage; typical values

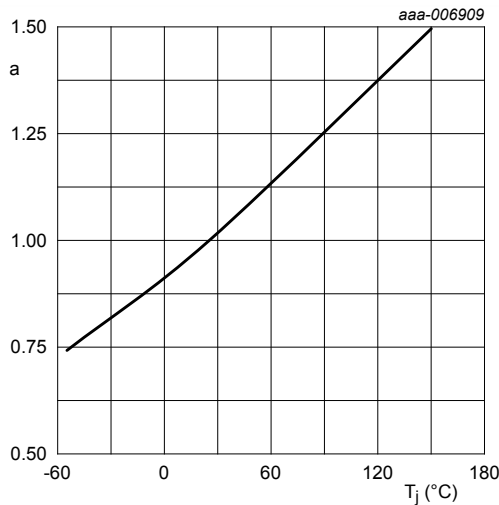


Fig. 11. TR2: normalized drain-source on-state resistance as a function of junction temperature; typical values

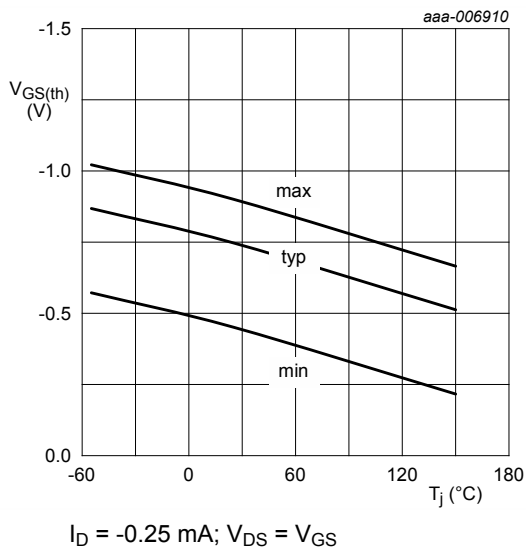


Fig. 12. TR2: gate-source threshold voltage as a function of junction temperature

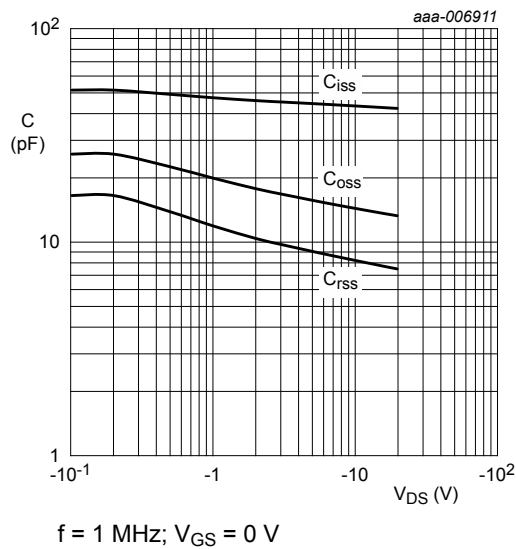


Fig. 13. TR2: input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

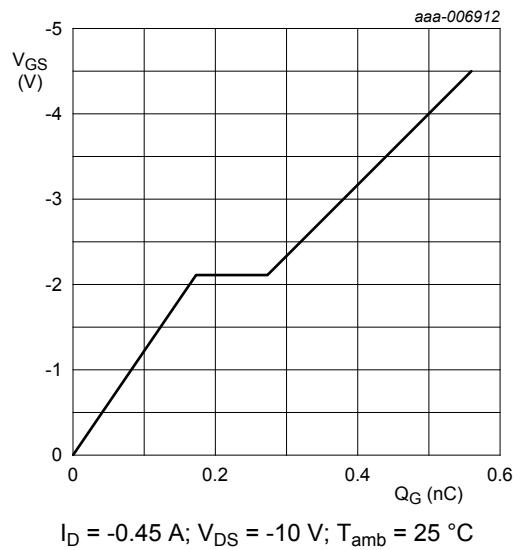


Fig. 14. TR2: gate-source voltage as a function of gate charge; typical values

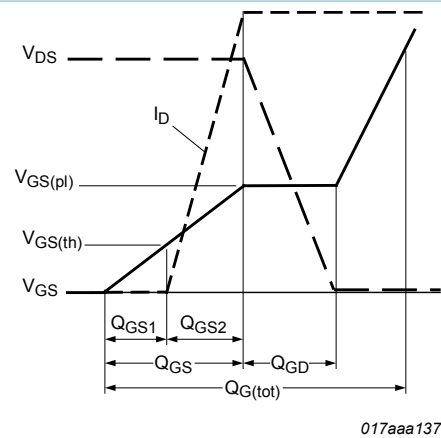
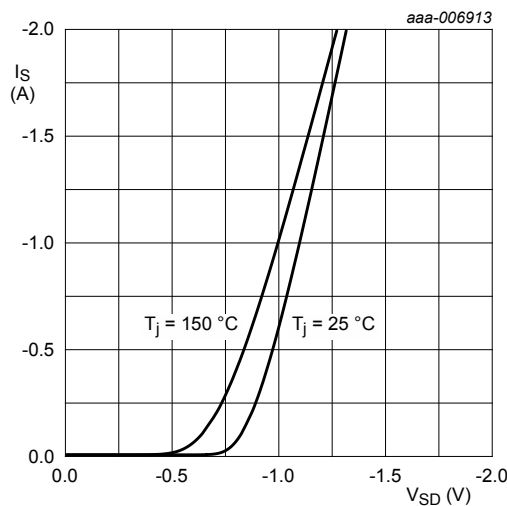


Fig. 15. MOSFET transistor: Gate charge waveform definitions



$V_{GS} = 0$ V

Fig. 16. TR2: source current as a function of source-drain voltage; typical values

11. Test information

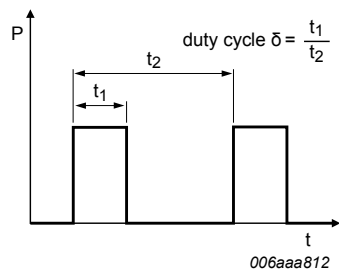


Fig. 17. Duty cycle definition

12. Package outline

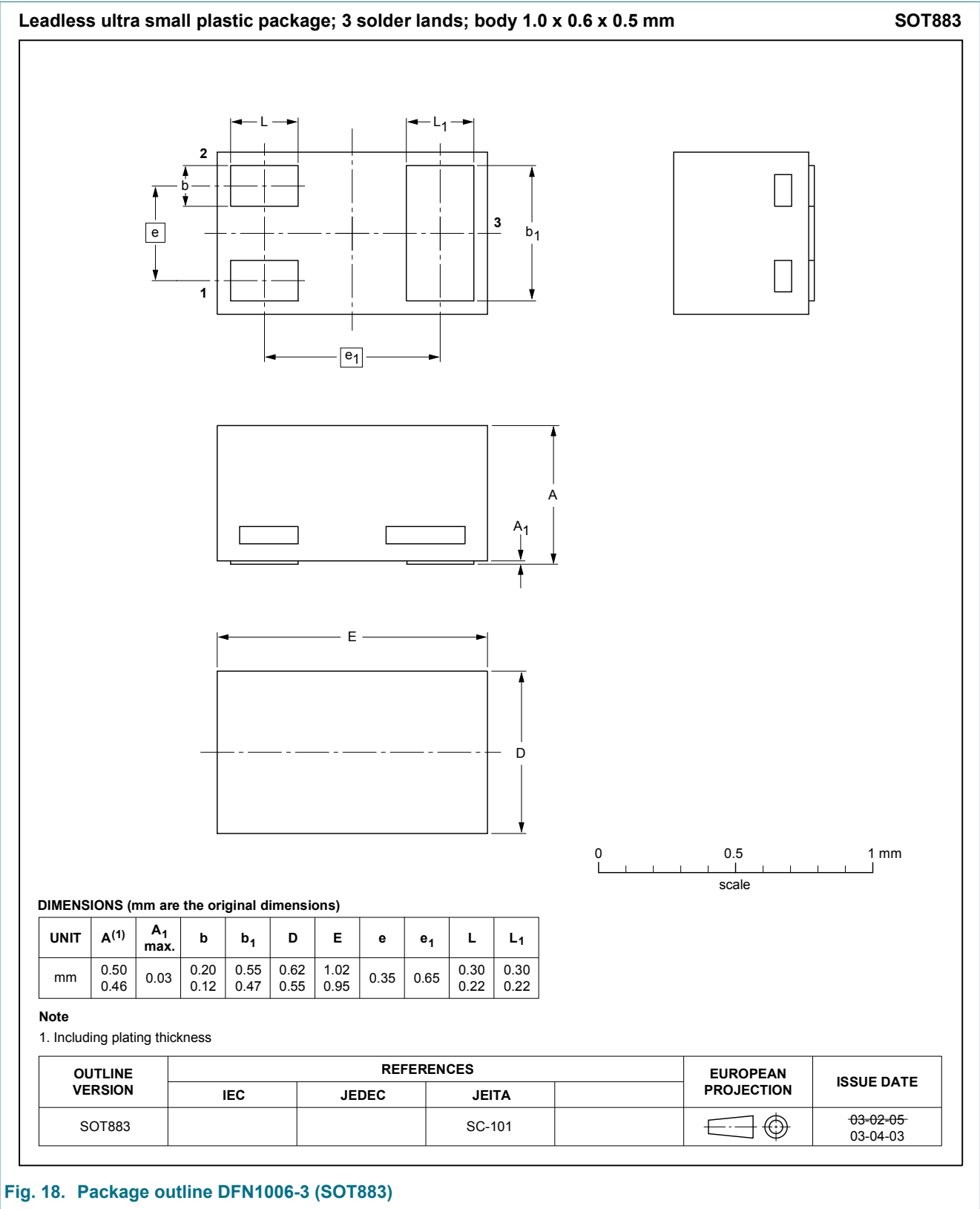


Fig. 18. Package outline DFN1006-3 (SOT883)

13. Soldering

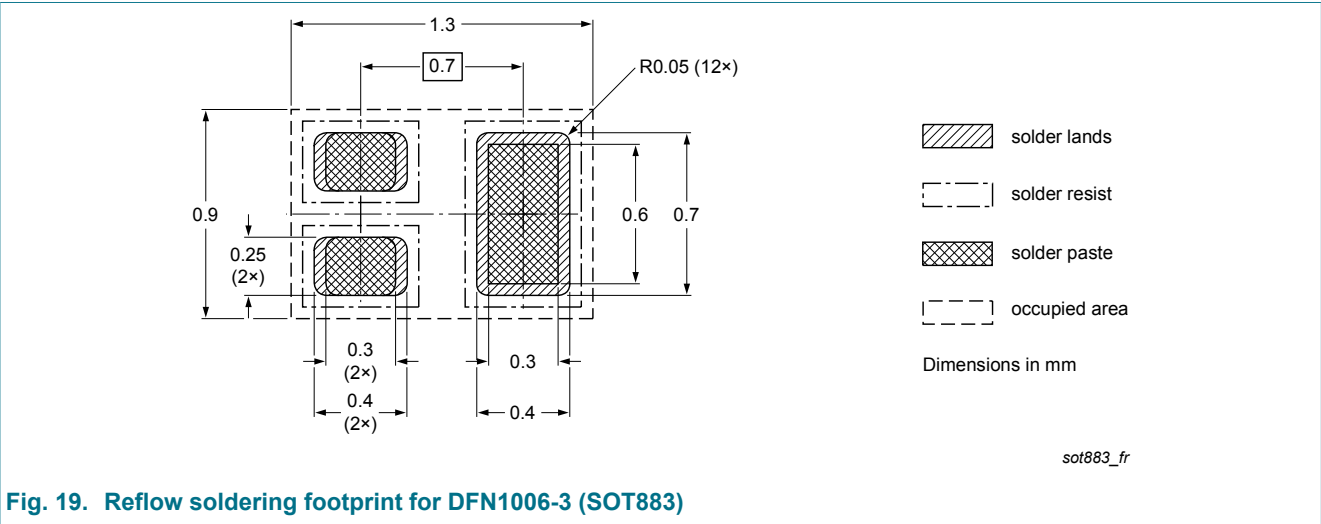


Fig. 19. Reflow soldering footprint for DFN1006-3 (SOT883)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMZ950UPE v.1	20140508	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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