HEWLETT PACKARD

MGA-61000
2-18 GHz Cascadable GaAs MMIC Amplifier

Features

- **Cascadable 50 Ω Gain Block**
- **Broadband Performance: 2-18 GHz**
  7.0 dB typical Gain
  ± 0.5 dB typical Gain Flatness
- **14.0 dBm typical $P_{1\,dB}$ at 18 GHz**
- **Single Supply Bias**

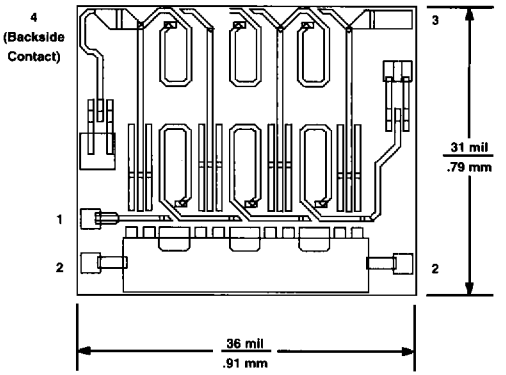
Description

The MGA-61000 is a high performance gallium arsenide Monolithic Microwave Integrated Circuit (MMIC) chip designed for use as a broadband high frequency gain stage in industrial and military applications.

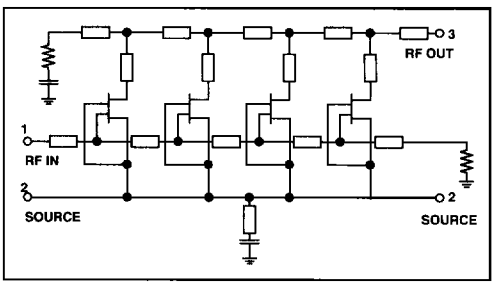
This MMIC is a distributed amplifier utilizing dual gate FETs, resulting in a fully matched gain block useful in the 2 to 18 GHz frequency range. An external self-bias source resistor allows for bias flexibility from a single positive power supply.

The die is fabricated using HP's nominal 0.3 micron recessed Schottky-barrier-gate, gold metallization, and silicon nitride passivation to achieve excellent performance, uniformity, and reliability.

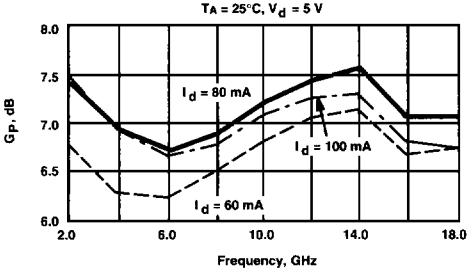
Chip Outline



Chip Schematic



TYPICAL POWER GAIN vs. FREQUENCY AND CURRENT
T_A = 25°C, V_d = 5 V



Electrical Specifications, T_A = 25°C

Symbol	Parameters and Test Conditions: V_d = 5 V; Z_O = 50 Ω		Units	Min.[1]	Typ.	Max.[1]
GP	Power Gain ($\|S_{21}\|^2$)	f = 2 to 18 GHz	dB	6.0	7.0	
ΔGP	Gain Flatness	f = 2 to 18 GHz	dB		±0.5	±0.75
VSWR	Input VSWR	f = 2 to 18 GHz				2.0:1
	Output VSWR	f = 2 to 18 GHz				2.0:1
–	Reverse Isolation ($\|S_{21}\|^2$)	f = 2 to 18 GHz	dB		30	
NF	50 Ω Noise Figure	f = 2 to 18 GHz	dB		6.0	
$P_{1\,dB}$	Output Power @ 1 dB Gain Compression V_d = 6 V	f = 2 to 18 GHz	dBm		14	
IP_3	Third Order Intercept Point	V_d = 6 V, f = 18 GHz	dBm		20	
I_d	Device Current		mA	60	80	100

Note: 1. RF performance is determined by assembling and testing 10 devices per wafer.

Absolute Maximum Ratings

Parameter	Absolute Maximum[1]
Device Voltage	7.0 V
Total Power Dissipation[2]	600 mW
CW RF Input Power	+20 dBm
Channel Temperature	175°C
Storage Temperature	–65°C to +175°C

Thermal Resistance: θ_{jc} = 60°C/W; T_{CH} = 150°C
Liquid Crystal Measurement; 1 μm spot size[3]

Notes:

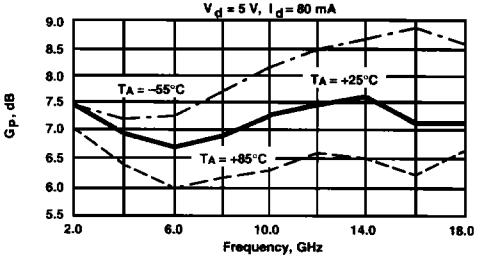
1. Operation of this device above any one of these parameters may cause permanent damage.
2. Derate linearly at 16.7 mW/°C for T_A > 139°C.
3. The small spot size of this technique results in a higher, though more accurate determination of θ_{jc} than do alternate methods. See MEASUREMENTS section for more information.

Part Number Ordering Information

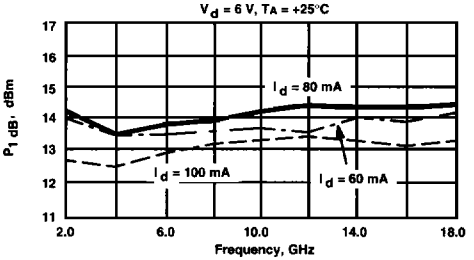
Part Number	Devices Per Tray
MGA-61000-GP0	1
MGA-61000-GP2	10
MGA-61000-GP6	Up to 300

Typical Performance

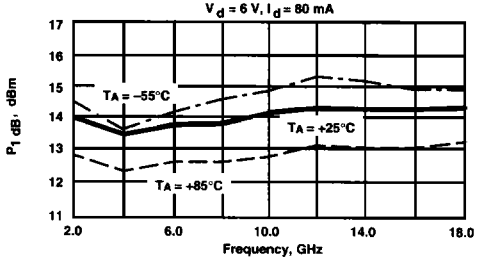
POWER GAIN vs. FREQUENCY AND TEMPERATURE
V_d = 5 V, I_d = 80 mA



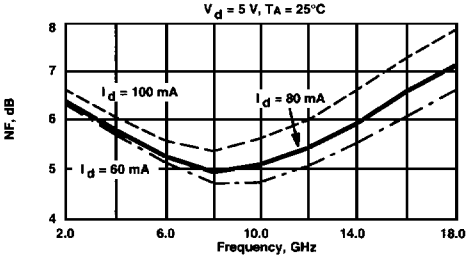
POWER OUTPUT @ 1 dB GAIN COMPRESSION vs. FREQUENCY AND CURRENT
V_d = 6 V, TA = +25°C



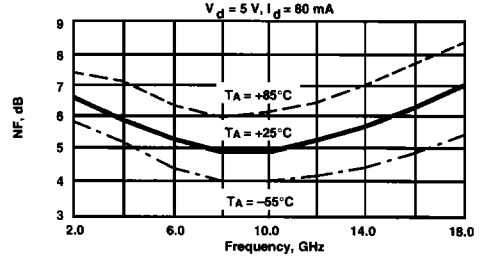
POWER OUTPUT @ 1 dB GAIN COMPRESSION vs. FREQUENCY AND TEMPERATURE
V_d = 6 V, I_d = 80 mA



NOISE FIGURE vs. FREQUENCY AND CURRENT
V_d = 5 V, TA = 25°C



NOISE FIGURE vs. FREQUENCY AND TEMPERATURE
V_d = 5 V, I_d = 80 mA

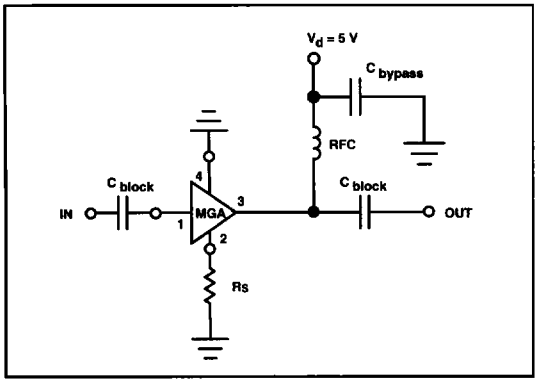


Typical Scattering Parameters: Z_O = 50 Ω

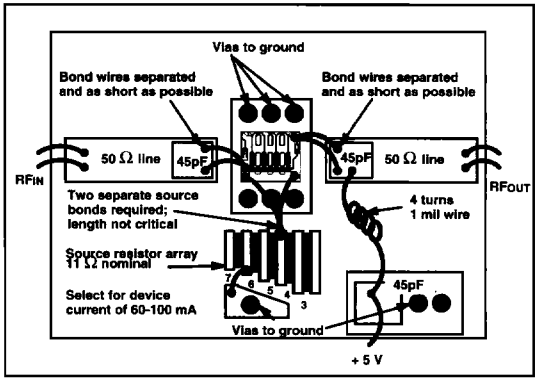
T_A = 25°C, V_d = 5 V, I_d = 80 mA

Freq. GHz	S_{11}		S_{21}			S_{12}			S_{22}	
	Mag	Ang	dB	Mag	Ang	dB	Mag	Ang	Mag	Ang
2.0	.15	143	7.4	2.36	145	–37.9	.013	59	.25	–130
3.0	.14	138	7.2	2.28	124	–35.4	.017	56	.17	–163
4.0	.15	134	6.9	2.22	105	–34.0	.020	47	.14	165
5.0	.16	126	6.8	2.19	86	–33.3	.022	39	.13	137
6.0	.16	118	6.8	2.18	68	–33.4	.021	31	.12	113
7.0	.16	111	6.8	2.20	50	–34.0	.020	24	.11	88
8.0	.16	106	6.9	2.22	32	–35.0	.018	20	.10	64
9.0	.15	103	7.0	2.25	13	–36.5	.015	15	.10	39
10.0	.15	105	7.2	2.30	–6	–38.4	.012	16	.10	17
11.0	.17	106	7.4	2.34	–27	–38.8	.011	21	.09	3
12.0	.19	104	7.4	2.36	–48	–38.0	.013	19	.07	–3
13.0	.22	98	7.4	2.35	–68	–36.5	.015	10	.06	19
14.0	.24	90	7.6	2.39	–88	–34.1	.020	–10	.08	46
15.0	.26	77	7.4	2.36	–111	–31.0	.028	–35	.15	51
16.0	.24	62	7.0	2.26	–133	–28.5	.037	–67	.21	41
17.0	.19	52	6.8	2.20	–154	–26.9	.045	–94	.24	31
18.0	.09	64	7.0	2.26	–173	–28.2	.039	–122	.24	39

Typical Biasing Configuration



Substrate Bonding Diagram



EXTERNAL ELEMENTS REQUIRED:

- Source Resistor Array (R_S): Select resistor for device current of 60-100 mA (11 Ω nominal).
- Input and Output DC Blocking Capacitors: 45 pF typical.
- RF Choke Network and Bypass Capacitor: 4 turns 1 mil wire; 45 pF capacitor typical.
- Input and Output RF Transmission Lines: 50 Ω typical.

RECOMMENDED DIE ATTACH PROCEDURE

1. Die attach should be performed under an inert atmosphere of either nitrogen or forming gas.
2. Set heater block temperature to 300 ± 10°C.
3. Place circuit on heater block and heat thoroughly; typically 5 - 15 seconds.
4. Place Au-Sn preform on circuit in die attach location, using sufficient quantity to ensure wetting and to produce a fillet around the die.
5. Using sharp tweezers, pickup the die and orient it properly on the circuit.
6. Scrub the die into the preform with a back-and-forth motion taking care not to scratch the top surface of the chip. Continue until wetting occurs; normally within 3 to 4 scrubs.
7. Wetting should occur on 100% of the chip perimeter to form a visible fillet around the die.
8. Remove the circuit from the heater block and allow it to cool in air. Total time for die attach should be less than 10 seconds.

RECOMMENDED WEDGE BONDING PROCEDURE

1. Set heater block temperature to 260 ± 10°C (If the wedge is heated, the heater block temperature should be lowered slightly from this setting. The exact setting will need to be determined empirically, and will vary from machine to machine).
2. Use prestressed (annealed) gold wire of .0007 or .001 inches diameter.
3. Tip bonding pressure should be between 15 and 20 grams, and should not exceed 20 grams. The footprint left by the wire should be between 1.5 and 2.5 wire diameters across.
4. Proceed with bonding according to machine instructions. Bonds should be made from the circuit to the chip bonding pads to minimize the potential for pad damage. Bonds should be made to the source (common) and drain (output) pads of the MMIC before bonding to the gate (input) pad to minimize the potential for ESD damage.

CAUTION: This device makes use of GaAs FET devices with very small gate geometries. Such devices are subject to damage by electro-static discharge (ESD), and must only be handled by properly grounded personnel working at grounded assembly stations.