

## Successive Approximation A/D Converter

8-Bit, 2.5Msps

The TRW TDC1001 analog-to-digital converter is a high-speed, 8-bit successive approximation device. This bipolar, monolithic converter offers significant advantages in size, cost, and performance, as well as high reliability and low-power consumption.

All digital interfaces are TTL compatible. A single +5VDC supply is required by the digital circuitry while -5VDC is required by the analog portion of the device. The analog and digital ground planes are internally isolated.

The TDC1001 consists of a comparator, reference buffer, 8-bit D/A converter, successive approximation register, output register, and control circuitry.

### Features

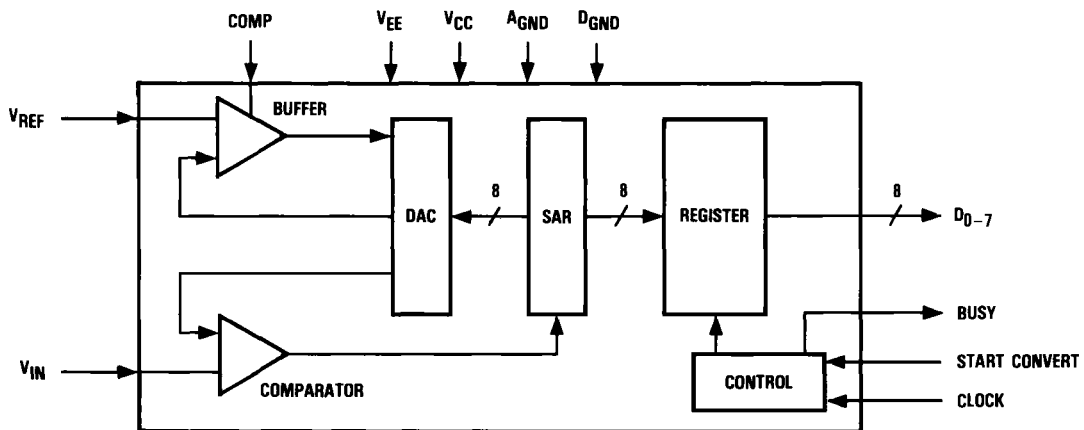
- 8-Bit Resolution
- Binary Output Coding
- TTL Compatible
- $\pm 1/2$  LSB Linearity
- Parallel Output Register
- 600mW Power Dissipation
- Available In An 18 Pin CERDIP Package

### Applications

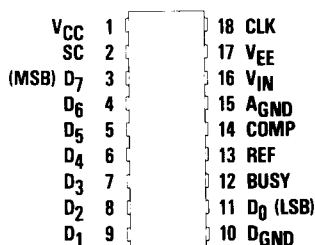
- Microprocessor Systems
- Numerical Control Interface
- Data Acquisition Systems



### Functional Block Diagram



## Pin Assignments



18 Pin CERDIP – B8 Package

## Analog Input

The analog input range of the device is set by the reference voltage. This is nominally  $-0.5\text{VDC}$  with an absolute tolerance of  $\pm 0.1\text{VDC}$ . Since the device is a successive approximation type A/D converter, a sample-and-hold circuit may be required in some applications.

## Conversion Timing Description

The timing sequence of the TDC1001 is typical of successive approximation converters. Nine clock cycles are required for each conversion. Start Convert must transition from LOW to HIGH a minimum of  $t_S$  prior to the leading edge of the first convert pulse, and must remain HIGH a minimum of  $t_H$  after the edge.

This first cycle clears the BUSY flag and prepares the device for a new conversion. The following eight clock cycles convert each data bit (MSB first, LSB last). During these eight clock cycles, the analog input must be held stable (to within  $1/2$  LSB). At  $t_D$  nanoseconds after the rising edge of the eighth clock pulse, the seven most significant bits are valid (and the BUSY signal goes LOW). At  $t_D$  nanoseconds after the ninth clock pulse the LSB is valid, and the conversion is completed.

## Data Outputs

The outputs of the TDC1001 are TTL compatible and capable of driving four low-power Schottky TTL (54/74 LS) unit loads or the equivalent. The outputs hold the previous data a minimum time ( $t_D$ ) after the rising edge of Start Convert (SC).

## Compensation Pin

The COMPensation pin (COMP), is provided for external compensation of the internal reference amplifier.

The compensation capacitor must be connected between this pin and  $V_{EE}$ . A tantalum capacitor greater than  $10\mu\text{F}$  is recommended for proper operation.

## Output Coding

An analog input voltage of  $0.0\text{V}$  will produce a digital output code of all zeros; an analog input voltage of  $-0.50\text{V}$  will produce a digital output code of all ones.

## Functional Description

### General Information

The TDC1001 consists of six functional sections: comparator for the analog input, reference buffer, 8-bit D/A converter (DAC), successive approximation register (SAR), output register, and control circuitry. The SAR and comparator will sequentially compare the analog input to the DAC output. The conversion process requires nine clock cycles.

### Power

The TDC1001 operates from separate analog and digital power supplies. Analog power ( $V_{EE}$ ) is  $-5.0\text{VDC}$  and digital power ( $V_{CC}$ ) is  $+5.0\text{VDC}$ . All power and ground pins must be connected.

Separate decoupling for each supply is recommended. The return for  $I_{EE}$ , the current drawn from the  $V_{EE}$  supply, is AGND. The return for  $I_{CC}$ , the current drawn from the  $V_{CC}$  supply, is DGND.

### Reference

The TDC1001 accepts a nominal input reference voltage of  $-0.5\text{VDC}$ . The voltage should be supplied by a precision voltage reference, as the accuracy of this voltage will have a significant effect on the overall accuracy of the system. The reference voltage input pin should be bypassed to AGND as close as possible to the device terminal.

## Package Interconnections

Signal Type	Signal Name	Function	Value	B8 Package Pins
Power	V <sub>EE</sub>	Analog Supply Voltage	-5.0VDC	17
	V <sub>CC</sub>	Digital Supply Voltage	+5.0VDC	1
	A <sub>GND</sub>	Analog Ground	0.0VDC	15
	D <sub>GND</sub>	Digital Ground	0.0VDC	10
Reference	V <sub>REF</sub>	Reference Voltage Input	-0.5VDC	13
Analog Input	V <sub>IN</sub>	Analog Input	0 to -0.5V	16
Conversion Timing Description	SC	Start Convert Input	TTL	2
	BUSY	Busy Flag Output	TTL	12
	CLK	Convert Clock Input	TTL	18
Outputs	D <sub>7</sub>	MSB Output	TTL	3
	D <sub>6</sub>		TTL	4
	D <sub>5</sub>		TTL	5
	D <sub>4</sub>		TTL	6
	D <sub>3</sub>		TTL	7
	D <sub>2</sub>		TTL	8
	D <sub>1</sub>		TTL	9
	D <sub>0</sub>	LSB Output	TTL	11
Compensation	COMP	Compensation Pin	>10μF	14

**A**

**Figure 1. Timing Diagram**

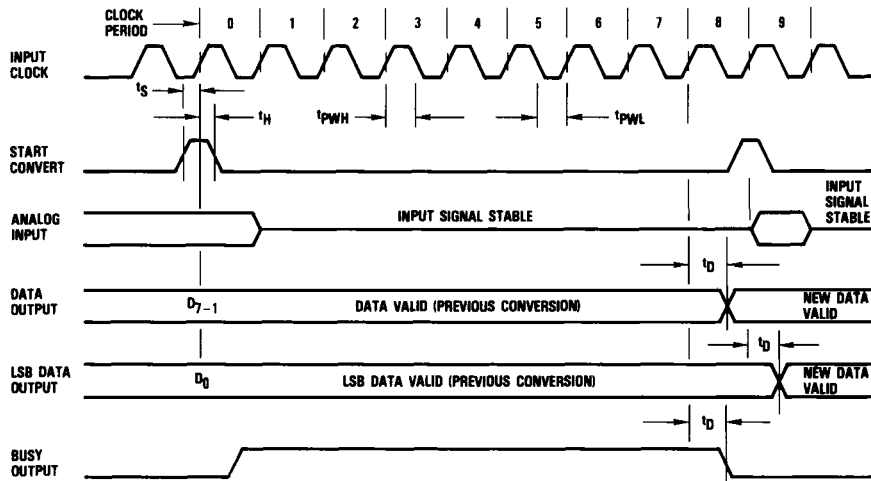


Figure 2. Simplified Analog Input Equivalent Circuit

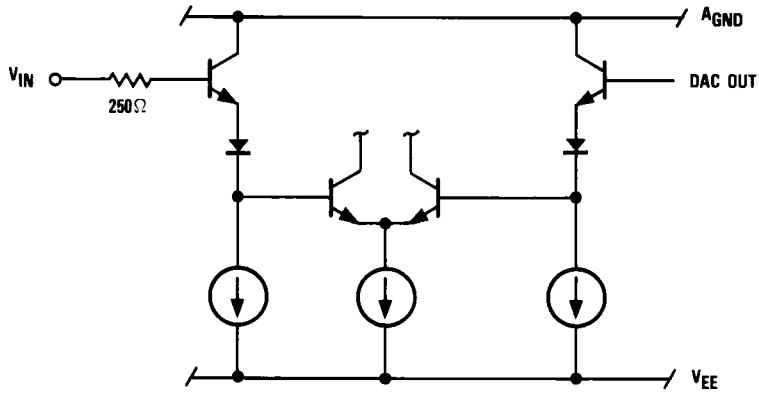


Figure 3. Digital Input Equivalent Circuit

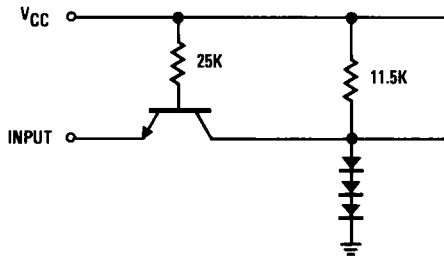
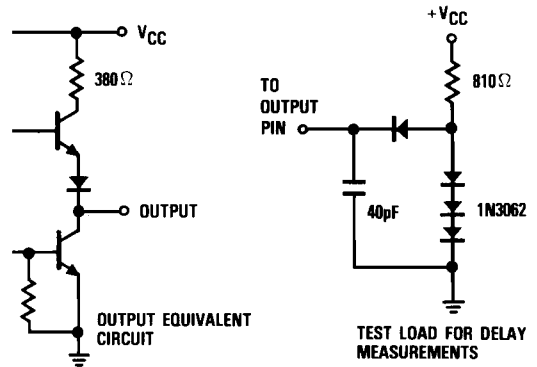


Figure 4. Output Circuits



## Absolute maximum ratings (beyond which the device may be damaged) <sup>1</sup>

### Supply Voltage

$V_{CC}$ (measured to $D_{GND}$ ).....	0 to +6.0V
$V_{EE}$ (measured to $A_{GND}$ ).....	0 to -6.0V
$A_{GND}$ (measured to $D_{GND}$ ).....	-0.5 to +0.5V

### Input Voltages

CLK, SC (measured to $D_{GND}$ ).....	-0.5 to +5.5V
$V_{IN}$ , $V_{REF}$ (measured to $A_{GND}$ ).....	+0.5V to $V_{EE}^V$

### Output

Applied voltage (measured to $D_{GND}$ ).....	-0.5 to +5.5V <sup>2</sup>
Applied current, externally forced.....	-1.0 to +6.0mA <sup>3,4</sup>
Short circuit duration (single output in high state to $D_{GND}$ ).....	1 sec

### Temperature

Operating, case.....	-60 to +140°C
junction.....	+175°C
Lead, soldering (10 seconds).....	+300°C
Storage.....	-65 to +150°C

### Notes

1. Absolute maximum ratings are limiting values applied individually while all other parameters are within specified operating conditions. Functional operation under any of these conditions is NOT implied.
2. Applied voltage must be current limited to specified range.
3. Forcing voltage must be limited to specified range.
4. Current is specified as positive when flowing into the device.

## Operating conditions

Parameter	Temperature Range						Units
	Standard			Extended			
	Min	Nom	Max	Min	Nom	Max	
$V_{CC}$ Positive Supply Voltage	4.5	5.0	5.5	4.5	5.0	5.5	V
$V_{EE}$ Negative Supply Voltage	-4.75	-5.0	-5.25	-4.75	-5.0	-5.25	V
$A_{GND}$ Analog Ground Voltage (Measured to $D_{GND}$ ) <sup>1</sup>	-0.1	0.0	+0.1	-0.1	0.0	+0.1	V
$t_{PWL}$ Clock Pulse Width, LOW	20			20			ns
$t_{PWH}$ Clock Pulse Width, HIGH	20			20			ns
$t_S$ Start Convert, Set-Up Time	7			7			ns
$t_H$ Start Convert, Hold Time	16			16			ns
$V_{IL}$ Input Voltage, Logic LOW			0.8			0.8	V
$V_{IH}$ Input Voltage, Logic HIGH	2.0			2.0			V
$I_{OL}$ Output Current, Logic LOW			4.0			4.0	mA
$I_{OH}$ Output Current, Logic HIGH			-400			-400	$\mu$ A
$V_{REF}$ Reference Voltage	-0.4	-0.5	-0.6	-0.4	-0.5	-0.6	V
$V_{IN}$ Analog Input Voltage	0.0		-0.6	0.0		-0.6	V
$T_A$ Ambient Temperature, Still Air	0		+70				°C
$T_C$ Case Temperature				-20		+95	°C

## Electrical characteristics within specified operating conditions

Parameter	Test Conditions	Temperature Range				Units
		Standard		Extended		
		Min	Max	Min	Max	
$I_{CC}$ Positive Supply Current	$V_{CC} = \text{MAX}$ , Static <sup>1</sup>		40		40	mA
$I_{EE}$ Negative Supply Current	$V_{EE} = \text{MAX}$ , $T_C = -20^\circ\text{C}$ to $+85^\circ\text{C}$		-80		-80	mA
$I_{BIAS}$ Analog Input Bias Current			10		10	$\mu\text{A}$
$I_{REF}$ Reference Current	$V_{REF} = \text{NOM}$		2.5		2.5	$\mu\text{A}$
$R_{REF}$ Total Reference Resistance		200		200		kOhms
$R_{IN}$ Analog Input Equivalent Resistance	$V_{REF} = \text{NOM}$	50		50		kOhms
$C_{IN}$ Analog Input Capacitance			10		10	pF
$I_{IL}$ Input Current, Logic LOW	$V_{CC} = \text{MAX}$ , $V_I = 0.5\text{V}$		-1.0		-1.0	mA
$I_{IH}$ Input Current, Logic HIGH	$V_{CC} = \text{MAX}$ , $V_I = 2.4\text{V}$		75		75	$\mu\text{A}$
$V_{OL}$ Output Voltage, Logic LOW	$V_{CC} = \text{MIN}$ , $I_{OL} = \text{MAX}$		0.5		0.5	V
$V_{OH}$ Output Voltage, Logic HIGH	$V_{CC} = \text{MIN}$ , $I_{OH} = \text{MAX}$	2.4		2.4		V
$I_{OS}$ Output Short Circuit Current			-25		-25	mA

Note:

1. Worst case, all digital inputs and outputs LOW.

## Switching characteristics within specified operating conditions

Parameter	Test Conditions	Temperature Range				Units
		Standard		Extended		
		Min	Max	Min	Max	
$f_S$ Maximum Clock Rate	$V_{CC}$ , $V_{EE} = \text{MIN}$	22.5		22.5		MHz
$t_C$ Conversion Time	$V_{CC}$ , $V_{EE} = \text{MIN}$		400		400	ns
$t_D$ Digital Output Delay	$V_{CC}$ , $V_{EE} = \text{MIN}$		60		60	ns

Note:

1. Only the falling edge of BUSY is tested.

## System performance characteristics within specified operating conditions

Parameter	Test Conditions	Temperature Range				Units
		Standard		Extended		
		Min	Max	Min	Max	
$E_{LI}$ Linearity Error Integral, Independent	$V_{CC}$ , $V_{EE} = \text{NOM}$		0.2		0.2	%
$E_{LD}$ Linearity Error Differential			0.2		0.2	%
$T_{CG}$ Gain Temperature Coefficient	$V_{CC}$ , $V_{EE} = \text{NOM}$		+10		+10	ppm/ $^\circ\text{C}$
$E_O$ Offset Voltage			$\pm 7$		$\pm 7$	mV
$T_{CO}$ Offset Temperature Coefficient	$V_{CC}$ , $V_{EE} = \text{NOM}$		-10		-10	$\mu\text{V}/^\circ\text{C}$
$E_G$ Gain Error			1.5		2.0	%
$T_{CIB}$ $I_{BIAS}$ Temperature Coefficient	$V_{CC}$ , $V_{EE} = \text{NOM}$		-1.0		-1.0	%/ $^\circ\text{C}$

## Application

The TDC1001 is a high-speed, TTL compatible, SAR type A/D converter. The combination of very small analog signals and high-speed digital circuitry requires careful design of supporting analog/digital circuitry. Proper physical component layout, trace routing, and provision for sizeable analog and digital grounds are as important as the electrical design.

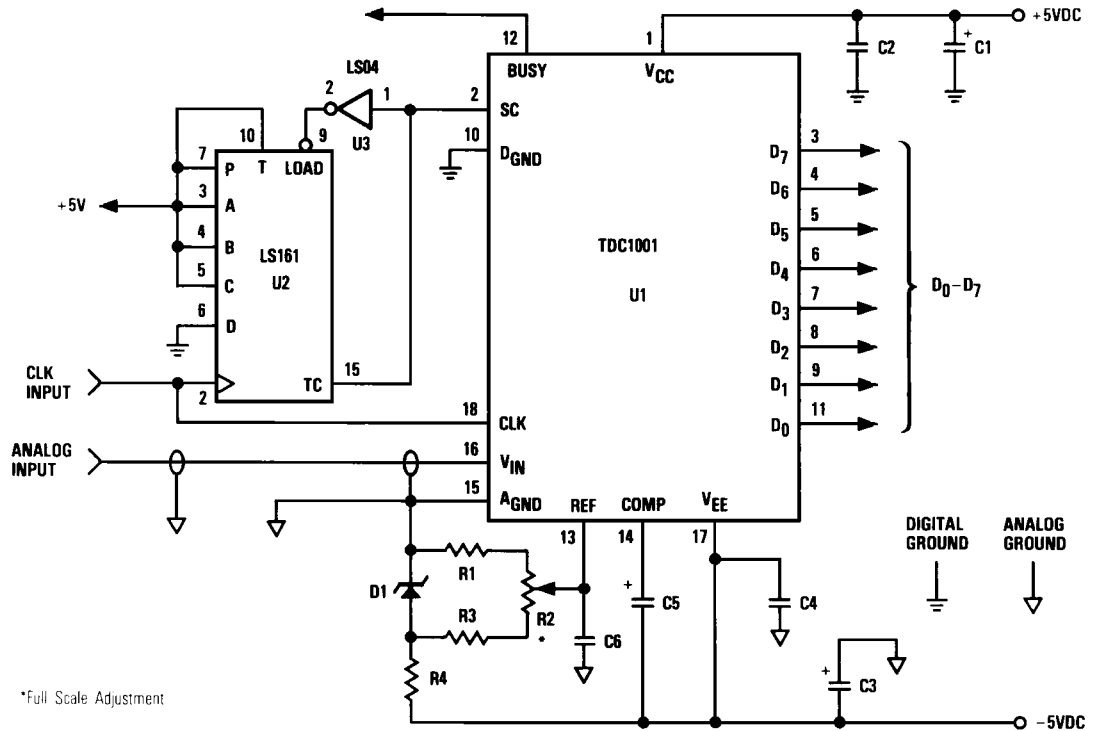
Two key design areas for fast, accurate A/D conversion are timing and grounding. The timing requirements for this device are detailed in Figure 1. Proper grounding is highly dependent on the board's mechanical layout and design constraints. In general, the noise associated with improper digital and analog ground isolation is synchronous with the clock and appears on the analog input.

Proper Design Practices Include:

- Sensitive signals such as clock, start convert, analog input, and reference should be properly routed and terminated to minimize ground noise pick-up and crosstalk. (Wirewrap is not recommended for these signals).
- Analog and digital ground planes should be substantial and common at one point only. Analog and digital power supplies should be referenced to their respective ground planes.
- Reference voltage should be stable and free of noise. Accuracy of the conversion is highly dependent on the integrity of this signal.
- The analog input should be driven from a low-impedance source ( $<25$  Ohms). This will minimize the possibility of picking up extraneous noise.
- Ceramic high frequency bypass capacitors (0.001 to  $0.01\mu\text{F}$ ) should be used at the input pins of VCC, VEE, and REF. All pins should be bypassed to AGND except VCC.
- A tantalum capacitor of greater than  $10\mu\text{F}$  should be connected from COMP (pin 14) to VEE.

**A**

Figure 5. Typical Interface Circuit



## Parts List

### Resistors

R1	909 Ohms	1%	1/8W
R2	100 Ohms		Multi-Turn Cermet Pot
R3	1.33 kOhms	1%	1/8W
R4	2.49 kOhms	1%	1/8W

### Capacitors

C1, C3, C5	10.0 $\mu$ F	25V
C2, C4	0.001 $\mu$ F	50V
C6	0.005 $\mu$ F	50V

### Integrated Circuits

U1	TDC1001J8	TRW 8-bit A/D Converter
U2	74LS161	TTL 4-bit Counter
U3	74LS04	TTL Hex Inverter
D1	LM113-1.22	1.22V Bandgap Voltage Reference



## Ordering Information

Product Number	Temperature Range	Screening	Package	Package Marking
TDC1001B8C	STD- $T_A = 0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	Commercial	18 Pin CERDIP	1001B8C
TDC1001B8A	EXT- $T_C = -55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	High Reliability	18 Pin CERDIP	1001B8A

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