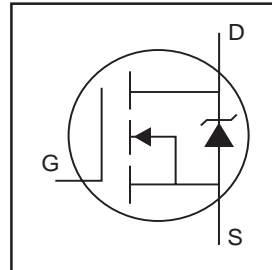


**IRF1404S**

**IRF1404L**

**HEXFET® Power MOSFET**

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



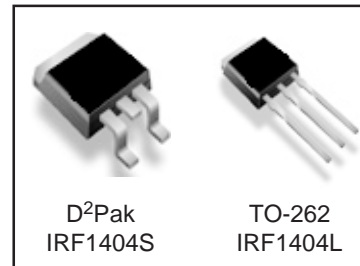
$V_{DSS} = 40V$
$R_{DS(on)} = 0.004\Omega$
$I_D = 162A\text{⑥}$

**Description**

Seventh Generation HEXFET® Power MOSFETs from International Rectifier utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D<sup>2</sup>Pak is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D<sup>2</sup>Pak is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0W in a typical surface mount application.

The through-hole version (IRF1404L) is available for low-profile applications.



**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V\text{⑦}$	162⑥	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V\text{⑦}$	115⑥	
$I_{DM}$	Pulsed Drain Current ①⑦	650	
$P_D @ T_A = 25^\circ C$	Power Dissipation	3.8	W
$P_D @ T_C = 25^\circ C$	Power Dissipation	200	W
	Linear Derating Factor	1.3	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$	Single Pulse Avalanche Energy②	519	mJ
$I_{AR}$	Avalanche Current①	95	A
$E_{AR}$	Repetitive Avalanche Energy①	20	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑦	5.0	V/ns
$T_J$	Operating Junction and	-55 to +175	°C
$T_{STG}$	Storage Temperature Range	-55 to +175	
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

**Thermal Resistance**

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	0.75	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mounted, steady-state)*	—	40	

# IRF1404S/L

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.036	—	V/ $^\circ\text{C}$	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	0.0035	0.004	$\Omega$	$V_{GS} = 10V, I_D = 95A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = 10V, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	106	—	—	S	$V_{DS} = 25V, I_D = 60A$ ⑦
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 32V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	160	200	nC	$I_D = 95A$
$Q_{gs}$	Gate-to-Source Charge	—	35	—		$V_{DS} = 32V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	42	60		$V_{GS} = 10V$ ④ ⑦
$t_{d(on)}$	Turn-On Delay Time	—	17	—	ns	$V_{DD} = 20V$
$t_r$	Rise Time	—	140	—		$I_D = 95A$
$t_{d(off)}$	Turn-Off Delay Time	—	72	—		$R_G = 2.5\Omega$
$t_f$	Fall Time	—	26	—		$R_D = 0.21\Omega$ ④ ⑦
$L_S$	Internal Source Inductance	—	7.5	—	nH	Between lead, and center of die contact
$C_{iss}$	Input Capacitance	—	7360	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	1680	—		$V_{DS} = 25V$
$C_{rss}$	Reverse Transfer Capacitance	—	240	—		$f = 1.0\text{MHz}$ , See Fig. 5 ⑦
$C_{oss}$	Output Capacitance	—	6630	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	1490	—		$V_{GS} = 0V, V_{DS} = 32V, f = 1.0\text{MHz}$
$C_{oss\text{ eff.}}$	Effective Output Capacitance ⑤ ⑦	—	1540	—		$V_{GS} = 0V, V_{DS} = 0V$ to $32V$

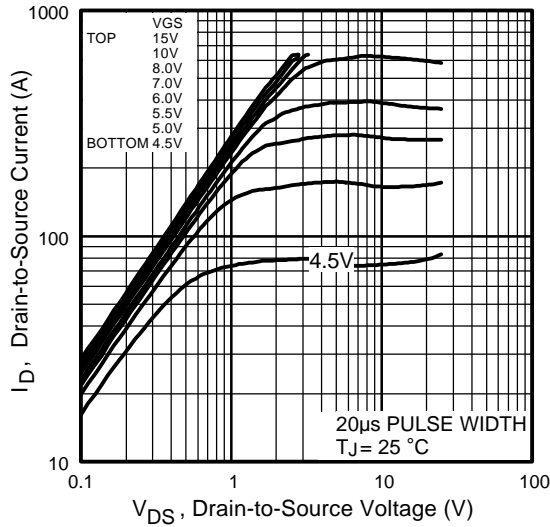
## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	162 ⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	650		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 95A, V_{GS} = 0V$ ④
$t_{rr}$	Reverse Recovery Time	—	71	110	ns	$T_J = 25^\circ\text{C}, I_F = 95A$
$Q_{rr}$	Reverse Recovery Charge	—	180	270	nC	$di/dt = 100A/\mu s$ ④ ⑦
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				

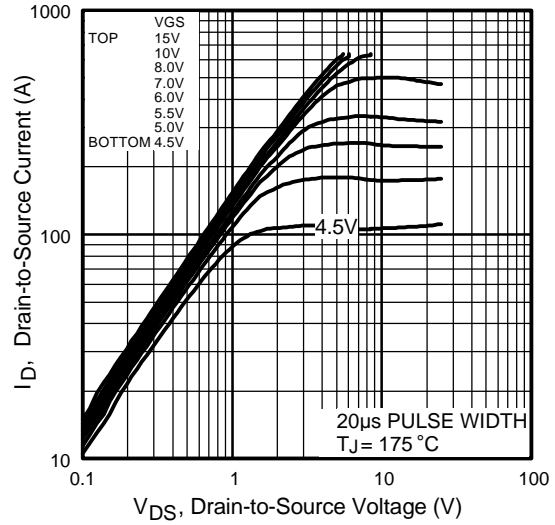
### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 0.12\text{mH}$ ,  $R_G = 25\Omega$ ,  $I_{AS} = 95A$ . (See Figure 12)
- ③  $I_{SD} \leq 95A$ ,  $di/dt \leq 150A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{oss\text{ eff.}}$  is a fixed capacitance that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- ⑥ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 75A
- ⑦ Use IRF1404 data and test conditions.

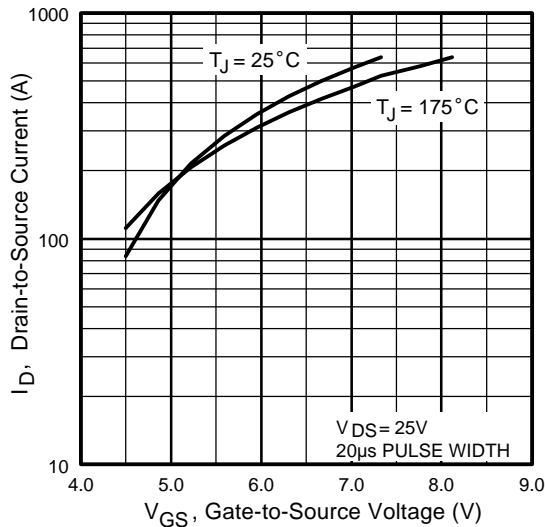
# IRF1404S/L



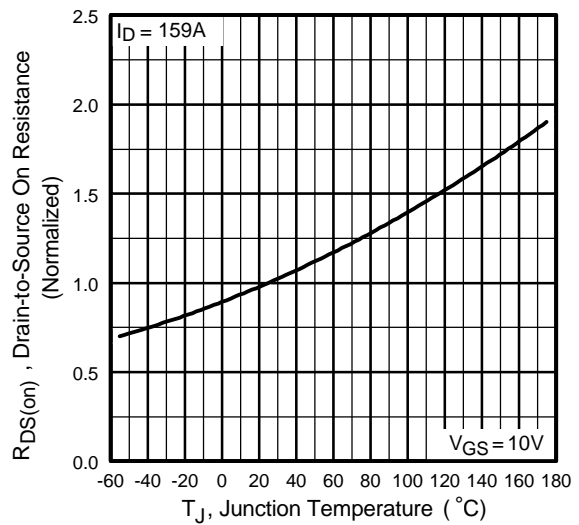
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics



**Fig 3.** Typical Transfer Characteristics

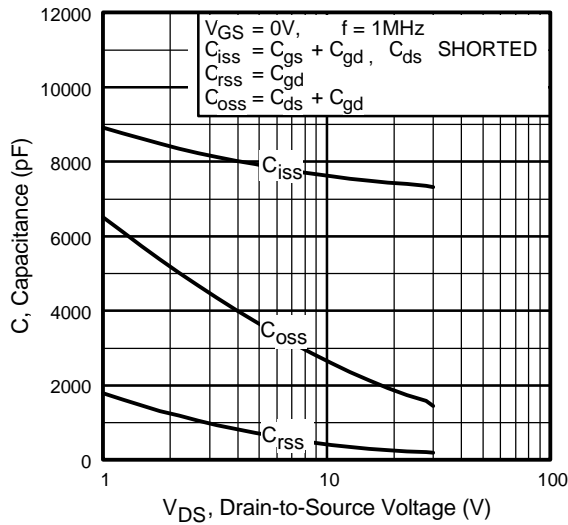


**Fig 4.** Normalized On-Resistance Vs. Temperature

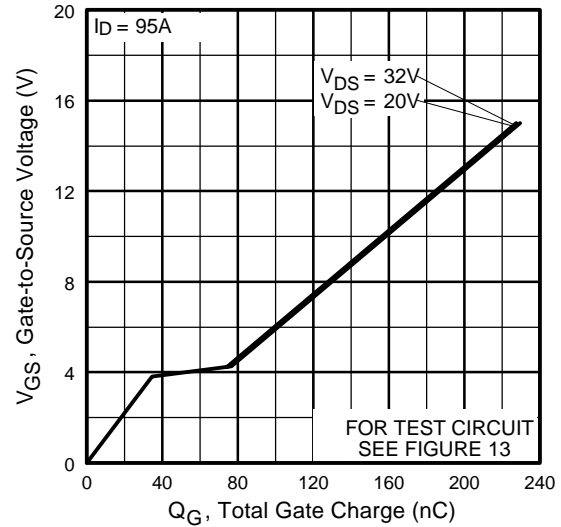


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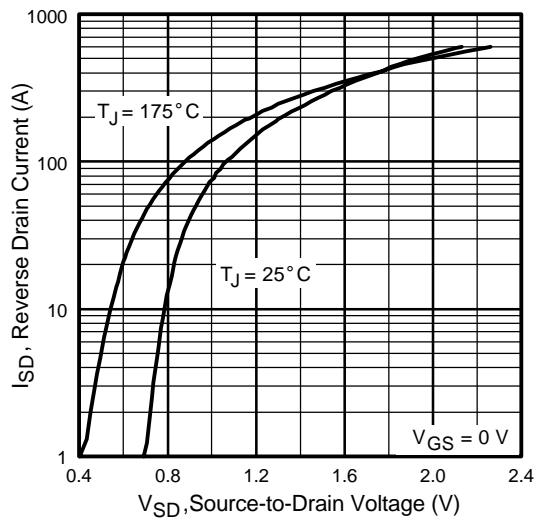
# IRF1404S/L



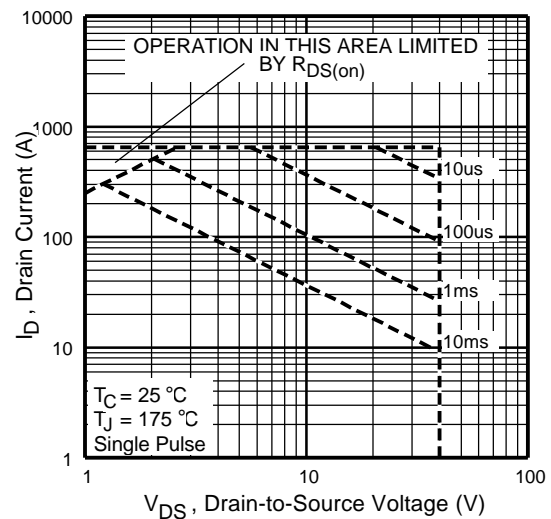
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage

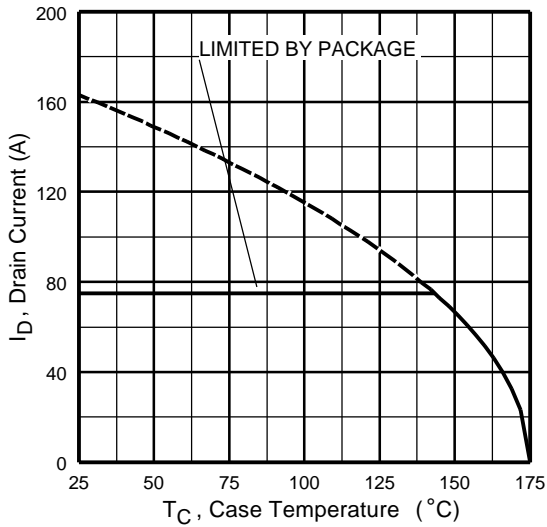


**Fig 7.** Typical Source-Drain Diode Forward Voltage

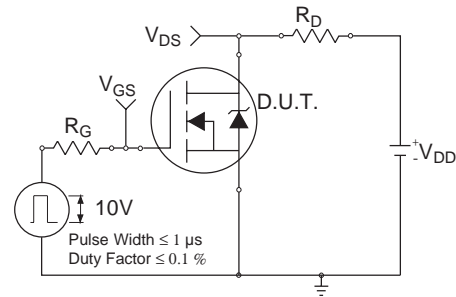


**Fig 8.** Maximum Safe Operating Area

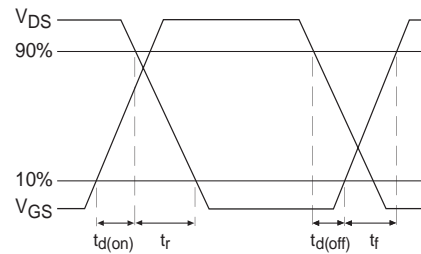
# IRF1404S/L



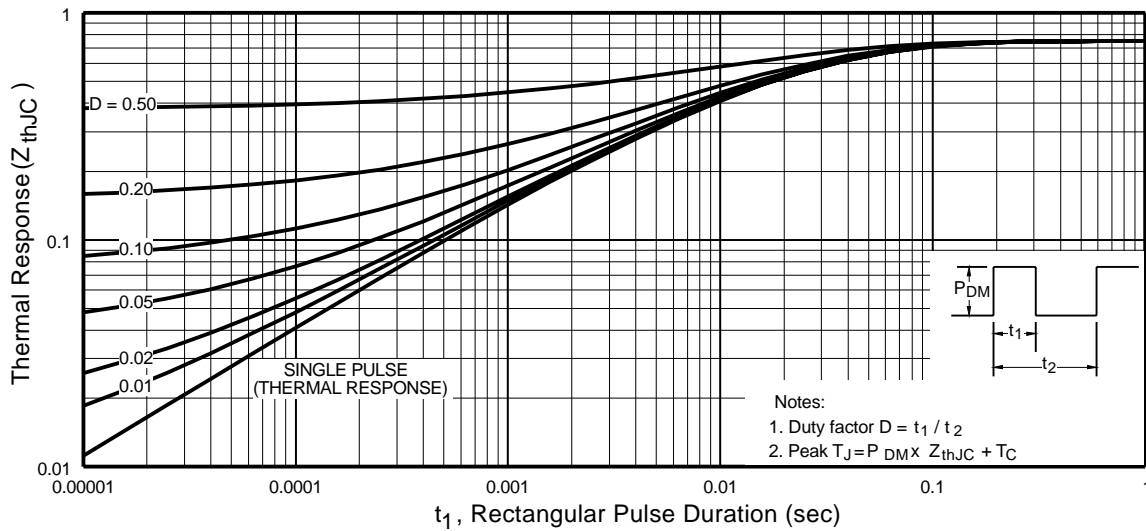
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit

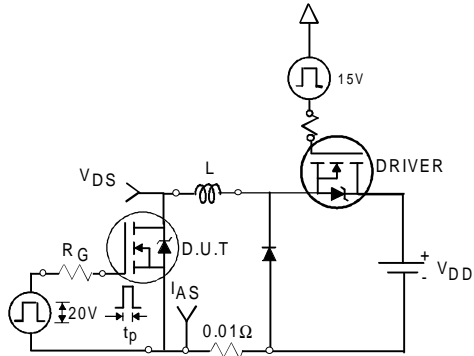


**Fig 10b.** Switching Time Waveforms

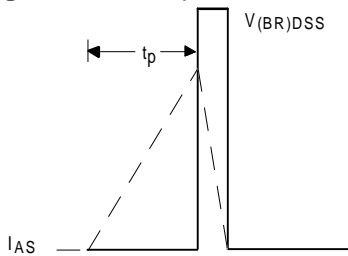


**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

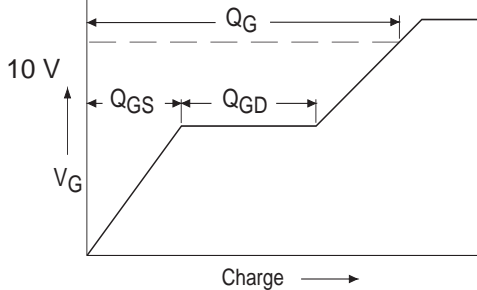
# IRF1404S/L



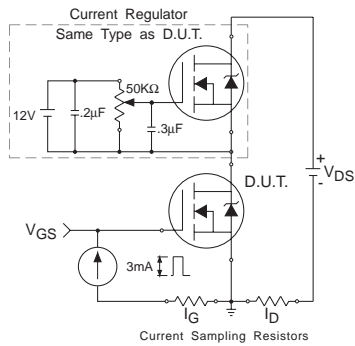
**Fig 12a.** Unclamped Inductive Test Circuit



**Fig 12b.** Unclamped Inductive Waveforms

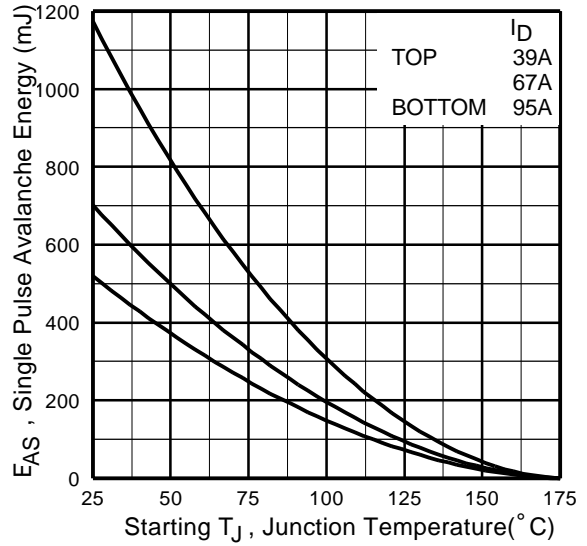


**Fig 13a.** Basic Gate Charge Waveform

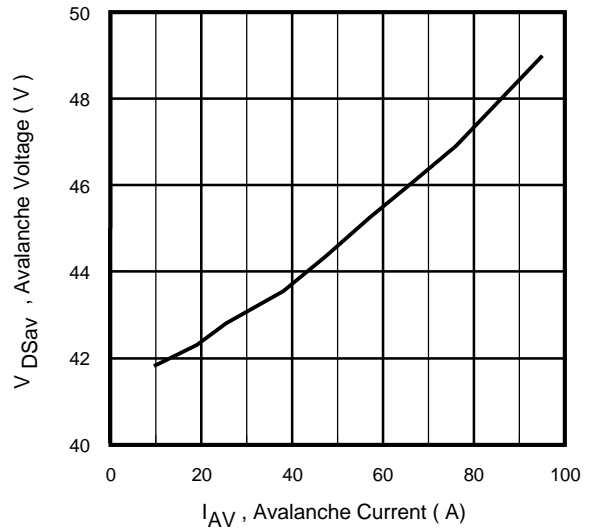


**Fig 13b.** Gate Charge Test Circuit

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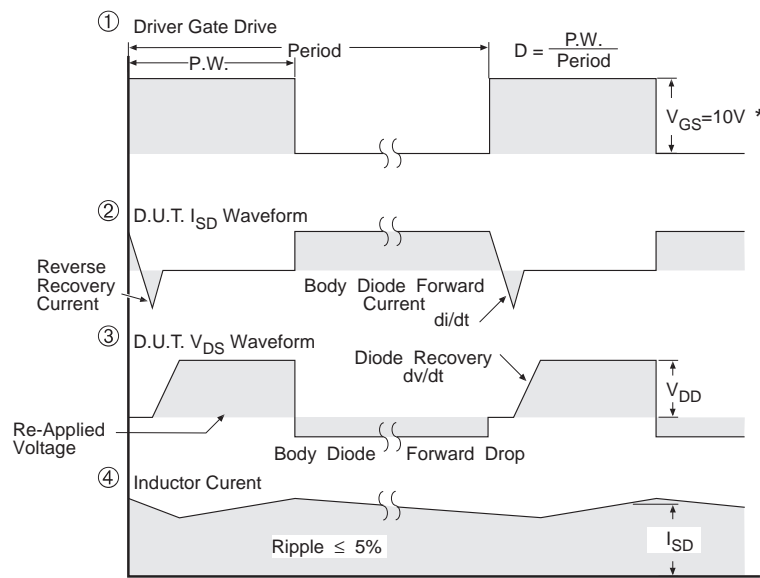
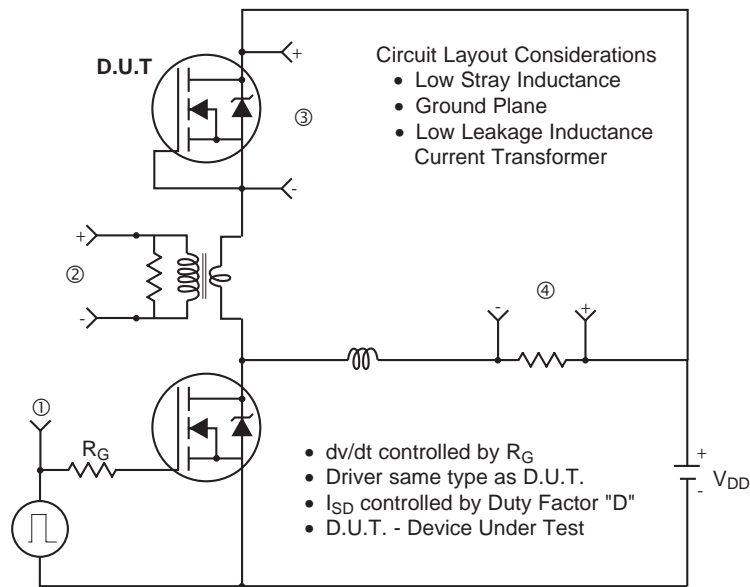


**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 12d.** Typical Drain-to-Source Voltage Vs. Avalanche Current

**Peak Diode Recovery dv/dt Test Circuit**



\*  $V_{GS} = 5V$  for Logic Level Devices

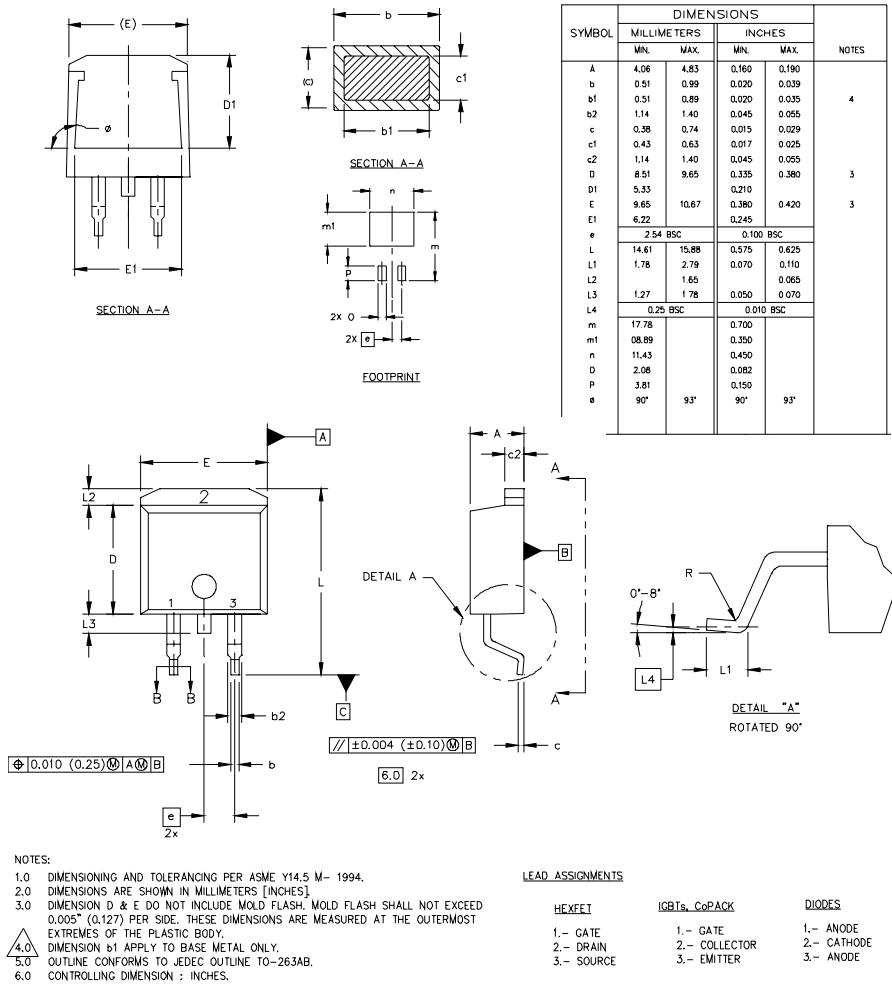
**Fig 14.** For N-channel HEXFET® Power MOSFETs



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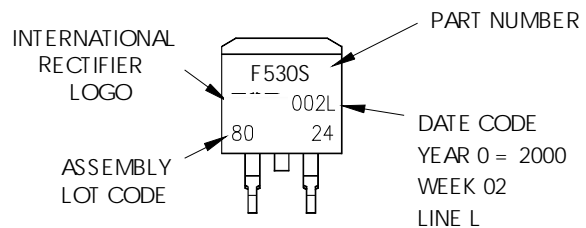
# IRF1404S/L

## D<sup>2</sup>Pak Package Outline



## D<sup>2</sup>Pak Part Marking Information

EXAMPLE: THIS IS AN IRF530S WITH  
 LOT CODE 8024  
 ASSEMBLED ON WW02, 2000  
 IN THE ASSEMBLY LINE "L"



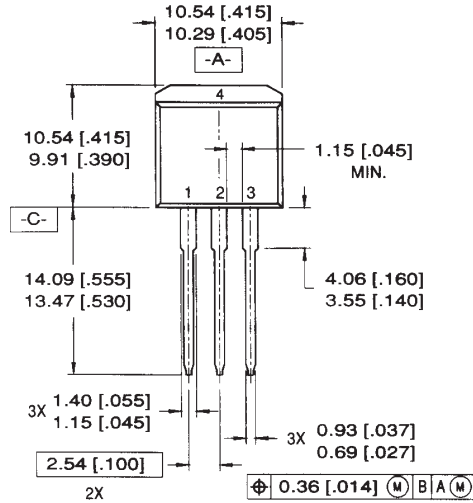




**KERSEMI**

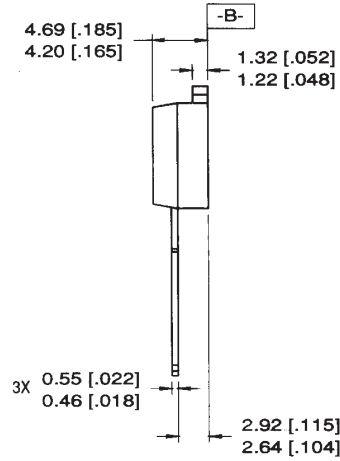
**IRF1404S/L**

**TO-262 Package Outline**



**LEAD ASSIGNMENTS**

- 1 = GATE      3 = SOURCE
- 2 = DRAIN    4 = DRAIN

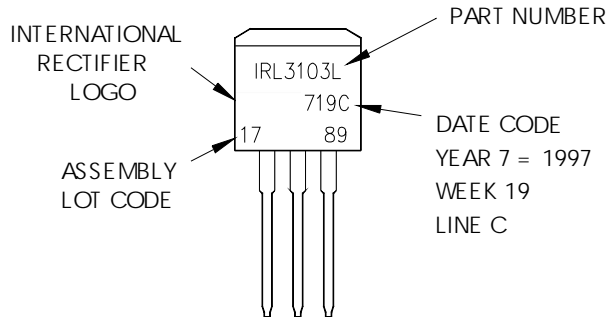


**NOTES:**

1. DIMENSIONING & TOLERANCING PER ANSI Y14.5M-1982
2. CONTROLLING DIMENSION: INCH.
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. HEATSINK & LEAD DIMENSIONS DO NOT INCLUDE BURRS.

**TO-262 Part Marking Information**

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON VW 19, 1997  
 IN THE ASSEMBLY LINE "C"

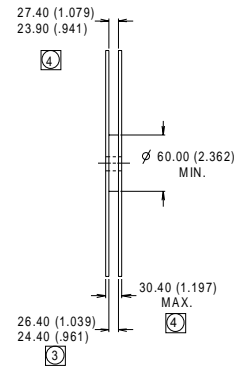
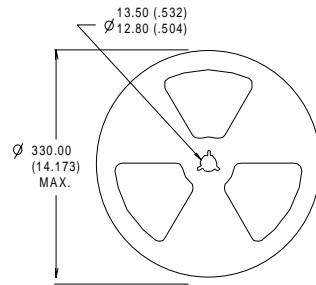
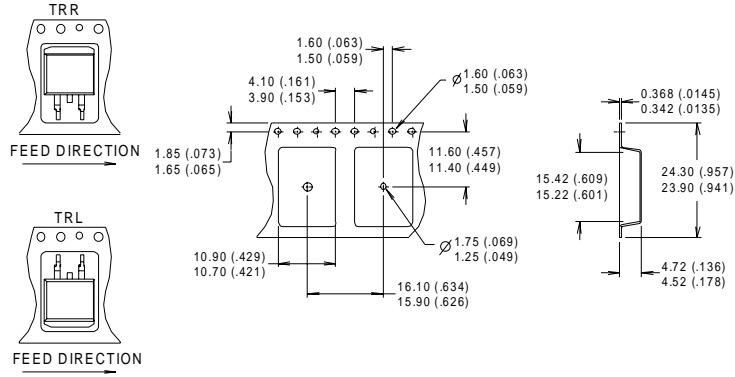




**KERSEMI**

# IRF1404S/L

## D<sup>2</sup>Pak Tape & Reel Information



- NOTES :
1. CONFORMS TO EIA-418.
  2. CONTROLLING DIMENSION: MILLIMETER.
  - ③ DIMENSION MEASURED @ HUB.
  - ④ INCLUDES FLANGE DISTORTION @ OUTER EDGE.