

AmPAL*HC29M16/AmPALHCT29M16

24-Pin E²-Based CMOS Programmable Array Logic

ADVANCE INFORMATION

DISTINCTIVE CHARACTERISTICS

- High-performance semi-custom logic replacement; Electrically Erasable (E²) technology allows reprogrammability
- 16 bidirectional user-programmable I/O logic macrocells for Combinatorial/Registered/Latched operation
- Output Enable controlled by a pin or product terms
- Variable product term distribution for increased design flexibility
- Programmable clock selection with two clocks/latch enables (LEs) and LOW/HIGH clock/LE polarity
- Register/Latch PRELOAD permits full logical verification
- Available in high-speed (t_{PD} = 35 ns, f_{MAX} = 20 MHz) and standard-speed (t_{PD} = 45 ns, f_{MAX} = 15.0 MHz) versions
- 100% post-programming functional yield (PPFY), fast programming and excellent reliability assured through proven E²PROM technology
- Full-function AC and DC testing at the factory
- CMOS and TTL-compatible versions
- 24-pin 300-mil DIP and 28-pin chip carrier packages

GENERAL DESCRIPTION

The AmPAL29M16 is a high-speed, E²-based CMOS Programmable Array Logic device designed for general logic replacement in TTL or CMOS digital systems. It offers high-speed, low-power consumption, high programming yield, fast programming and excellent reliability. Programmable logic devices (PLDs) combine the flexibility of custom logic with the off-the-shelf availability of standard products, providing major advantages over other semicustom solutions such as gate arrays and standard cells, including reduced development time and low up-front development cost.

The AmPAL29M16 uses the familiar sum-of-products (AND-OR) structure, allowing users to customize logic functions by programming the device for specific applications. It provides up to twenty-nine array inputs and sixteen outputs. It incorporates AMD's unique input/output logic macrocell which provides flexible input/output structure and polarity, flexible feedback selection, multiple Output Enable choices, and a programmable clocking scheme. The macrocells can be individually programmed as "Combinatorial", "Registered", or "Latched" with active-HIGH or active-LOW polarity. The flexibility of the logic macrocells permits the

system designer to tailor the device to particular application requirements.

Increased logic power has been built into the AmPAL29M16 by providing a variable number of logical product terms per output. Eight outputs have eight product terms each, four outputs have twelve product terms each, and the other four outputs have sixteen product terms each. This variable product-term distribution allows complex functions to be implemented in a single PAL device. Each output can be dynamically controlled by an Output Enable pin or Output Enable product terms. Each output can also be permanently enabled or disabled.

System operation has been enhanced by the addition of common asynchronous-PRESET and RESET product terms and a power-up RESET feature. The AmPAL29M16 also incorporates PRELOAD and Observability functions which permit full logical verification of the design.

The AmPAL29M16 is compatible with HCT (High-performance CMOS & TTL) and HC (High-performance CMOS) logic levels and is offered in the space-saving 300-mil DIP package as well as chip carrier surface-mount packages.

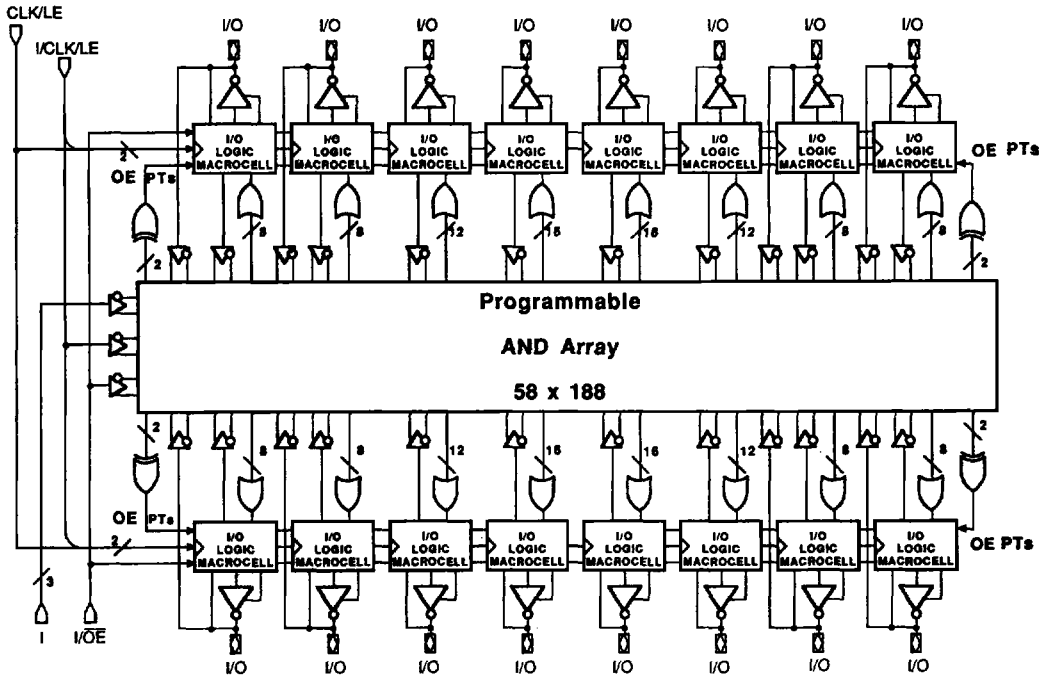
AmPAL*HC29M16/AmPALHCT29M16

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Publication #	Rev.	Amendment
08740	A	/0
Issue Date: October 1986		

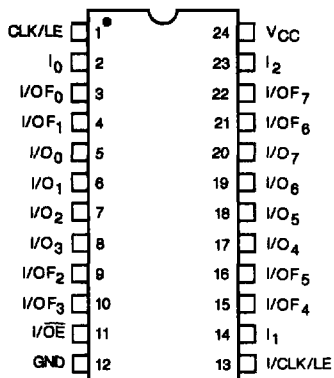
BLOCK DIAGRAM



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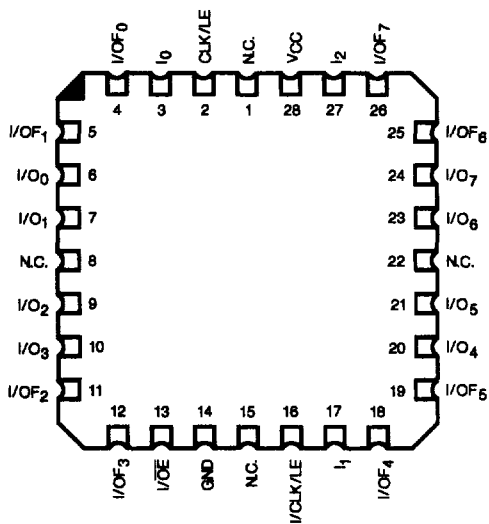
CONNECTION DIAGRAMS
Top View

DIPs



CD010271

LCC*



CD010280

*Also available in PLCC. Pinouts identical to LCC.

Note: Pin 1 is marked for orientation.

PIN DESCRIPTION

The following describes the functionality of all the pins on the 24-pin DIP. The 28-pin chip carrier has the same functionality with NO CONNECTS on pins 1,8,15,22.

CLK/LE (PIN 1):

Used as dedicated clock/latch enable pin for all registers/latches on the device if so selected. (See I/O Logic Macrocell Configurations.) This pin is a clock pin for macrocells configured as registers and a latch enable pin for macrocells configured as latches.

I/CLK/LE PIN (PIN 13):

Used as dedicated input or as an alternate clock/latch enable pin for all the registers/latches if so selected. (See I/O Logic Macrocell Configurations.) This pin is a clock pin for macrocells configured as registers and a latch enable pin for macrocells configured as latches.

I/OE PIN (PIN 11):

Used as a dedicated input pin to the AND array or as the Output Enable control pin (Active LOW) for all macrocells with pin-controlled Output Enable selected.

I₀-I₂ (PINS 2,14,23):

Dedicated input pins.

I/O₀-I/O₇ (PINS 3,4,9,10,15,16,21,22):

Eight bidirectional I/O pins with two independent feedback paths to the AND array. The first feedback path is a dedicated I/O pin feedback to the AND array for combinatorial input. The second feedback path consists of direct register/latch feedback to the array (see Figure 1).

I/O₀-I/O₇ (PINS 5,6,7,8,17,18,19,20):

Eight bidirectional I/O pins with user-programmable register/latch or I/O pin feedback to the AND array (see Figure 1).

V_{CC} (PIN 24):

Supply Voltage

GND (PIN 12):

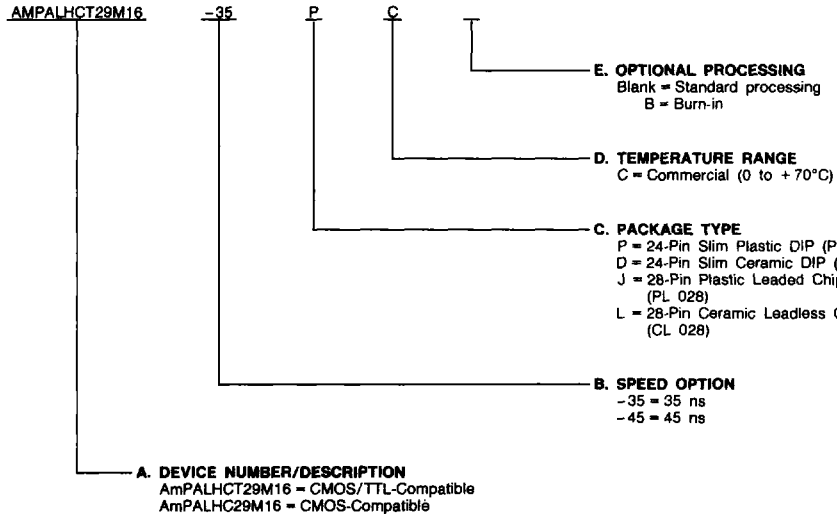
Circuit Ground

ORDERING INFORMATION

Standard Products

AMD standard products are available in several packages and operating ranges. The order number (Valid Combination) is formed by a combination of:

- A. Device Number**
- B. Speed Option** (if applicable)
- C. Package Type**
- D. Temperature Range**
- E. Optional Processing**



Valid Combinations

Valid Combinations	
AmPALHCT29M16-35, -45	PC, DC, DCB, JC, LC, LCB
AmPALHC29M16-35, -45	JC, LC, LCB

Valid Combinations list configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

FUNCTIONAL DESCRIPTION

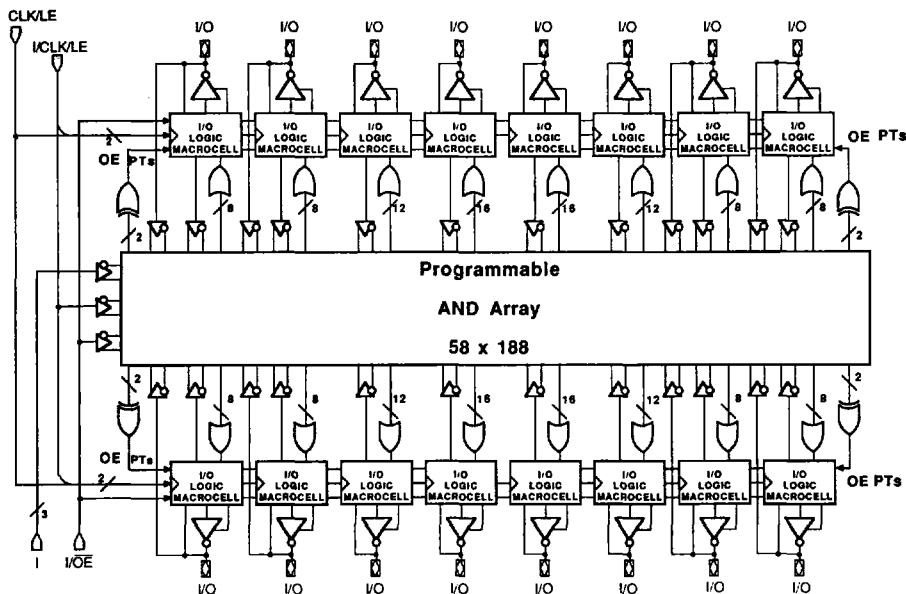
Inputs

The AmPAL29M16 has 29 inputs to drive each product term (up to 58 inputs with both TRUE and complement versions available to the AND array) as shown in the block diagram below. Of these 29 inputs, 3 are dedicated inputs, 16 are from 8 I/O logic macrocells with 2 feedbacks, 8 are from other I/O

logic macrocells with single feedback, 1 is for I/CLOCK/LE and 1 is for I/OE input.

Initially the AND-array gates are disconnected from all the inputs. This condition represents a logical TRUE to the AND array. By selectively programming the E²cells, the AND array may be connected to either the TRUE input or the complement input. When both the TRUE and complement inputs are connected, a logical FALSE results at the output of the AND gate.

BLOCK DIAGRAM



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Product Terms

The degree of programmability and complexity of a PAL device is determined by the number of connections that form the programmable-AND and OR gates. Each programmable-AND gate is called a product term. The AmPAL29M16 has 188 product terms. 176 of these product terms provide logic capability and 12 are architectural or control product terms. Among the 12 control product terms, 2 are for common Asynchronous-PRESET and RESET, 1 is for Observability, and 1 is for PRELOAD. The other 8 are common Output Enable product terms. The Output Enable of each bank of 4 macrocells can be programmed to be controlled by a common Output Enable pin or 2 AND/XOR product terms. It may be also permanently enabled or permanently disabled.

Each product term on the AmPAL29M16 consists of a 58-input AND gate. The outputs of these AND gates are connected to a fixed-OR plane. Product terms are allocated to OR gates in a variable distribution across the device ranging from 8-to-16 wide, with an average of 11 logical product terms per output. Increased number of product terms per output allows more complex functions to be implemented in a single PAL device. This flexibility aids in implementing functions such as counters, exclusive-OR functions, or complex state machines, where different states require different numbers of product terms.

Common asynchronous-PRESET and RESET product terms are connected to all Registered/Latched inputs/outputs. When the asynchronous-PRESET product term is asserted (HIGH) all the registers/latches will immediately be loaded with a HIGH, independent of the clock. When the asynchronous-RESET product term is asserted (HIGH) all the registers/latches will be immediately loaded with a LOW, independent of the clock. The actual output state will depend on the macrocell polarity selection. The latches must be in latched mode (not transparent mode) for the RESET/PRESET, PRELOAD, and power-up RESET modes to be meaningful.

Input/Output Logic Macrocells

The I/O logic macrocell allows the user the flexibility of defining the architecture of each input or output on an individual basis. It also provides the capability of using the associated pin either as an input or an output.

The AmPAL29M16 has 16 macrocells, one for each I/O pin. Each I/O macrocell can be programmed for combinatorial, registered or latched operation (see Figure 1). Combinatorial output is desired when the PAL device is used to replace combinatorial glue logic. Registers are used in synchronous logic applications while latches are used in asynchronous applications where speed is critical. The output polarity for each macrocell in each of the three modes of operation is

Table 1. AmpPAL29M16 I/O Logic Macrocell Architecture Selections

S3	I/O Cell
1	Output Cell
0	Input Cell

S2	Storage Element
1	Register
0	Latch

S1	Output Type
1	Combinatorial
0	Register/Latch

S0	Output Polarity
1	Active LOW
0	Active HIGH

S8	Feedback*
1	Register/Latch
0	I/O

*Applies to macrocells with single feedback only.

TC003961

Table 1. AmpPAL29M16 I/O Logic Macrocell Clock Polarity & Output Enable Selections (Cont'd.)

S4	S5	Clock Edge/Latch Enable Level	S6	S7	Output Buffer Control
1	1	CLK/LE pin positive-going edge, active-HIGH LE	1	1	Pin-Controlled 3-State Enable
1	0	CLK/LE pin negative-going edge, active-LOW LE	1	0	XOR PT-Controlled 3-State Enable
0	1	I/CLK/LE pin positive-going edge, active-HIGH LE	0	1	Permanently Enabled (Output only)
0	0	I/CLK/LE pin negative-going edge, active-LOW LE	0	0	Permanently Disabled (Input only)

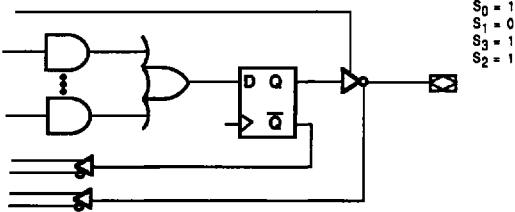
TC003971

1 = Erased State (Charged or disconnected)
 0 = Programmed State (Discharged or connected)



SOME POSSIBLE CONFIGURATIONS OF THE INPUT/OUTPUT LOGIC MACROCELL

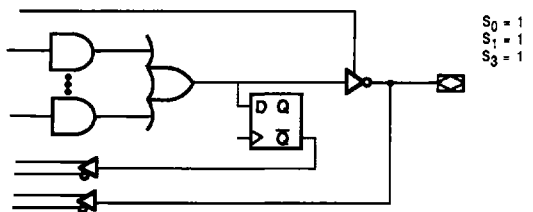
OUTPUT REGISTERED/ACTIVE LOW



LD000961

$S_0 = 1$
 $S_1 = 0$
 $S_3 = 1$
 $S_2 = 1$

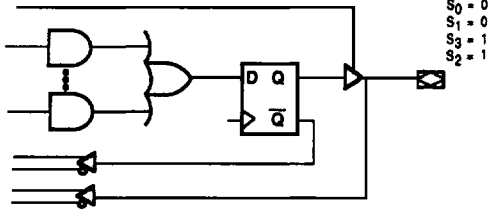
OUTPUT COMBINATORIAL/ACTIVE LOW



LD000951

$S_0 = 1$
 $S_1 = 1$
 $S_3 = 1$

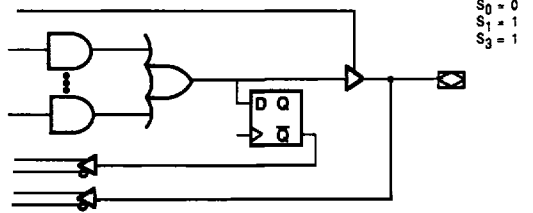
OUTPUT REGISTERED/ACTIVE HIGH



LD000971

$S_0 = 0$
 $S_1 = 0$
 $S_3 = 1$
 $S_2 = 1$

OUTPUT COMBINATORIAL/ACTIVE HIGH

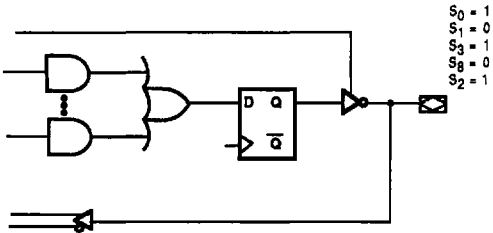


LD000981

$S_0 = 0$
 $S_1 = 1$
 $S_3 = 1$

Figure 2A: Dual Feedback Macrocells

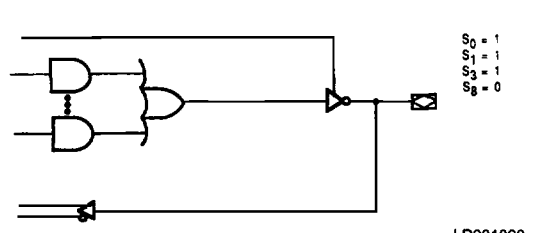
OUTPUT REGISTERED/ACTIVE LOW, I/O FEEDBACK



LD000991

$S_0 = 1$
 $S_1 = 0$
 $S_3 = 1$
 $S_6 = 0$
 $S_2 = 1$

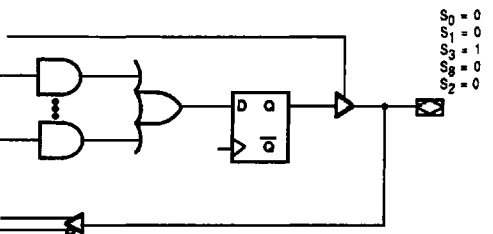
OUTPUT COMBINATORIAL/ACTIVE LOW, I/O FEEDBACK



LD001000

$S_0 = 1$
 $S_1 = 1$
 $S_3 = 1$
 $S_6 = 0$

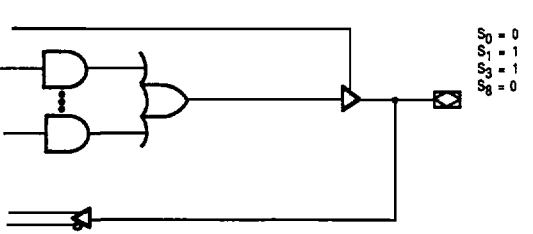
OUTPUT LATCHED/ACTIVE HIGH, I/O FEEDBACK



LD001011

$S_0 = 0$
 $S_1 = 0$
 $S_3 = 1$
 $S_6 = 0$
 $S_2 = 0$

OUTPUT COMBINATORIAL/ACTIVE HIGH, I/O FEEDBACK

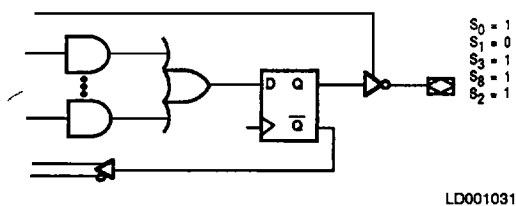


LD001021

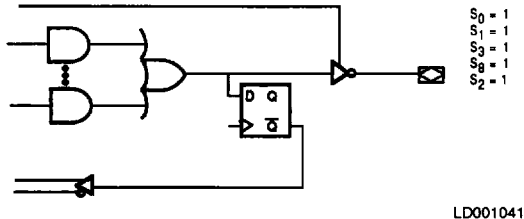
$S_0 = 0$
 $S_1 = 1$
 $S_3 = 1$
 $S_6 = 0$

Figure 2B: Single Feedback Macrocells

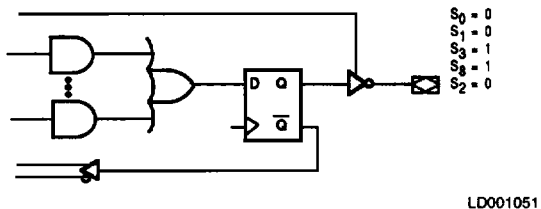
OUTPUT REGISTERED/ACTIVE LOW, REG. FEEDBACK



OUTPUT COMBINATORIAL/ACTIVE LOW, REG. FEEDBACK



OUTPUT LATCHED/ACTIVE LOW, LATCHED FEEDBACK



OUTPUT COMBINATORIAL/ACTIVE LOW, LATCH FEEDBACK

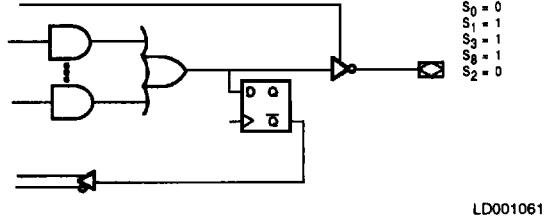


Figure 2B: Single Feedback Macrocells (Cont'd.)

INPUT REGISTERED/LATCHED

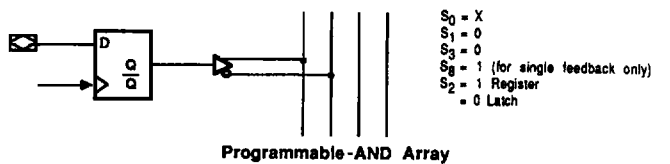
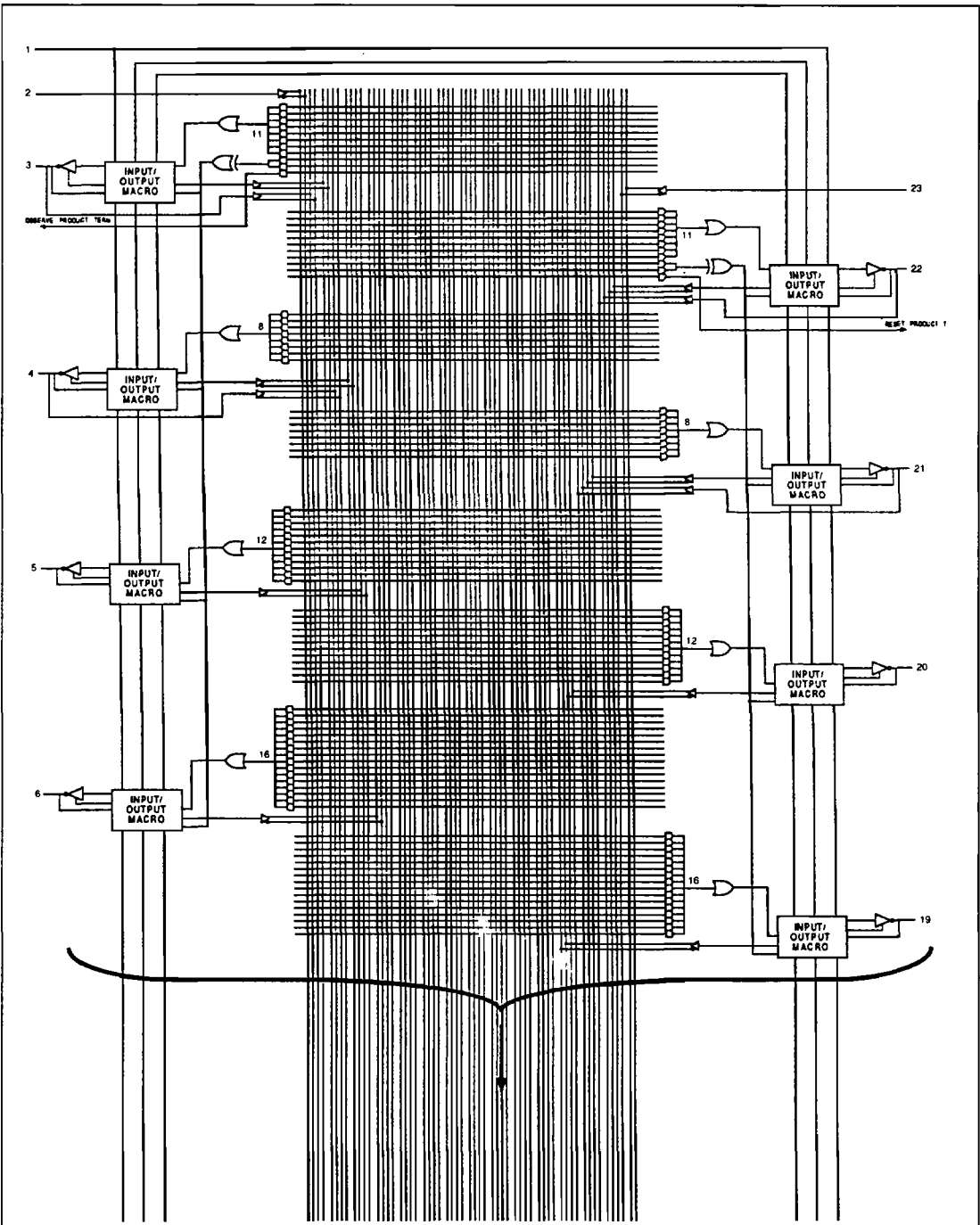


Figure 2C: All Macrocells



LD001350

Figure 3. AmPAL29M16 Logic Diagram

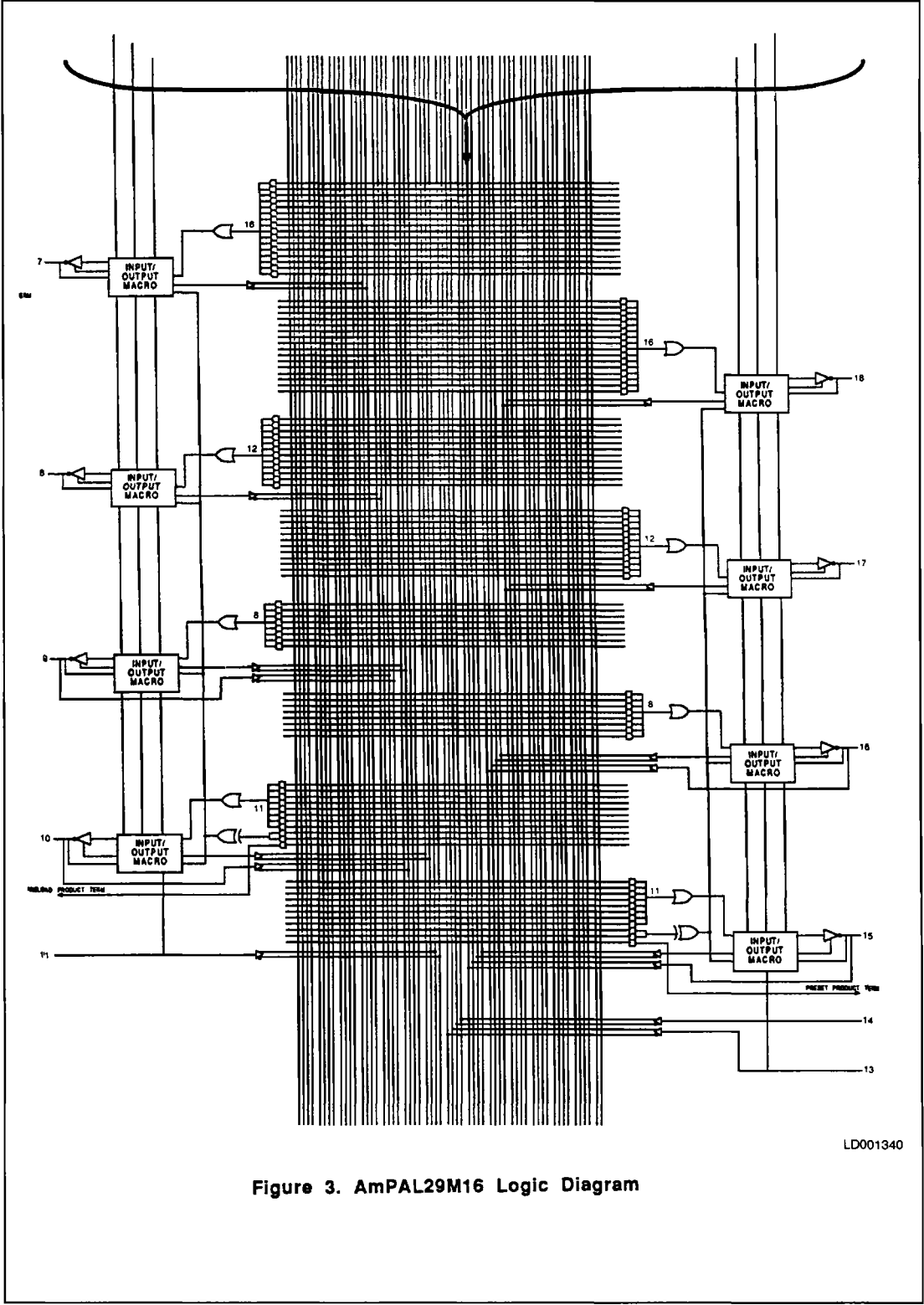


Figure 3. AmpAL29M16 Logic Diagram

Designed in Testability and Debugging

PRELOAD

To simplify testing, the AmPAL29M16 is designed with PRELOAD circuitry that provides an easy method for testing logical functionality. Both TTL-level and supervoltage-enabled PRELOAD modes are available. This offers even more test capability than previously implemented in AMD's PAL devices. The TTL-level PRELOAD product term can be useful during debugging, where supervoltages may not be available.

PRELOAD allows any arbitrary state value to be loaded into the registers/latches of the device. A typical functional-test sequence would be to verify all possible state transitions for the device being tested. This requires the ability to set the state registers into an arbitrary "present state" value and to set the devices inputs into any arbitrary "present input" value. Once this is done, the state machine is clocked into a new state, or "next state", which can be checked to validate the transition from the "present state". In this way any transition can be checked.

Since PRELOAD can provide the capability to go directly to any desired arbitrary state, test sequences may be greatly shortened. Also, all possible states can be tested, thus greatly reducing test time and development costs and guaranteeing proper in-system operation.

Observability

The output register/latch observability product term, when asserted, suppresses the combinatorial output data from appearing on the I/O pin and allows the observation of the contents of the register/latch on the output pin for each of the logic macrocells. This unique feature allows for easy debugging and tracing of the buried state machines. In addition, a capability of supervoltage observability is also provided.

Power-Up Reset

All the device registers/latches have been designed to reset during device power-up. Following the power-up, all registers/latches will be cleared, setting the outputs to a state determined by the output select multiplexer. This feature provides extra flexibility to the designer and is especially valuable in simplifying state machine initialization.

Security Cell

A security cell is provided on each device to prevent unauthorized copying of the user's proprietary logic design. Once programmed, the security cell disables the programming, verification, PRELOAD, and the observability modes. The only way to erase the protection cell is by charging the entire array and architecture cells, in which case no proprietary design can be copied. (This cell should be programmed only after the rest of the device has been completely programmed and verified.)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature -65 to +150°C
 Ambient Temperature under bias..... -55 to +125°C
 Supply Voltage with
 Respect to Ground.....-0.5 V to +7.0 V
 DC Output Voltage.....-0.5 V to V_{CC} + 0.5 V
 DC Input Voltage
 (Except Pin 1/OE)-0.5 V to V_{CC} + 0.5 V
 DC Input Voltage (Pin 1/OE)-0.6 V to +17 V
 DC Input Current-1 mA to +1 mA

Stresses above those listed under **ABSOLUTE MAXIMUM RATINGS** may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

OPERATING RANGES

Commercial (C) Devices — HCT Devices
 Temperature (T_A) Operating Free Air0°C to +70°C
 Supply Voltage (V_{CC})+4.75 to +5.25 V
 Commercial (C) Devices — HC Devices
 Temperature (T_A)0°C to +70°C
 Supply Voltage (V_{CC})+4.50 to +5.50 V
 Military (M) Devices*

Operating ranges define the limits between which the functionality of the device is guaranteed.

*Consult Factory for Military Specifications

DC CHARACTERISTICS over operating range unless otherwise specified

HCT Devices*

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL} I _{OH} = -2 mA	2.4		V
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 6 mA	0.5	V
			I _{OL} = 4 mA	0.33	
			I _{OL} = 20 μA	0.1	
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH for all Inputs	2.0		V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW for all Inputs		0.8	V
I _I	Input Leakage Current	V _{IN} = 0 to 5.5 V, V _{CC} = Max.		10	μA
I _O	Output Leakage Current	V _{IN} = 0 to 5.5 V, V _{CC} = Max.		10	μA
I _{CCOP}	Operating Current Supply	f = f _{MAX} , Outputs Open (I _O = 0)		120	mA
I _{SC}	Output Short Circuit Current	V _{CC} = Max., V _O = 0 V	-30	-90	mA

CAPACITANCE

Parameter Symbol	Parameter Description	Test Conditions	Typ.	Units
C _{IN}	Input Capacitance	V _{CC} = 5.00 V, T _A = 25°C V _{IN} = 0 V @ f = 1 MHz	5	pF
C _{OUT}	Output Capacitance		8	

Note: These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

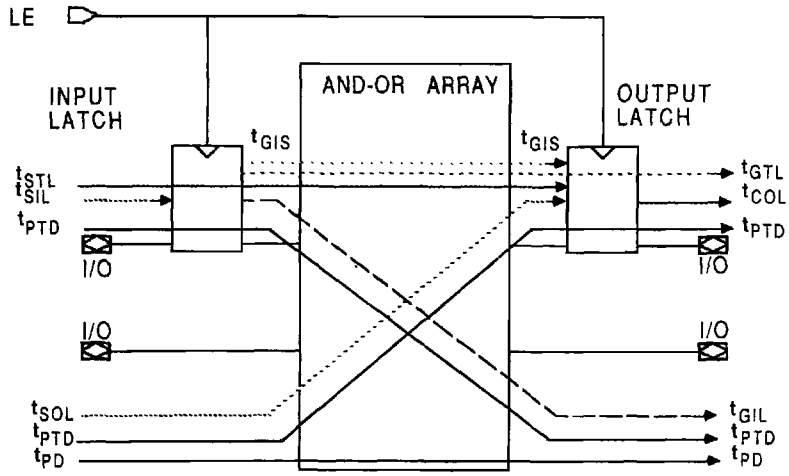
* Consult factory for DC specification on HC Devices.



SWITCHING CHARACTERISTICS over operating range unless otherwise specified All values are determined under the loading of one TTL gate and a capacitance of 50 pF.
All Typical values are determined at $V_{CC} = 5\text{ V}$ and $T_A = 25\text{ C}$.

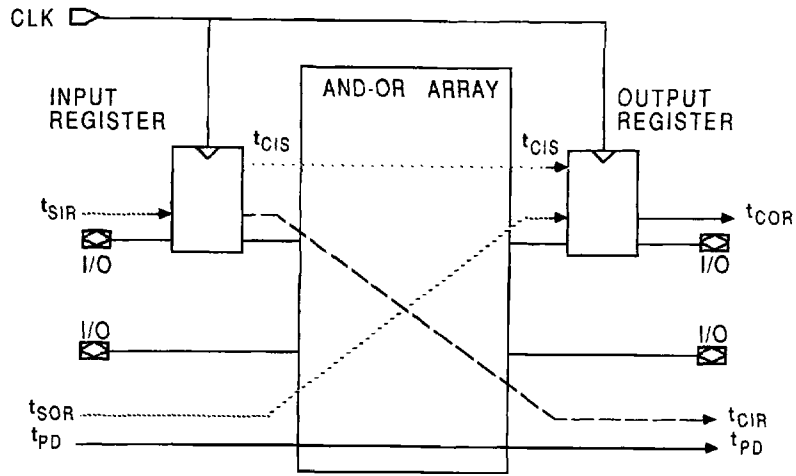
Parameter Number	Parameter Symbol	Parameter Description	-35		-45		Units
			Min.	Max.	Min.	Max.	
REGISTERED OPERATION (Numbers 1 through 12)							
1	t_{PD}	Input or I/O Pin to Combinatorial Output		35		45	ns
Output Register							
2	t_{SOR}	Input or I/O Pin to Output Register Setup	27		34		ns
3	t_{COR}	Output Register Clock to Output		23		32	ns
4	t_{HOR}	Data Hold Time for Output Register	0		0		ns
Input Register							
5	t_{SIR}	I/O Pin to Input Register Setup	6		8		ns
6	t_{CIR}	Register Feedback Clock to Combinatorial Output		45		58	ns
7	t_{HIR}	Data Hold Time for Input Register	3		4		ns
Clocking and Frequency							
8	t_{CIS}	Register Feedback to Output Register/Latch Setup	35		45		ns
9	f_{MAX}	Maximum Frequency $1/(t_{SOR} + t_{COR})$		20		15	MHz
10	f_{MAXI}	Max Internal Frequency $1/t_{CIS}$		28.5		22.5	MHz
11	t_{CWH}	Clock Width HIGH	12		15		
12	t_{CWL}	Clock Width LOW	12		15		
LATCH OPERATION (Numbers 13 through 24)							
13	t_{PD}	Input or I/O Pin to Combinatorial Output		35		45	ns
14	t_{PTD}	Input or I/O Pin to Output via One Transparent Latch		45		55	ns
Output Latch							
15	t_{SOL}	Input or I/O Pin to Output Latch Setup	27		34		ns
16	t_{GOL}	Latch Enable to Transparent Mode Output		23		32	ns
17	t_{HOL}	Data Hold Time for Output Latch	0		0		ns
18	t_{STL}	Input or I/O Pin to Output Latch Setup via Transparent Input Latch	35		45		ns

Parameter Number	Parameter Symbol	Parameter Description	-35		-45		Units
			Min.	Max.	Min.	Max.	
Input Latch							
19	t _{SIL}	I/O Pin to Input Latch Setup	6		8		ns
20	t _{GIL}	Latch Feedback, Latch Enable Transparent Mode to Combinatorial Output		45		58	ns
21	t _{HIL}	Data Hold Time for Input Latch	3		4		ns
Latch Enable							
22	t _{GIS}	Latch Feedback Transparent Mode to Output Register/Latch Setup	35		45		ns
23	t _{GWH}	Latch Enable Width HIGH	12		15		ns
24	t _{GWL}	Latch Enable Width LOW	12		15		ns
RESET/PRESET & OUTPUT ENABLE OPERATION (Numbers 25 through 32)							
25	t _{APO}	Input or I/O Pin to Output Register/Latch RESET/PRESET		.40		55	ns
26	t _{AW}	Async. RESET/PRESET Pulse Width	35		45		ns
27	t _{ARO}	Async. RESET/PRESET to Input Register/Latch Recovery	30		40		ns
28	t _{ARI}	Async. RESET/PRESET to Input Register/Latch Recovery	20		30		
29	t _{PZX}	I/ \overline{O} E Pin to Output Enable		30		40	ns
30	t _{PXZ}	I/ \overline{O} E Pin to Output Disable		30		40	ns
31	t _{EA}	Input or I/O to Output Enable via PT		35		45	ns
32	t _{ER}	Input or I/O to Output Disable via PT		35		45	ns



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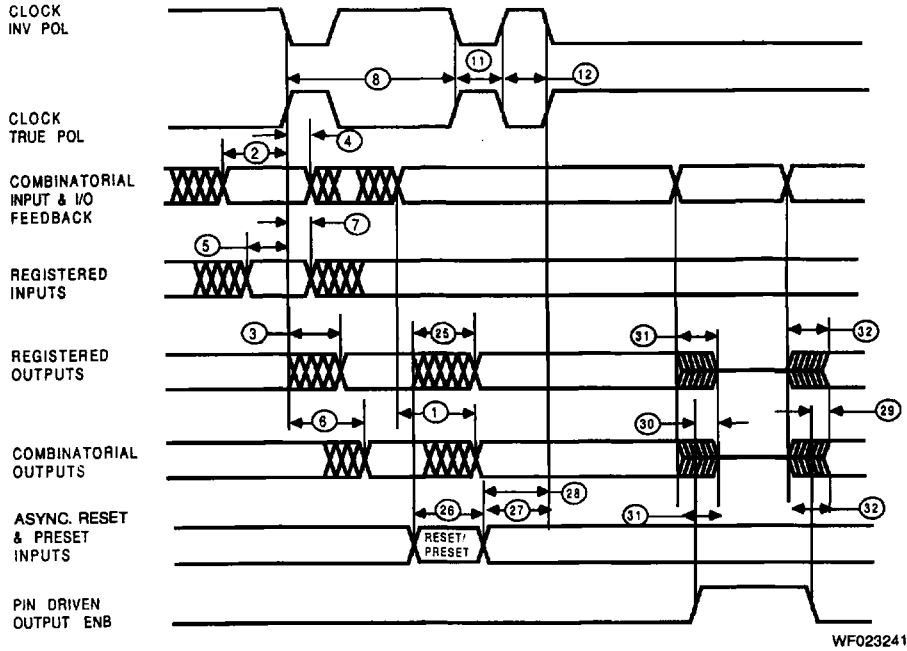
INPUT/OUTPUT SPECS (PIN LE REFERENCE)



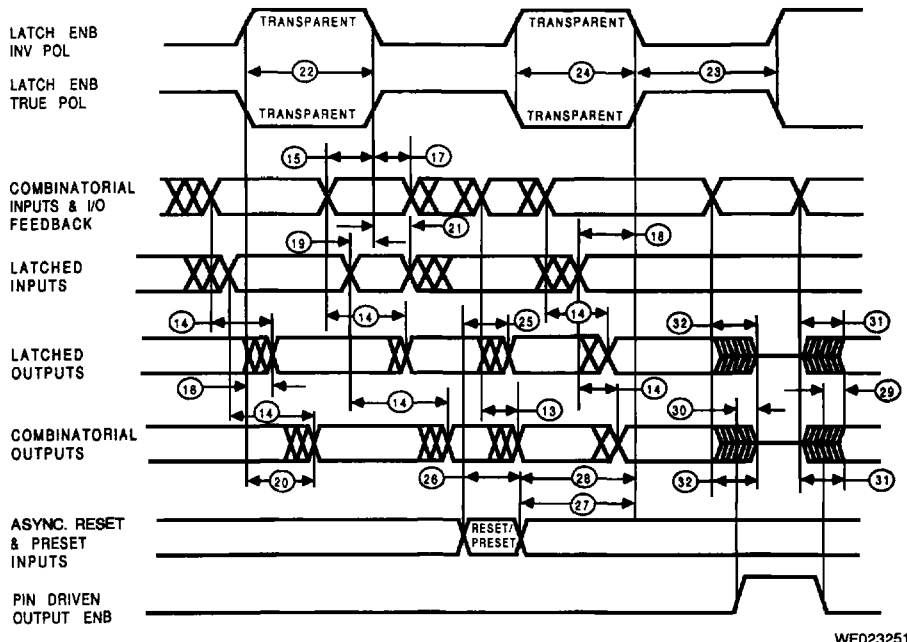
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INPUT/OUTPUT REGISTER SPECS (PIN CLK REFERENCE)

SWITCHING WAVEFORMS

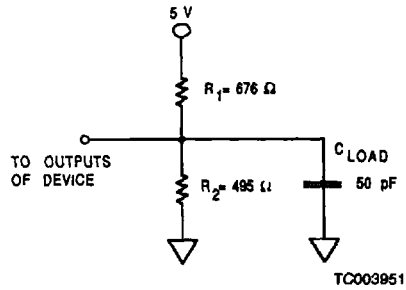


Register



Latch

SWITCHING TEST CIRCUIT



KEY TO SWITCHING WAVEFORMS

WAVEFORM	INPUTS	OUTPUTS
	MUST BE STEADY	WILL BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGING FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGING FROM L TO H
	DON'T CARE; ANY CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE "OFF" STATE

KS000010