# Am6420

## *High Speed 12-Bit Accurate Sample-and-Hold*

**PRELIMINARY DATA**

### DISTINCTIVE CHARACTERISTICS

- Acquisition time 500ns (0.01%)
- Droop rate 20μV/μs
- Aperture delay 2ns
- Aperture uncertainty 200ps
- Gain bandwidth 15MHz
- Slew rate 50V/μs
- Sample to hold offset error 0.2mV
- Internal hold capacitor
- Connect in any standard op-amp configuration
- 12-bit accuracy
- Low output impedance over frequency

### APPLICATIONS

- Precision data acquisition systems
- Data distribution systems
- Auto zeroing system
- Peak detector

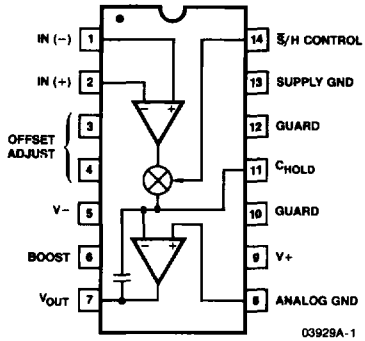
### FUNCTIONAL DESCRIPTION

The Am6420 is a monolithic sample-and-hold circuit consisting of a gated high performance operational amplifier and an internal hold capacitor. The integrating connection of the internal capacitor yields a constant hold-step error, which is internally trimmed to a minimum value.

When the Am6420 is in the sample (or track mode), it behaves as an operational amplifier, and any of the standard op-amp feedback networks may be connected around it to control gain, frequency response, etc. When the device is put into the hold mode, its output remains at its last level before the hold signal. In many systems, the Am6420 may replace both an amplifier and a sample-and-hold.

The Am6420 offers a number of improvements over other monolithic, hybrid, and discrete sample-and-hold circuits. Accuracy is better than 0.01% over the full operating temperature range (0 to 70°C commercial, −55 to +125°C military), while dynamic characteristics include fast acquisition time, low droop rate, and a temperature compensated hold-step. High slew rate and bandwidth allow the device to be used at gains greater than unity, thus eliminating the need for a scaling amplifier.

### BLOCK DIAGRAM




### ORDERING INFORMATION*

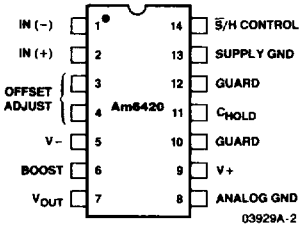
| Part Number | Package Type | Temperature Range |
|---|---|---|
| Am6420DM | Hermetic DIP | −55 to 125°C |
| Am6420LM | Leadless** | −55 to 125°C |
| Am6420DC | Hermetic DIP | 0 to 70°C |
| Am6420LC | Leadless** | 0 to 70°C |
| Am6420XC | Dice | 0 to 70°C |

*Also available with burn-in processing. To order, add suffix B to the part number.

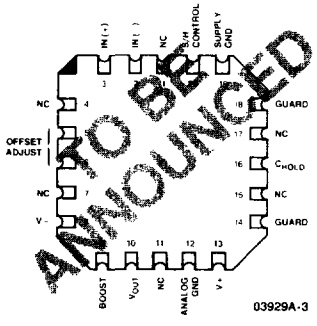
**Availability of Leadless packages will be announced.

### CONNECTION DIAGRAMS – Top Views

**D-14-1**




**Leadless Chip-Pak**
**L-20-1**



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## MAXIMUM RATINGS

| | |
|---|---|
| Supply Voltage, V+ to Supply GND | −0.5 to +16.5V |
| V− to Supply GND | +0.5 to −16.5V |
| Max Differential V+ to V− | 33V |
| Differential Input Voltage | 25V |
| $\overline{S}$/H Control Voltage to Ground | −1 to +6V |
| Output Current | Short Circuit Protected |
| Operating Temperature Am6420DC | 0 to 70°C |
| Storage Temperature | −65 to +150°C |
| Lead Temperature (Soldering 60 Seconds) | 300°C |
| Power Dissipation | 700mW |





## ELECTRICAL CHARACTERISTICS V+ = +15V, V− = −15V, $T_A$ = 25°C, unless otherwise noted.

| Parameters | Description | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **GAIN AND ACCURACY** | | | | | | |
| $A_E$ | Voltage Gain Error | $A_V$ = +1 | | 0.005 | | % |
| A | Gain Non-Linearity | | | 0.005 | | % |
| **INPUT CHARACTERISTICS** | | | | | | |
| $R_{IN}$ | Input Resistance | | | 5 | | MΩ |
| $C_{IN}$ | Input Capacitance | | | 5 | | pF |
| $I_{OS}$ | Input Offset Voltage | 5°C (On-Chip Trimmed) | | ±0.2 | | mV |
| $\Delta V_{OS}/\Delta t$ | Input Offset T | | | 5 | | μV/°C |
| $I_B$ | Bias Curre | $T_A$=25°C | | 80 | | nA |
| $I_{BM}$ | B | $T_{MIN}$ to $T_{MAX}$ | | 150 | | nA |
| $V_{CM}$ | t V ge R e | $V_S$ = ±15V | | ±11 | | V |
| **TRANSFER CHAR TERISTICS** | | | | | | |
| GBW | Gain andwidth Product | | | 13 | | MHz |
| BW | Full Power Bandwidth | $10V_{p-p}$ | | 1.2 | | MHz |
| $\Delta V/\Delta t$ | Slew Rate | $10V_{p-p}$, $C_H$ = 50pF | | 50 | | V/μs |
| $C_{MR}$ | Common Mode Rejection Rate | $V_{CM}$ = 10V, 1kHz | | 80 | | dB |
| **SAMPLE/HOLD CHARACTERISTICS:** ($T_A$ = 25°C) | | | | | | |
| $t_{ACQ}$ | Acquisition Time | | | 500 | | ns |
| $t_{AD}$ | Aperture Delay Time | | | 2 | | ns |
| $t_{AU}$ | Aperture Uncertainty | | | 200 | | ps |
| $t_{HS}$ | Hold Settling Time | 0.01% | | 30 | | ns |
| | Droop Rate 25°C | | | 20 | | μV/μs |
| | Sample-to-Hold Offset Error, 25°C | | | 0.2 | | mV |
| **OUTPUT CHARACTERISTICS** | | | | | | |
| | Output Voltage | | | +11 | | V |
| | | | | −6 | | |
| | Output Current | Can Be Externally Boosted | | +10 | | mA |
| | | | | −2 | | |
| | Output Resistance | | | 1 | | Ω |
| | Max Load Capacitance | | | 50 | | pF |
| | Supply Current | | | +20 | | mA |
| | | | | −15 | | |

## PIN DESCRIPTION

| | |
|---|---|
| **IN(−)** | The inverting input of the input amplifier. |
| **IN(+)** | The noninverting input of the input amplifier. |
| **Offset Adjust** | The offset adjust terminals of the input amplifier. A small differential current into these pins can be used to trim the $V_{OS}$ of the input amp. |
| **$\overline{S}$/H Control** | This pin controls the internal switch to make the output either track the input ($\overline{S}$/H low) or hold the last value ($\overline{S}$/H high). |
| **$V_{OUT}$** | The output of the on-chip buffer amplifier. |
| **$C_{HOLD}$** | An external hold capacitor can be connected from $V_{OUT}$ to this pin to improve droop rate. The $C_{HOLD}$ pin should be surrounded by a guard ring connected to the guard pins. |
| **Guard** | These pins should be connected to the guard ring around the $C_{HOLD}$ pin to prevent leakage. DO NOT connect guard to ground or to $V_{OUT}$ as the guard voltage is internally generated. |
| **Boost** | An external resistor from this pin to the negative power supply can be used to increase the current sink capability of the output buffer. |
| **Analog Ground** | The output voltage is referenced to this pin; care should be taken to keep the ground free of noise. |
| **Supply Ground** | This ground pin should be connected to the system ground. |
| **V+** | The positive power supply pin. |
| **V−** | The negative power supply pin. |

## APPLICATIONS INFORMATION

The Am6420 may be connected in an op-amp configuration including voltage followers, inverting and noninverting amplifiers, and active filters. Examples of these connections are shown in Figures 1 through 4. These circuits are intended as examples only and may be changed to meet the exact needs of the system.

The Am6420 input offset voltage is internally trimmed to less than ±0.2mV; in most applications, this is an acceptable error and the offset adjust pins 3 and 4 should be left open. If better input offset is required, it can be adjusted using the circuit shown in Figure 5. With both input grounded, connect a square wave to the $\overline{S}$/H control and adjust the potentiometer for 0 volts at the output in hold mode.

The output sink capability of the Am6420 is nominally −2mA; this can be increased by connecting an external resistor from the boost pin (pin 6) to the negative power supply (pin 5). Boost current is calculated by:

$$I_{boost} = 1.2/R_{boost}$$

Total output sink current should not be more than 10mA, therefore boost current should be limited to 8mA.

The internal hold capacitor (50pF) is optimized for fast acquisition and minimum hold-step error. However, if improved droop rate is desired, an external hold capacitor can be connected from $V_{OUT}$ (pin 7) to $C_{HOLD}$ (pin 11). Acquisition time and droop rate are directly and indirectly proportional, respectively, to hold capacitance. For example, if an external 50pF capacitor were added, the total hold capacitance would be doubled. This would double the acquisition time and decrease the droop rate by 1/2. To maintain stability, a capacitor must be added from $C_{HOLD}$ (pin 11) to ground; the value of this capacitor should be approximately 1/2 of the value of the external hold capacitor (Figure 6), and should be a low leakage type, such as a mica. The hold-step has been trimmed for the internal capacitor; when an external capacitor is used, offset adjustment may be needed to correct the hold-step.

### LAYOUT CONSIDERATIONS

In order to take advantage of full accuracy of the Am6420, care should be taken to avoid system errors. One of the most common causes of errors in data acquisition systems is improper grounding. High frequency digital circuits should not be connected to the same ground trace as high accuracy analog circuits; separate ground paths should be provided for analog and digital signals and connected together at only one point in the system. The Am6420 provides two ground pins; all internal circuit grounds except the output amplifiers are connected to the power supply ground. The output amplifier is connected to the analog ground, which should also be used for output return. Recommended ground connections are shown in Figure 7.

To keep leakage current to a minimum and improve droop rate, the $C_{HOLD}$ pin should be surrounded by a guard ring (Figure 8). This ring should be connected to pins 10 and 12 of the Am6420 and *must not be connected to ground or $V_{OUT}$* since the guard voltage is internally generated and connected to the guard pins.

The Am6420 provides excellent power rejection, however, system performance may be enhanced by proper power supply bypassing. A 0.1μF capacitor and a 10μF tantalum capacitor should be connected from the power supply pins to the power supply ground, as close to the pins as possible.

### GLOSSARY OF TERMS

**Acquisition Time:** The time required for the hold capacitor to be charged to a full-scale value after the sample command is given.

**Aperture Delay Time:** The time elapsed between the sample command and the actual opening of the switch.

**Aperture Uncertainty:** The variation in aperture delay time from sample-to-sample.

**Droop Rate:** The rate at which the output voltage changes while in the hold mode. Droop is caused by the capacitor being discharged through the buffer amplifier's input circuit.

**Hold Settling Time:** The time required for the buffer output to settle within the specified accuracy band after the switch is opened.

**Sample-to-Hold Offset Error:** The difference in output voltage between the time-to-hold command is given and the time the output settles to its final value. It is caused by charge injection from the switch to the capacitor during the opening of the switch.

**Figure 1. Am6420 in Unity Gain Sample-and-Hold Circuit**

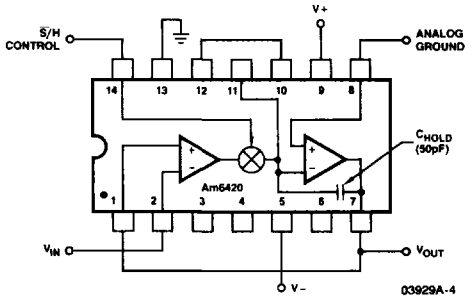


**Figure 2. Am6420 Connected as a Noninverting Amplifier**

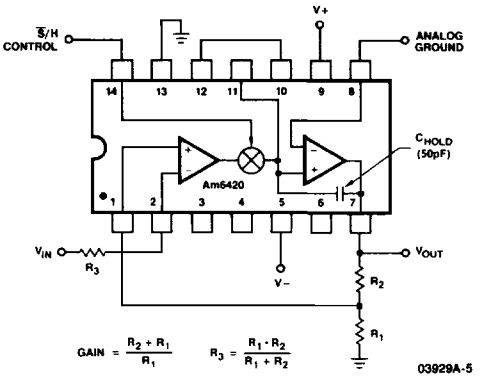


**Figure 3. Am6420 in an Inverting Amplifier Configuration**

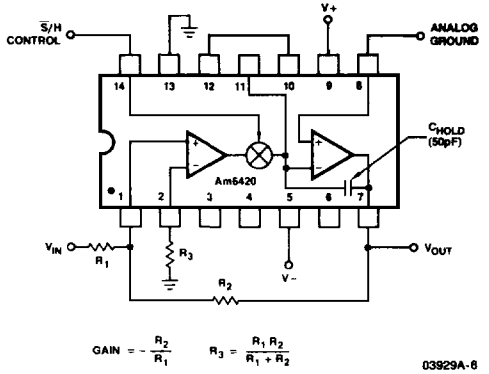


**Figure 4. Am6420 in an Active Filter Circuit**

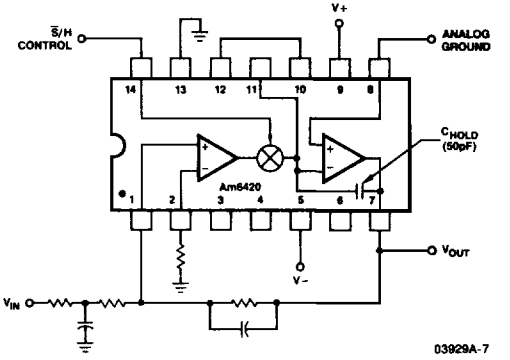


**Figure 5. Am6420 $V_{OS}$ Adjustment Circuit**

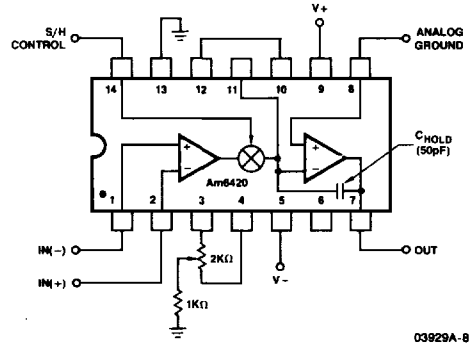


**Figure 6. Am6420 with External $C_{HOLD}$**

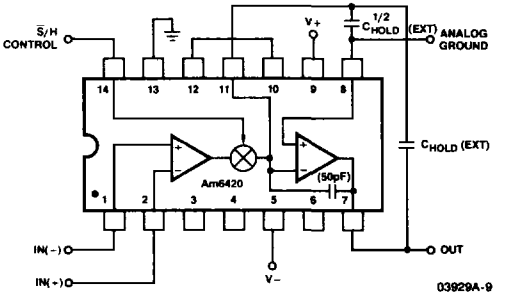


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Figure 7. Data Acquisition System Grounding

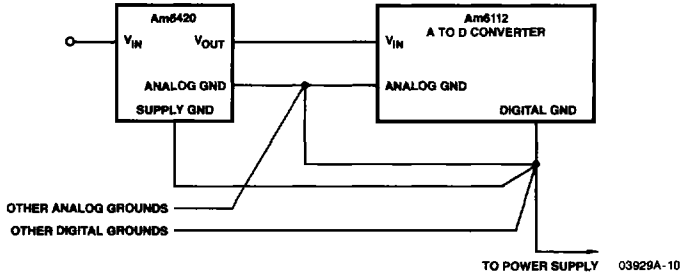


Figure 8. Pad Layout – Top View