M02011

CMOS Transimpedance Amplifier with AGC for Fiber Optic Networks up to 622 Mbps

The M02011 is a CMOS transimpedance amplifier with AGC. The AGC gives a wide dynamic range of 40 dB. The high transimpedance gain of 66 kΩ ensures good sensitivity.

For optimum system performance, the M02011 die should be mounted with a GaAs or InGaAs PIN photodetector inside a lensed TO-Can or other optical sub-assembly.

The M02011 can either bias the PIN diode from the internal regulator, or use an externally biased PIN diode.

A replica of the average photodiode current is available at the MON pad for photo-alignment and 'Loss of Signal' monitoring.

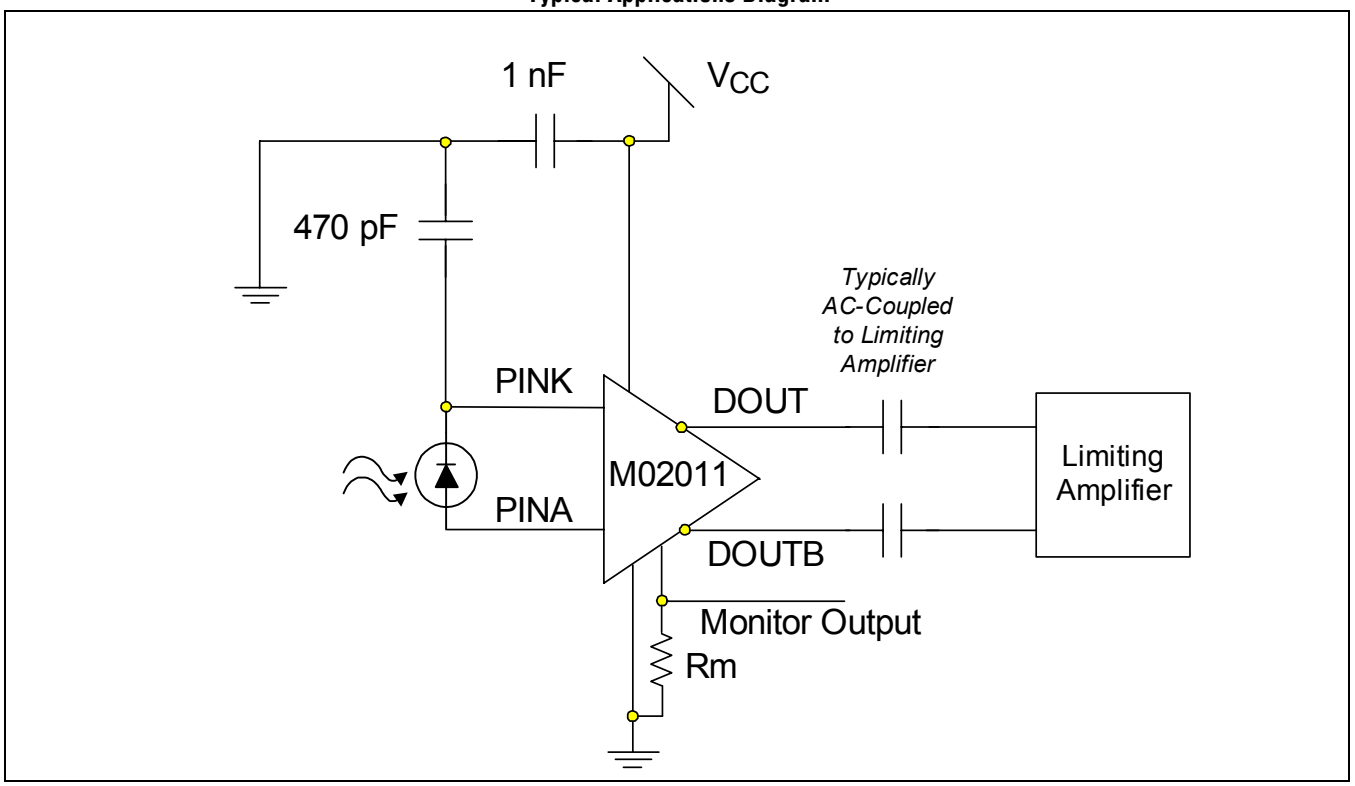
Applications

- APON
- BPON
- ATM/SONET

Features

- Typical -34 dBm sensitivity, +6 dBm saturation at 622 Mb/s when used with 0.9 A/W InGaAs PIN. (Cpd ≤ 0.5 pF, BER 10^{-10})
- Typical differential transimpedance: 65 kΩ
- Fabricated in standard CMOS
- Differential output
- Standard +3.3 Volt supply
- Available in die form only
- Monitor output
- AGC provides dynamic range of 40 dB
- Internal or external bias for photodiode
- PIN or APD sensor
- Same pad layout and die size as M02013/14/15/16

Typical Applications Diagram



Ordering Information

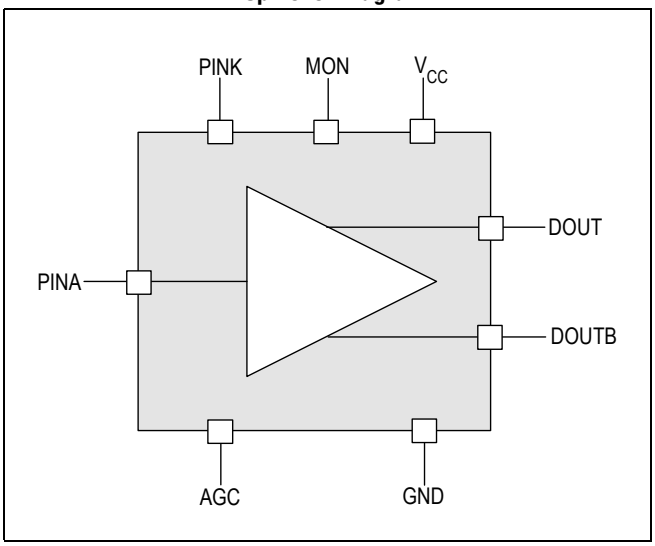
Part Number	Package	Operating Temperature
M02011-XX*	Waffle Pack	–40 °C to 95 °C
M02011-XX*	Expanded whole wafer on a ring	–40 °C to 95 °C

*For full ordering number please contact sales

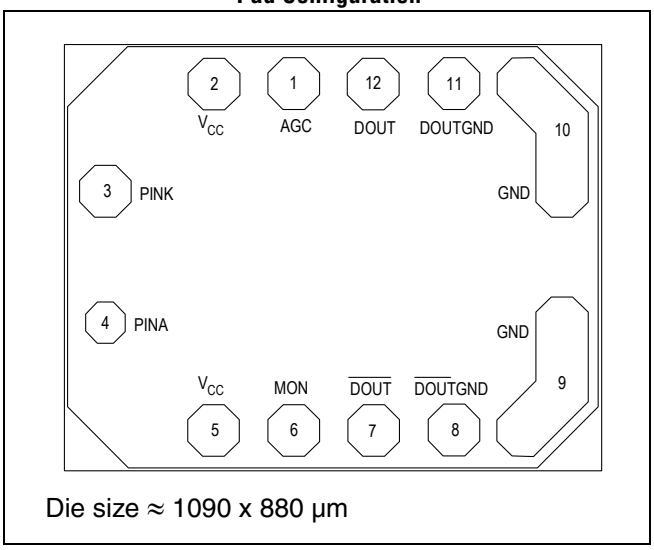
Revision History

Revision	Level	Date	Description
C	Released	April 2007	Production release. Increased max operating temperature, updated specifications based on full device characterization and included information on assembly, I_{MON} and using the device with externally biased detectors in the Applications Information section.

Top Level Diagram



Pad Configuration



Die size ≈ 1090 x 880 µm

1.0 Product Specification

1.1 Absolute Maximum Ratings

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Table 1-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{CC}	Power supply (V_{CC}-GND)	-0.4 to +4	V
T_A	Operating ambient	-40 to +95	°C
T_{STG}	Storage temperature	-65 to +150	°C
I_{IN}	PINA Input current	8 (1)	mA_{PP}
V_{PINA}, V_{PINK}, V_{Dout}, V_{DoutB}, V_{AGC}, V_{MON}	Maximum input voltage at PINA, PINK, Dout, DoutB, AGC and MON	-0.4V to Vcc + 0.4V	V
I_{PINK}	Maximum average current sourced out of PINK	10	mA
I_{Dout}, I_{DoutB}	Maximum average current sourced out of Dout and DoutB	10	mA

NOTES:
1. Equivalent to 4.9 mA average current with an extinction ratio of 10 dB.

1.2 Recommended Operating Conditions

Table 1-2. Recommended Operating Conditions

Symbol	Parameter	Rating	Units
V_{CC}	Power supply (V_{CC}-GND)	3.3 ± 10%	V
C_{PD}	Max. Photodiode capacitance (V_r = 1.8 V), for 622 Mbps data rate	1.0	pF
T_A	Operating ambient temperature	-40 to +95	°C

1.3 DC Characteristics

Table 1-3. DC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units
V_B	Photodiode bias voltage (PINK - PINA)	1.7	2.0	2.2	V
V_{CM}	Common mode output voltage	0.7	1	1.3	V
I_{CC}	Supply current (no loads)	20	28	35	mA
R_{LOAD}	Recommended differential output loading	85	100 (1)	–	Ω

NOTE:
1. 100Ω is the load presented by the limiting amplifier.

1.4 AC Characteristics

Table 1-4. AC Characteristics

Symbol	Parameter	Condition	Min.	Typ.(1)	Max.	Units
R_{OUT}	Output impedance (single ended)		30	50	70	Ω
LFC	Low frequency cutoff (2)		–	13	17	kHz
V_D	Differential output voltage	100Ω differential load	–	250	450	mV
DCD	Duty cycle distortion (3)	622 Mbps	–	–	80	ps
DJ	Deterministic jitter (includes DCD) (3)	622 Mbps, 2^{23} - 1 PRBS	–	–	120	ps_{PP}
PDJ	Pattern Dependant Jitter (at crossing point), with no DCD	622 Mbps, 2^{23} - 1 PRBS	–	–	55	ps_{PP}
In, rms	Total input RMS noise	DC to 467 MHz (Bessel Filter), Cin = 0.5 pF	–	50	60	nA
	Total input RMS noise	DC to 467 MHz (Bessel Filter), Cin = 1 pF	–	56	70	nA
PIN_mean_min	Optical Sensitivity (4)		-33	-34	–	dBm
Imon_off	Monitor Output Offset (5)	V_{MON} = 0 to 2V	–	–	1.3	µA
Imon_ratio	Monitor Output Gain Ratio (5)	V_{MON} = 0 to 2V	–	0.7	–	–
Imon_error	Monitor Output Accuracy (3, 5)	V_{MON} = 0 to 2V	–	–	±2	dB

NOTES:
1. Die designed to operate over an ambient temperature range of -40°C to +85°C, T_A and V_{CC} range from 3.0 - 3.6V. Typical values are tested at T_A = 25° C and V_{CC} = 3.3V.
2. Input -33 dBm, Extinction Ratio = 10, Temp = 25°C.
3. Input current < 1 mA average.
4. BER 10^{-10}, PD capacitance = 0.5 pF, Responsivity 0.9 A/W, Extinction Ratio = 10, Temp = 25°C.
5. Offset and slope adjustment necessary to achieve rated accuracy.

1.5 Dynamic Characteristics

Table 1-5. Dynamic Characteristics

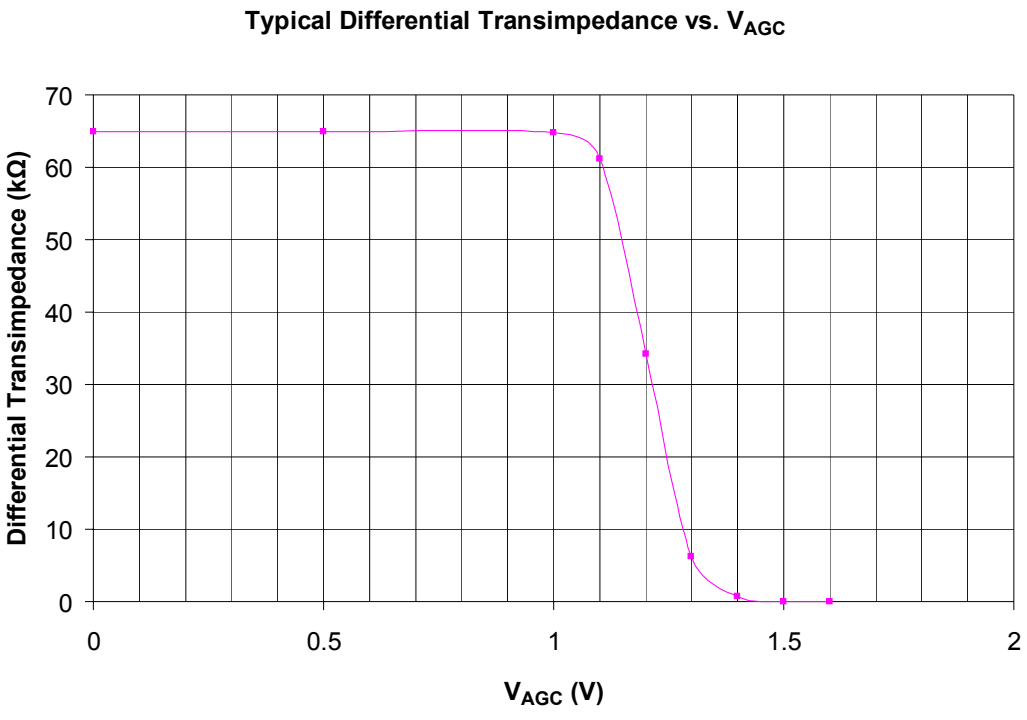
Symbol	Parameter	Min.	Typ.	Max.	Units
G	Transimpedance - Single ended - Differential	 26.5 53	 32.5 65	 38 76	kΩ
BW	Bandwidth to -3 dB point @ -33 dBm, 0.9A/W, 0.5 pF PD	450	600	–	MHz
	Bandwidth to -3 dB point @ -33 dBm, 0.9A/W, 1 pF PD	–	460	–	
RC	AGC loop time constant	–	2	–	µs
I_{AGC}	AGC threshold	–	5	–	$µA_{PP}$
I_{OVL}	Maximum functional input current	3.6 (1)	–	–	mA
PSRR	Power supply rejection, f < 1 MHz	–	22	–	dB

NOTES:
1. Equivalent to +3.4 dBm input optical power at Extinction Ratio = 10, Responsivity = 1.0 A/W.

1.6 Typical Performance

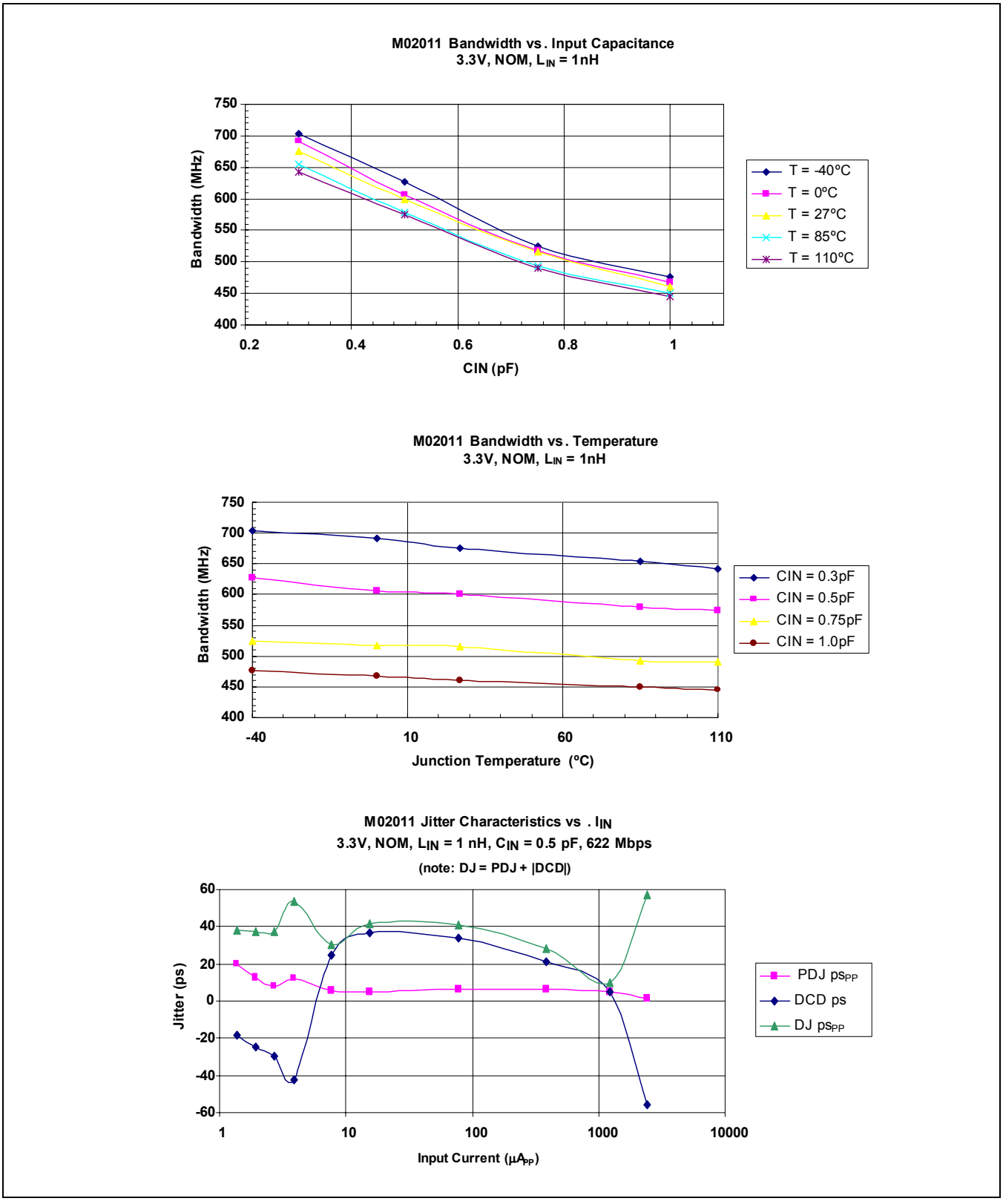
V_{CC} = 3.3V, Temperature = 25°C, L_{IN} = 1 nH, unless otherwise stated.

Figure 1-1. Typical Performance Diagrams 1 of 3



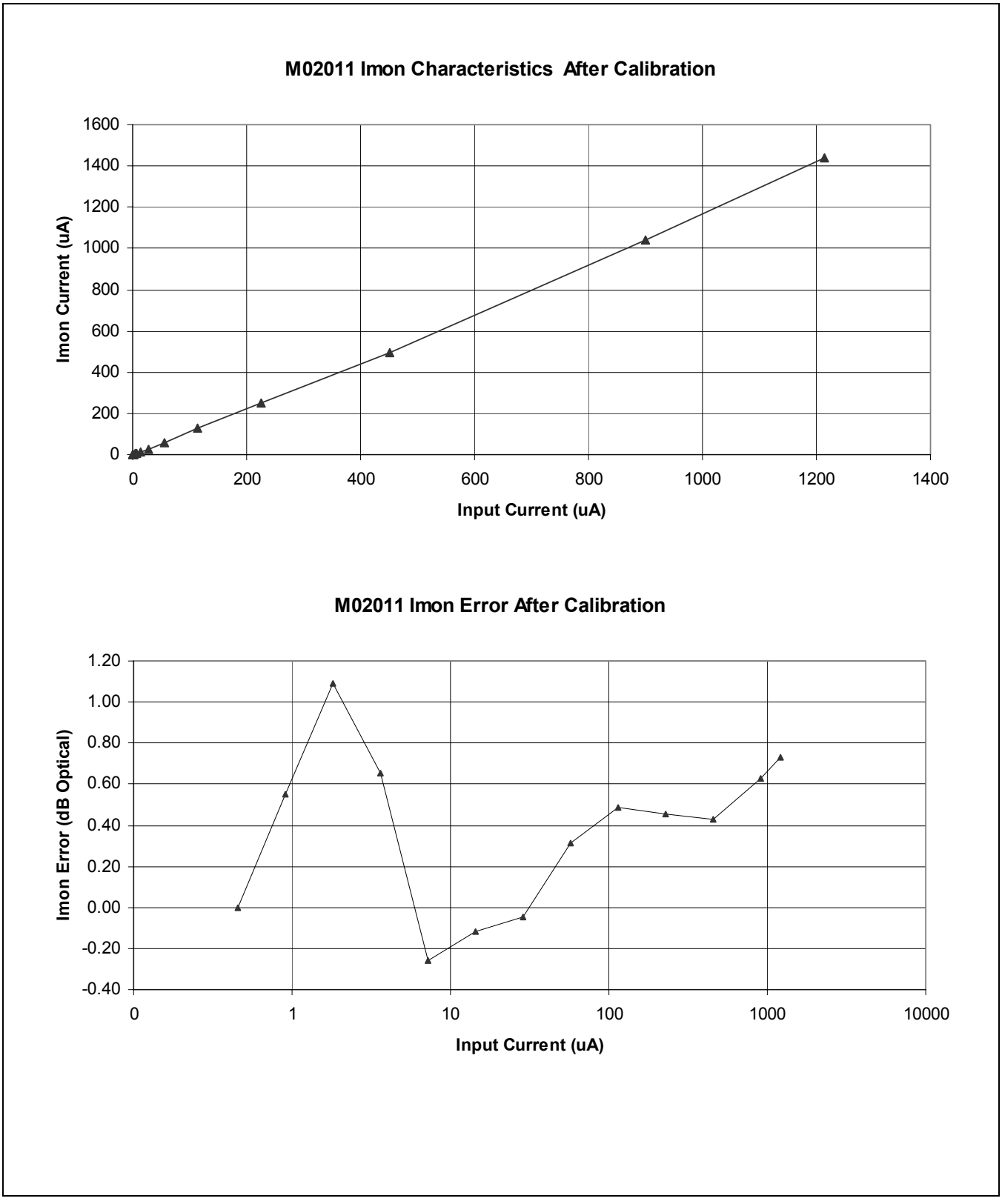
V_{CC} = 3.3V, Temperature = 25°C, L_{IN} = 1 nH, unless otherwise stated.

Figure 1-2. Typical Performance Diagrams 2 of 3



V_{CC} = 3.3V, Temperature = 25°C, L_{IN} = 1 nH, unless otherwise stated.

Figure 1-3. Typical Performance Diagrams 3 of 3



2.0 Pin Definitions

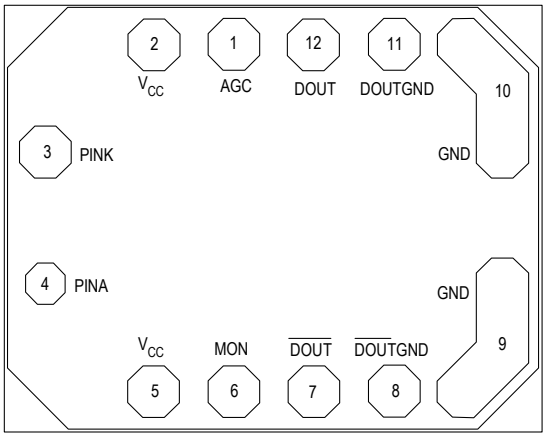
Table 2-1. Pad Description

Die Pad No	Name	Function
1	AGC	Monitor or force AGC voltage
2	V_{CC}	Power pin. Connect to most positive supply
3	PINK	Common PIN input. Connect photo diode cathode here and a 470 pF capacitor to Gnd (1)
4	PINA	Active PIN input. Connect to photo diode anode
5	V_{CC}	Power pin. Connect to most positive supply (only one V_{CC} pad needs to be connected)
6	MON	Analog current source output. Current matched to average photodiode current
7	DOUT	Differential data output (goes low as light increases)
8	$\overline{\text{DOUT}}$GND	Ground return for $\overline{\text{DOUT}}$ pad (2)
9	GND	Ground pin. Connect to the most negative supply (2)
10	GND	Ground pin. Connect to the most negative supply (2)
11	DOUTGND	Ground return for DOUT pad (2)
12	DOUT	Differential data output (goes high as light increases)
NA	Backside	Backside. Connect to the lowest potential, usually ground

Notes:

1. Alternatively the photodiode cathode may be connected to a decoupled positive supply, e.g. V_{CC}.
2. All ground pads are common on the die. Only one ground pad needs to be connected to the TO-Can ground. However, connecting more than one ground pad to the TO-Can ground, particularly those across the die from each other can improve performance in noisy environments.

Figure 2-1. Bare Die Layout



3.0 Functional Description

3.1 Overview

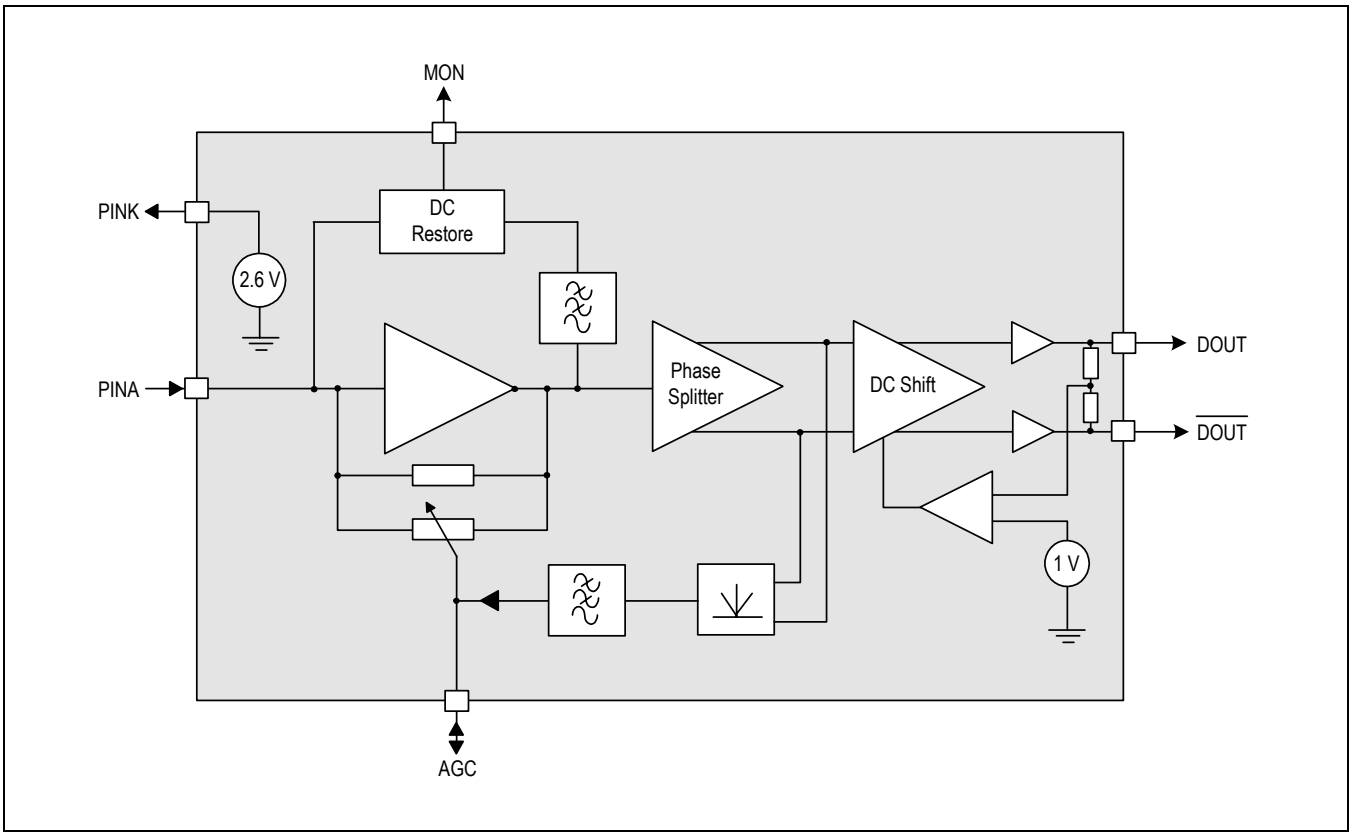
The M02011 is a CMOS transimpedance amplifier with AGC. The AGC gives a wide dynamic range of 40 dB. The high transimpedance gain of 66 kΩ ensures good sensitivity.

For optimum system performance, the M02011 die should be mounted with a GaAs or InGaAs PIN photodetector inside a lensed TO-Can or other optical sub-assembly.

The M02011 can either bias the PIN diode from the internal regulator, or use an externally biased PIN diode.

A replica of the average photodiode current is available at the MON pad for photo-alignment and 'Loss of Signal' (LOS) monitoring.

Figure 3-1. M02011 Block Diagram



3.2 General Description

3.2.1 TIA (Transimpedance Amplifier)

The transimpedance amplifier consists of a high gain single-ended CMOS amplifier (TIA), with a feedback resistor. The feedback creates a virtual earth low impedance at the input and virtually all of the input current passes through the feedback resistor, defining the voltage at the output. Advanced CMOS design techniques are employed to maintain the stability of this stage across all input conditions.

An on-chip low dropout linear regulator has been incorporated into the design to give excellent noise rejection up to several MHz. Higher frequency power supply noise is removed by the external 470 pF decoupling capacitor connected to PINK.

The circuit is designed for PIN photodiodes in the “grounded cathode” configuration, with the anode connected to the input of the TIA and the cathode connected to AC ground, such as the provided PINK terminal. Reverse DC bias is applied to reduce the photodiode capacitance. Avalanche photodiodes can be connected externally to a higher voltage.

3.2.2 AGC

The M02011 has been designed to operate over the input range of +6 dBm to -34 dBm. This represents a ratio of 1:10000 whereas the acceptable dynamic range of the output is only 1:30 which implies a compression of 333:1 in the transimpedance. The design uses a MOS transistor operating in the triode region as a “voltage controlled resistor” to achieve the transimpedance variation.

Another feature of the AGC is that it only operates on signals greater than -26 dBm (@0.9 A/W). This knee in the gain response is important when setting “signal detect” functions in the following post amplifier. It also aids in active photodiode alignment.

The AGC pad allows the AGC to be disabled during photodiode alignment by grounding the pad through a low impedance. The AGC control voltage can be monitored during normal operation at this pad by a high impedance (>10 MΩ) circuit.

3.2.3 Output Stage

The signal from the TIA enters a phase splitter followed by a DC-shift stage and a pair of voltage follower outputs. These are designed to drive a differential (100 Ω) load. They are stable for driving capacitive loads, such as interstage filters. Each output has its own GND pad, all four GND pads on the chip should be connected for proper operation. Since the M02011 exhibits rapid roll-off (3 pole), simple external filtering is sufficient.

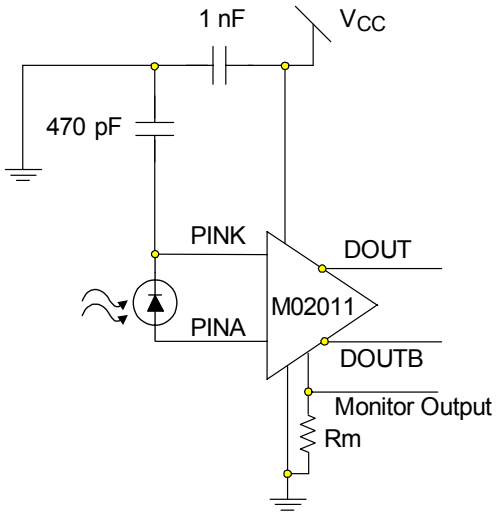
3.2.4 Monitor O/P

High impedance output sources a replica average photodiode current for monitoring purposes. This output is compatible with the DDMI Receive Power Specification (SFP-8472) and Mindspeed’s range of DDMI controllers. Ensure that the voltage on V_{MON} is in the range of 0 to 2V. Refer to Figure 4-1.

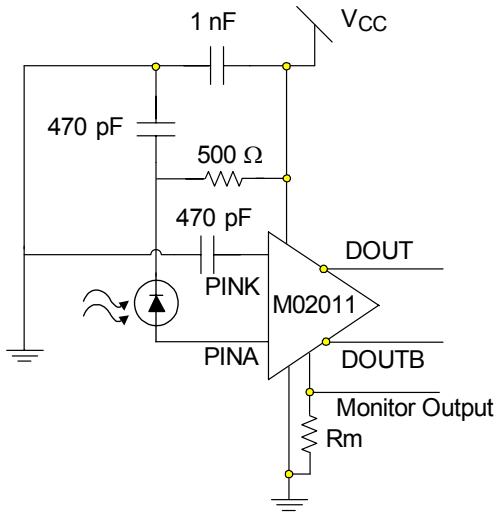
4.0 Applications Information

4.1 Recommended Pin Diode Connections

Figure 4-1. Suggested PIN Diode Connection Methods



Recommended Circuit



Alternative Circuit - Cathode Connected to V_{CC}

Note:

Selection of Rm depends on the maximum input current as detailed in Table 4-1.

4.2 Monitor Calibration

To achieve the best monitor accuracy, both the slope and calibrated offset should be used. The offset calibration is achieved by measuring the dark current from the MON output. The calibrated monitor value is usually determined by y = mx + b or:

$I_{MON\_CALIBRATED}$ = (Slope * $I_{MON\_READING}$) + I_{MON_OFFSET}

Where Slope = 1/Imon_ratio (Table 1-4) = 1/0.7 = 1.43 and

I_{MON_OFFSET} = $I_{INPUT@CAL}$ - ($I_{MON\_READING@CAL}$ * Slope)

4.3 Selecting the Monitor Resistor

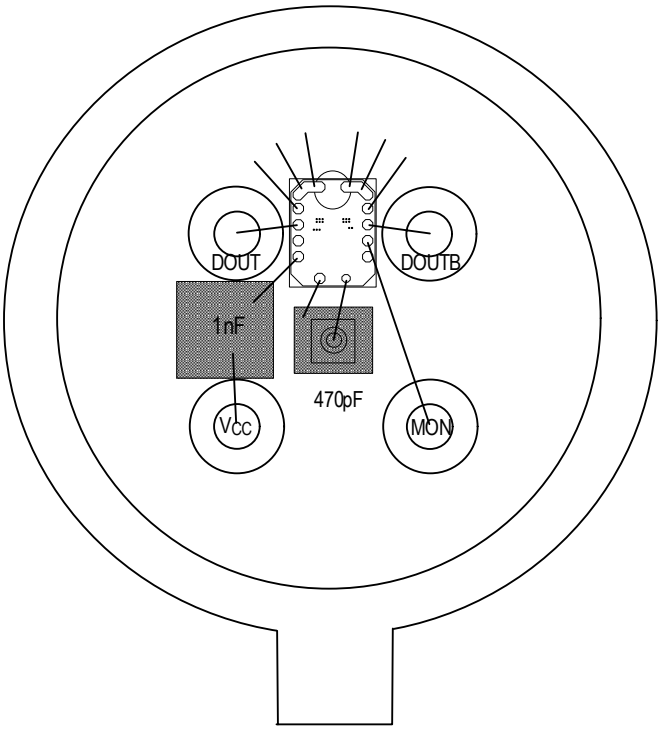
As described earlier the high impedance monitor output sources a replica average photodiode current for monitoring purposes. If detected by converting the current to a voltage through an external resistor (Figure 4-1), ensure that the voltage on V_{MON} is in the range of 0 to 2V. The table below provides suggested values for the monitor resistor.

Table 4-1. Selection of Rm for Maximum Input Current

I_{IN} Max (mA)	Optical Power (dBm)	Rm (Ω)
4	+6	500
2	+3	1000
1	0	2000
0.5	-3	4000

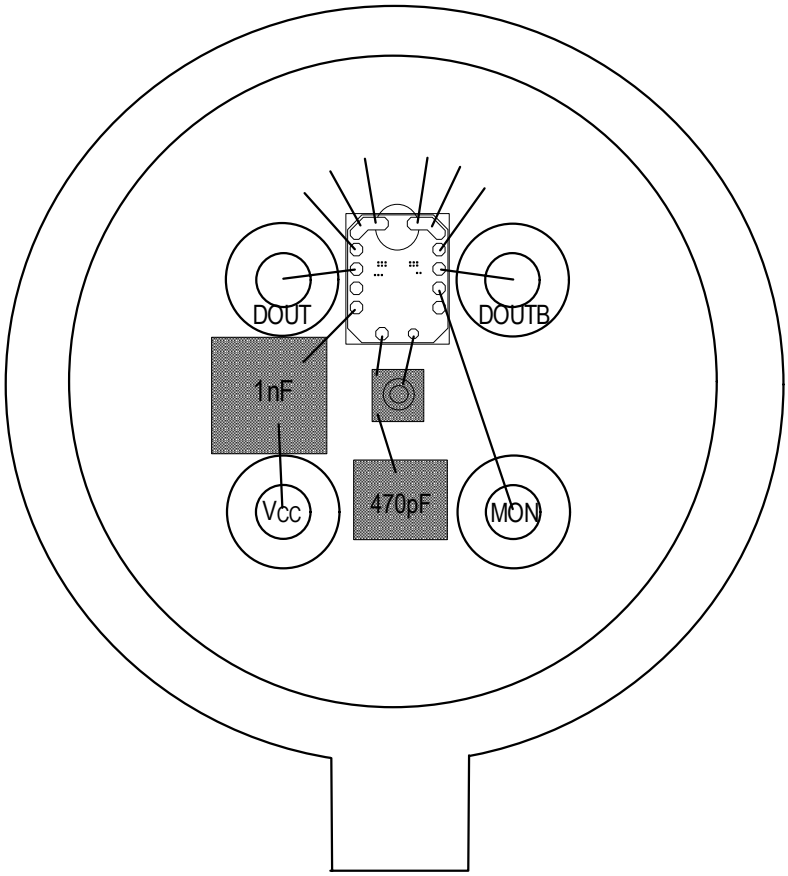
4.4 TO-Can Layout

Figure 4-2. Typical Layout Diagram with Photodiode Mounted on PINK Capacitor (5 pin TOCAN)



Notes:
Typical application inside of a five lead TO-Can.
Only one of the V_{CC} pads and all of the GND pads need to be connected. The backside must be connected to the lowest potential, usually ground, with conductive epoxy or a similar die attach material. If a monitor output is not required then a four lead TO-Can may be used.

Figure 4-3. Typical Layout Diagram with Photodiode Mounted on TOCAN base (5 pin TOCAN)



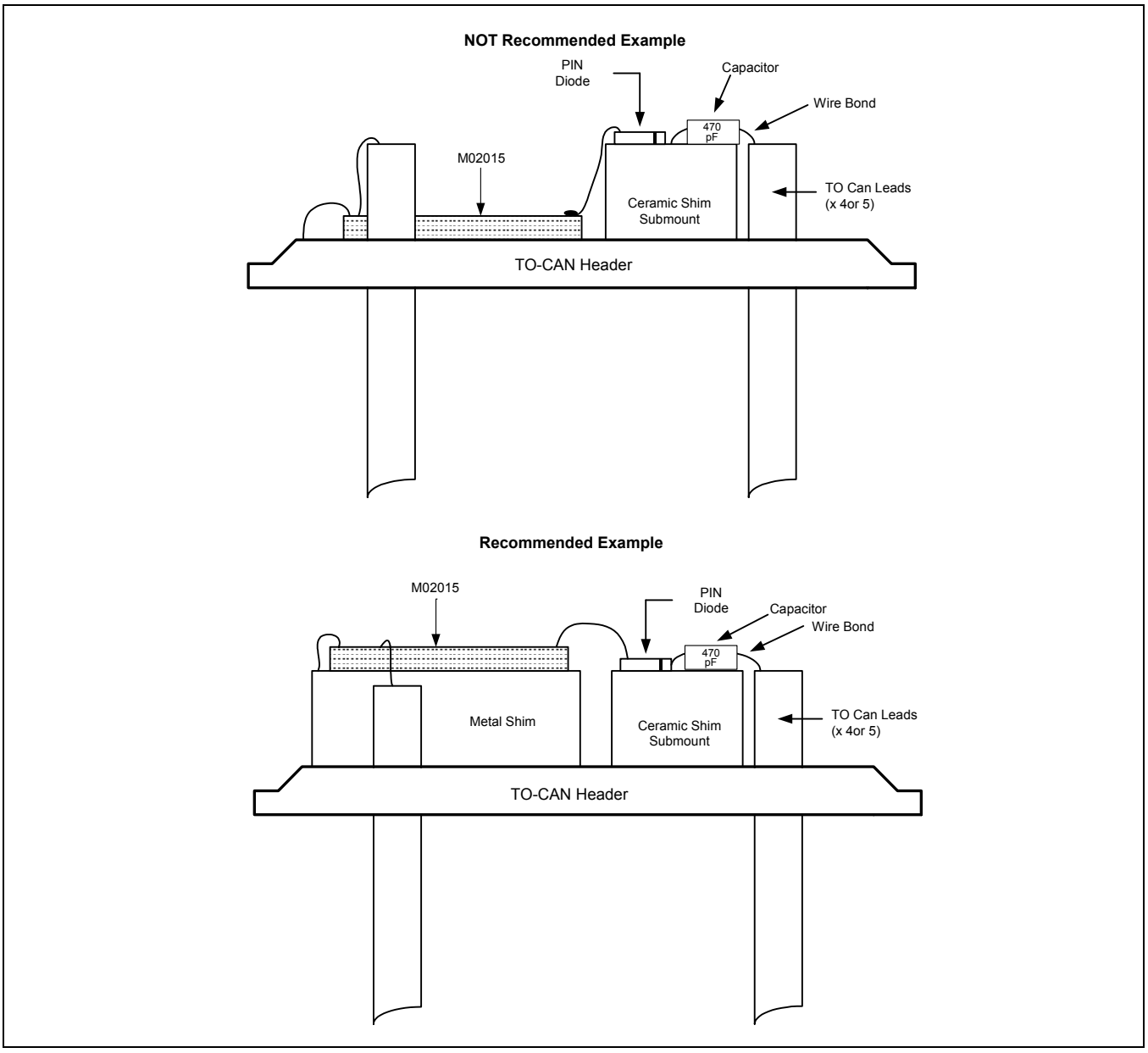
Notes:
Typical application inside of a five lead TO-Can.
Only one of the V_{CC} pads and all of the GND pads need to be connected. The backside must be connected to the lowest potential, usually ground, with conductive epoxy or a similar die attach material. If a monitor output is not required then a four lead TO-Can may be used.

4.5 Treatment of PINK

PINK requires bypassing to ground with a capacitor when powering a photo diode. If PINK is not used to bias the photo diode, then it is not necessary to bypass an unused PINK.

4.6 TO-Can Assembly Recommendations

Figure 4-4. TO-Can Assembly Diagram



4.6.1 Assembly

The M02011 is designed to work with a wirebond inductance of 1 nH ± 0.25 nH. Many existing TO-Can configurations will not allow wirebond lengths that short, since the PIN diode submount and the TIA die are more than 1 mm away in the vertical direction, due to the need to have the PIN diode in the correct focal plane. This can be remedied by raising up the TIA die with a conductive metal shim. This will effectively reduce the bond wire length. Refer to Figure 4-4 above for details.

Mindspeed recommends ball bonding with a 1 mil (25.4 µm) gold wire. For performance reasons the PINA pad is smaller than the others and also has less via material connected to it. It therefore requires more care in setting of the bonding parameters. **For the same reason PINA has no ESD protection.**

In addition, please refer to the Mindspeed Product Bulletin (document number 0201X-PBD-002). Care must be taken when selecting chip capacitors, since they must have good low ESR characteristics up to 1.0 GHz. It is also important that the termination materials of the capacitor be compatible with the attach method used.

For example, Tin/Lead (Pb/Sn) solder finish capacitors are incompatible with silver-filled epoxies. Palladium/Silver (Pd/Ag) terminations are compatible with silver filled epoxies. Solder can be used only if the substrate thick-film inks are compatible with Pb/Sn solders.

4.6.2 Recommended Assembly Procedures

For ESD protection the following steps are recommended for TO-Can assembly:

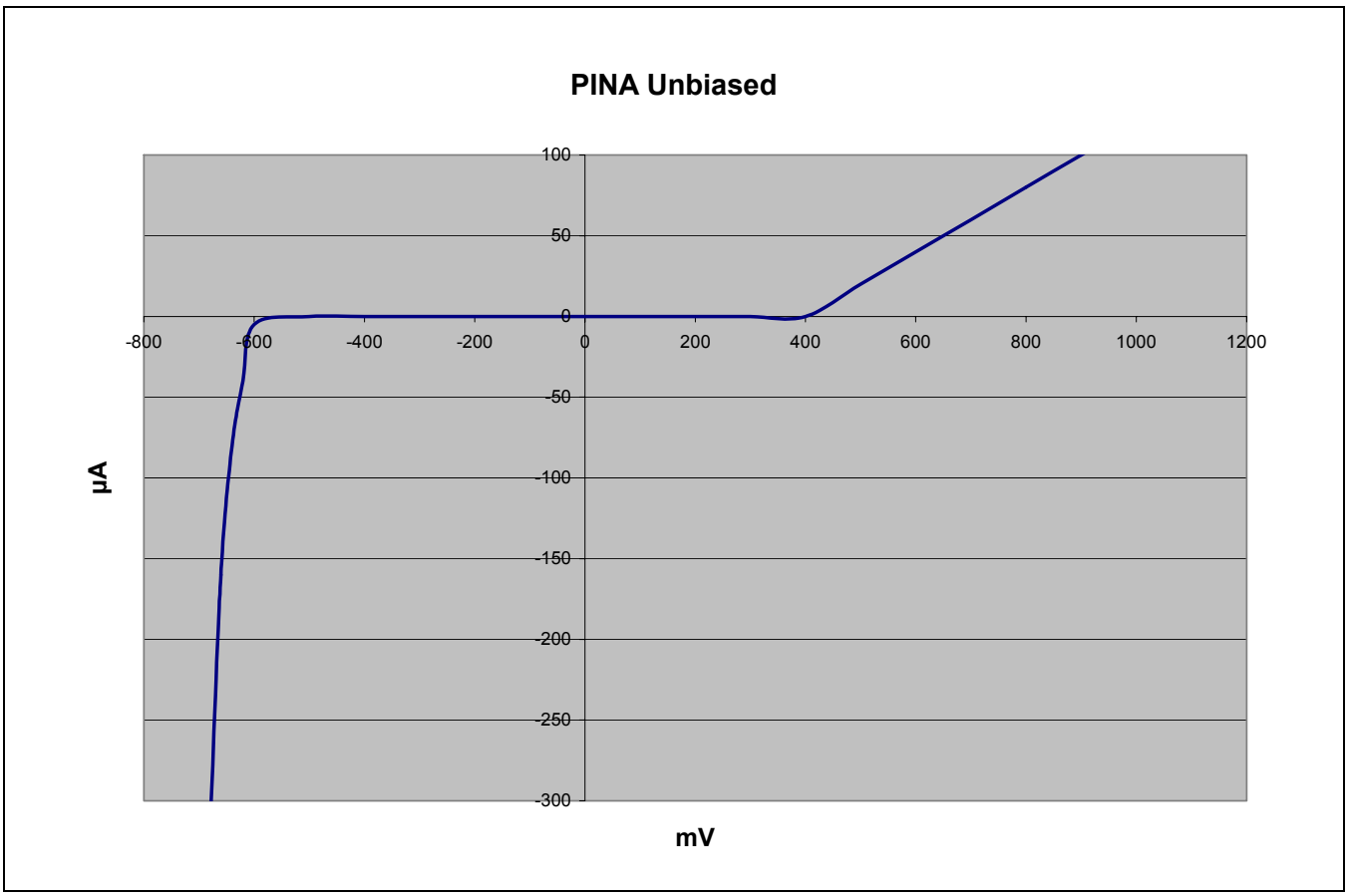
a. Ensure good humidity control in the environment (to help minimize ESD).
b. Consider using additional ionization of the air (also helps minimize ESD).
c. As a minimum, it is best to ensure that the body of the TO-can header or the ground lead of the header is grounded through the wire-bonding fixture for the following steps. The wire bonder itself should also be grounded.

1. Wire bond the ground pad(s) of the die first.
2. Then wire bond the V_{CC} pad to the TO-Can lead.
3. Then wire bond any other pads going to the TO-Can leads (such as DOUT, $\overline{\text{DOUT}}$ and possibly MON)
4. Next wire bond any capacitors inside the TO-Can.
5. Inside the TO-can, wire bond PINK.
6. The final step is to wire bond PINA.

4.7 TIA Use with Externally Biased Detectors

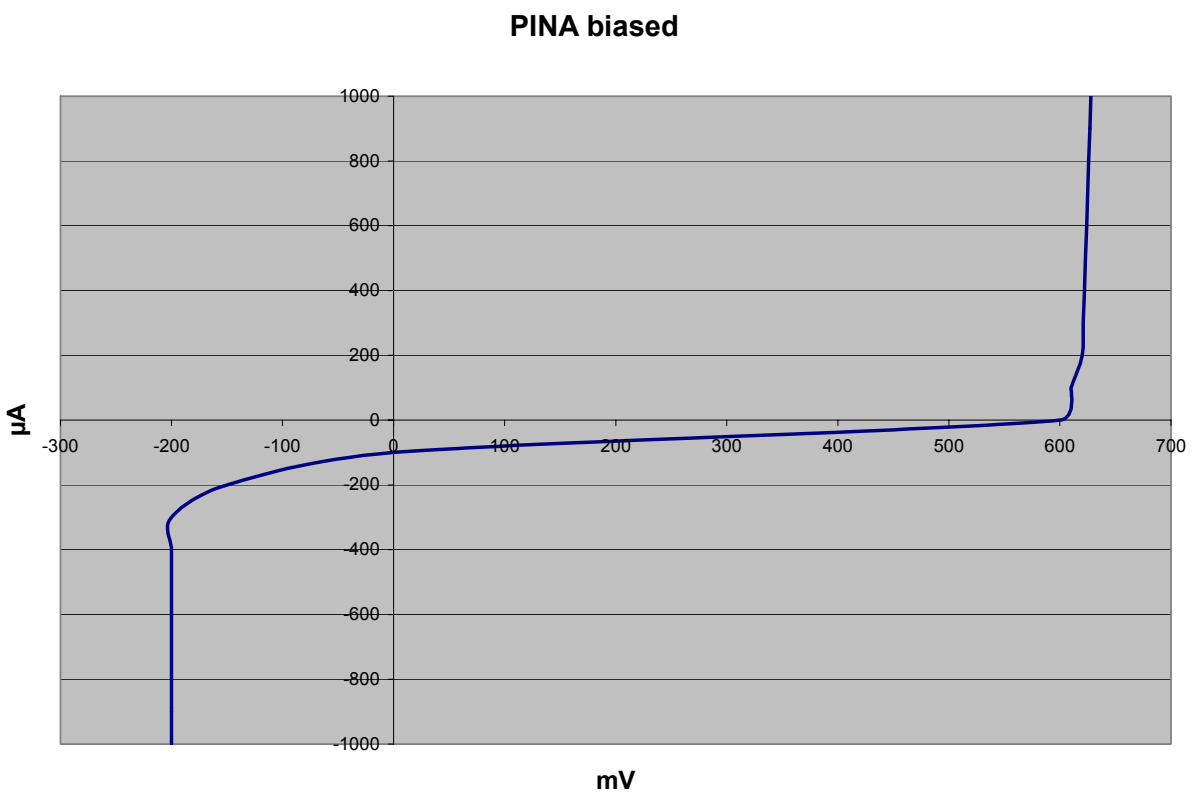
In some applications, Mindspeed TIAs are used with detectors biased at a voltage greater than available from TIA PIN cathode supply. This works well if some basic cautions are observed. When turned off, the input to the TIA exhibits the following I/V characteristic:

Figure 4-5. TIA Use with Externally Biased Detectors, Powered Off



In the positive direction after about 700 mV, the impedance of the input is relatively high. After the TIA is turned on, the DC servo and AGC circuits attempt to null any input currents (up to the absolute maximum stated in Table 1-1) as shown by the I/V curve in Figure 4-6.

Figure 4-6. TIA Use with Externally Biased Detectors, Powered On

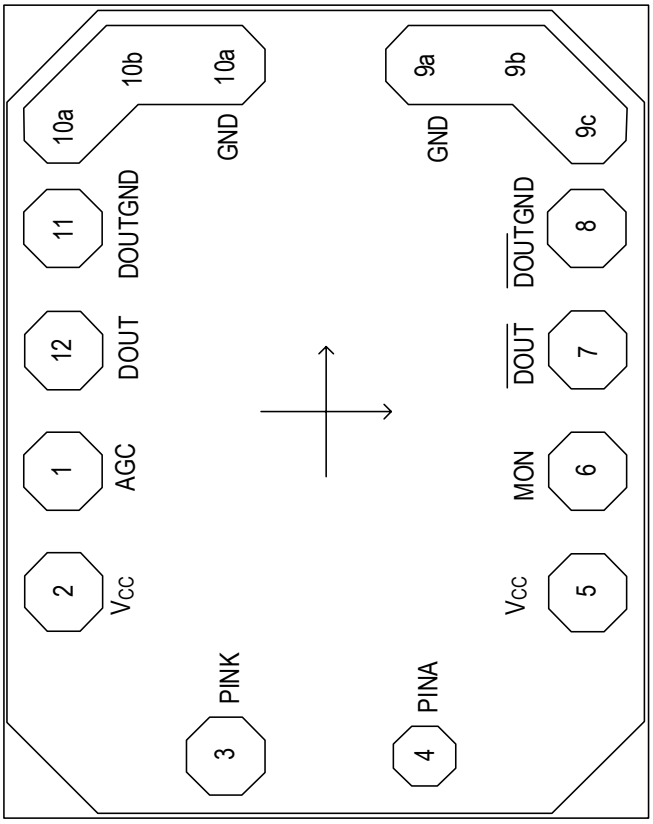


It can be seen that any negative voltage below 200 mV is nulled and that any positive going voltage above the PINA standing voltage is nulled by the DC servo. The DC servo upper bandwidth varies from part to part, but is generally at least 30 kHz.

When externally biasing a detector such as an APD where the supply voltage of the APD exceeds that for PINA Table 1-1, care should be taken to power up the TIA first and to keep the TIA powered up until after the power supply voltage of the APD is removed. Failure to do this with the TIA unpowered may result in damage to the input FET gate at PINA. In some cases the damage may be very subtle, in that nearly normal operation may be experienced with the damage causing slight reductions in bandwidth and corresponding reductions in input sensitivity.

5.0 Die Specification

Figure 5-1. Bare Die Layout



Pad Number	Pad	X	Y
1	AGC	-329	-76
2 (1)	V_{CC}	-329	-228
3	PINK	-124	-434
4	PINA	124	-434
5 (1)	V_{CC}	329	-228
6	MON	329	-76
7	$\overline{\text{DOUT}}$	329	76
8 (1)	$\overline{\text{DOUT}}$GND	329	228
9c (1, 2)	GND	329	360
9b (1, 2)	GND	255	434
9a (1, 2)	GND	124	434
10a (1, 2)	GND	-124	434
10b (1, 2)	GND	-255	434
10c (1, 2)	GND	-329	360
11 (1)	DOUTGND	-329	228
12	DOUT	-329	76

NOTES:

1. It is only necessary to bond one V_{CC} pad and one GND pad. However, bonding one of each pad (if available) on each side of the die is encouraged for improved performance in noisy environments.
2. Each location is an acceptable bonding location.

Notes:
Process technology: CMOS, Silicon Nitride passivation
Die thickness: 300 µm
Pad metallization: Aluminium
Die size: 880 µm x 1090
Pad opening: 86 µmsq.
Octagonal pad: 70 µm across flat PINA (70 µm x 70 µm)
Pad Centers in µm referenced to center of device
Connect backside bias to ground

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