# XR-2135A CCITT Data Buffer

## GENERAL DESCRIPTION

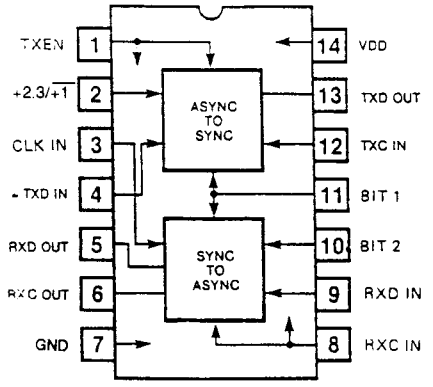
The XR-2135A is a digital circuit designed to perform the function of data buffering for various serial data systems, including modems. Both the asynchronous- to-synchronous conversion and the synchronous-to- asynchronous conversion are performed at data rates up to 19.2 kBPS. The XR-2135A is selectable for character lengths of 8, 9, 10 and 11 bits. A combined enable/disable input is supplied for the synchronous-to- synchronous and asynchronous-to-synchronous converter sections. This input allows the same data lines to be used for synchronous or asynchronous modes of operation.

The receive data buffer section (synchronous-to-asynchronous) accepts input synchronous data along with a receive clock and converts this to an asynchronous format. The transmit data buffer (asynchronous-to-synchronous) accepts on the input asynchronous data and will synchronize the data to a transmit clock. The transmit data input can accept data from -2.5% underspeed up to +2.3% overspeed in 8, 9,10 bit and 11 bit word modes. The +2.,3/+1* pin selects the overspeed capability. Automatic break extension is included in case of a break being received. The XR-2135A is constructed using polysilicon gate CMOS technology for low power and high speed operation. The master clock (CLK IN) can be clocked at speed up to 4.9152 MHz (19.2 kBPS data rate). The XR-2135A, available in a 14 pin package, is designed to operate with a single 5V supply.

## FEATURES

Data Rates up to 19.2 kBPS
Asynchronous-to-Synchronous Conversion
Synchronous-to-Asynchronous Conversion
Independent Disable Inputs for Receiver and Transmitter Sections
Single 5 Volt Supply Operation
Underspeed and Overspeed capability of -2.5% to +1%or + 2.5% to +2.3%
Missing Stop bit detector
Break extended for transmitted data
Programmable Character Lengths of 8, 9,10 or 11 bits

## PIN ASSIGNMENT




## ORDERING INFORMATION

| Part Number | Package | Operating Temperature |
|---|---|---|
| XR-2135ACN | Ceramic | 0°C to 70°C |
| XR-2135ACP | Plastic | 0°C to 70°C |

## APPLICATIONS

Modem Data Buffers
Terminals
Data Communication Test Equipment

## ABSOLUTE MAXIMUM RATINGS

| | |
|---|---|
| Power Supply | -0.3 to +7.0 V |
| Input Voltage | -0.3toVDD+0.3V |
| DC Input Current (any input) | ±10 mA |
| Power Dissipation (Package Limitation) | 250 mW |
| Storage Temperature Range | 65°C to +125C |

## ELECTRICAL CHARACTERISTICS

Test Conditions: VDD = 5VDC ±5%, TA= 25°C, CLK IN = 307.2 KHz ± 0.01%,
Data Rate - 1200 BPS $f_{TXC}$ IN = 1200 Hz $f_{RXC}$ IN= 1200 Hz ±0.01%, unless otherwise specified.

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNIT | CONDITIONS |
|---|---|---|---|---|---|---|
| DC CHARACTERISTICS | | | | | | |
| $V_{OL}$ | Output Low Voltage | | | 0.05 | V | $I_{OL}$= 20 uA |
| $V_{OH}$ | Output High Voltage | 4.8 | 5.0 | | V | $I_{OH}$= -20 uA |
| $V_{IL}$ | Input Low Voltage | | | 0.8 | V | |
| $V_{IH}$ | Input High Voltage | 2.4 | | | V | |
| $I_{OL}$ | Output Low Current | 2 | 7 | | mA | |
| $I_{OH}$ | Output High Current | | -9 | -400 | uA | |
| $I_{IN}$ | Input Leakage Current | -10 | 0 | 10 | uA | |
| $I_{DD}$ | Supply Current Quiescent | | 100 | 250 | uA | CLK IN, TXCIN, RXC IN At 5VDC |
| AC CHARACTERISTICS | | | | | | |
| $t_{wstr}$ | Start Bit Width | 819 | 821 | | uS | B1 = 1 B2 = 0 (10 bit) |
| BPS RANGE | Receiver Transmit | 1170 | 1200 | 1212 | BPS | 8, 9, and 10 Bit Mode |
| $f_{RXCO}$ | RXC OUTfrequency Multiplier | 1.015 | | | Hz/Hz | RXC OUT=1219 Hz |

## SYSTEM DESCRIPTION

The XR-2135A provides the complete interface between synchronous and character asynchronous formatted data systems. The synchronous side consists of two data lines TXD IN and RXD IN each with their respective clocks, TXC and RXC. Received data should change on the falling edge of RXC and be stable on the rising edge of RXC. The asynchronous-to-synchronous conversion handies data that is formatted so that the data bits or data and parity bits are bracketed by start and stop bits. Acceptable character lengths are 8, 9, 10 and 11 bits. The word length is pin selectable.

The XR-2135A is optimized for applications where a single clock is the source for the master clock (CLK IN), the TXDIN IN and RXC IN. The master clock (CLK IN) is 256 times the data rate. In modem applications, the RXC IN should be in lock with the received data, and jitter should be less than ±30 ns. The asynchronous transmit data being clock in by an asynchronous clock at the data rate (CLK IN/256). The asynchrorious-to- synchronous converter when receiving overspeed data will shave on the stop bit. The break signal extended will detect a missing stop bit and extend this an additional character length and 3 bits.

## PRINCIPLES OF OPERATION

The XR-2135A data buffer can be separated into three blocks: the asynchronous-to-synchronous converter for the transmitted data, the synchronous-to-asynchronous converter for the received data and the master dock divider.

The asynchronous-to-synchronous converter uses a two bit shift register to allow resetting of the stop bit to compensate for underspeed conditions.

A counter circuit, synchronized to the location of the stop start bit occurrence is used to control when the stop bit needs to be adjusted. An 11 bit shift register is used to monitor the data for the occurrence of a break signal.

The break extended is activated by the continuous reception of a series of logic 0s for one entire word's time (8, 9, 10 or 11 bits depending upon the setting of BIT 2 and BIT 1). When this oocurs, the synchronized register is reset, and 2 words + 3 bits of logic 0s are shifted out and appear at TXD OUT.

If 1% overspeed data is received, and the modem is selected for 8, 9, 10 or 11 bit word operation, the stop bit in the word will be increased in width. In the case of underspeed, the stop bit will be truncated, when the one bit shift register is reset. When the +2.3% mode is selected the operation remains the same, only a different timer is used to determine the location of the stop bit.

The enable pin, Pin 1, controls the bypassing of the asynchronous-to-synchronous converter and the synchronous-to-asynchronous converter. The bypass mode is buffered and the delay through the buffer is less than 30 ns.

The synchronous to asynchronous converter contains a 21 bit synchronous shift register and a 8,9, 10 or 11 bit programmable parallel loading asynchronous shift register also uses a stop-start bit detector. The difference is that a missing stop bit detector is needed for synchronous data that is received without a stop bit. When this occurs, the last stage of the asynchronous shift register is set, and a stop bit re-inserted. The asynchronous shift register is clocked at a rate that is 1.015 times the nominal data rate. For 1200 BPS, this is 1219. For 9600 BPS, the rate would be 9744 BPS.

The master clock divider takes the CLK IN and divides by 256 to provide the internal data clocks as well as producing various reset pulses to perform the functions described above.

## PIN DESCRIPTIONS

| PIN# | SYMBOL | DESCRIPTION |
|---|---|---|
| 1 | TXEN | Enable Input: This input when tied to a logic high permits the TXD IN to be clocked through the asynchronous-to-synchronous converter. When this input is tied to a logic low, the shift registers of the asynchronous-to-synchronous converter and synchronous-to-asynchronous converters are bypassed and both TXEN and RXD IN are buffered and connected. |
| 2 | +2.3/+1 | Overspeed Enable Input: This input when tied to a logic high enables the asynchronus-to-synchronous converter to accept data at a rate from-2.5% to +1%. When disabled, |

| PIN# | SYMBOL | DESCRIPTION |
|---|---|---|
| 3 | CLK IN | Master Clock Input: This clock provides the asynchronous clocks and reset pulses used by the XR-2135 to perform the asynchronous-to-synchronous conversion as well as the synchronous to asynchronous conversion. The formula to use for determining the datarate is CLK IN / 256-data rate in BPS. |
| 4 | TXD IN | Transmit Data Input: The serial data should be applied to this pin. When 8, 9, or 10 bits are selected, the range for the data rate is -2.5% to +1%. This input has a high input impedance. |
| 5 | RXD OUT | Received Data Output: This is the asynchronous received data output (when TXEN is tied high). The data rate of this output is 1.5 times the synchronous data rate. |
| 6 | RXC OUT | Received Clock Output: This clock is synchronized with the RXD OUT. It should be noted that when stop bits are being inserted or deleted, the clock will produce a pulse at the time of the stop bit.being shifted out at RXD OUT. |
| 7 | GND | This pin should be tied to the digital ground of theXR-2135. |
| 8 | RXC IN | Receive Clock Input: The received clock synchronous with the received data should be tied to this pin. The acceptable litter is only $\pm$30ns relative to the data. The data should be stable on the rising edge of this clock and change on the failing edge. If the received data is bit asynhronous (no clock relative to the data) this pin does not have to be clock for the data to appear at RXD OUT if TXEN is at a logic low. |
| 9 | RXD IN | Received Data input: The synchronous data is applied to this pin. |
| 10 | BIT 2 | Character Length Select: |
| 11 | BIT 1 | These two digital inputs control the length of the word that will be applied to the XR-2135. Refer to Table 2 for the truth table of the function. |
| 12 | TXC IN | Transmit Clock Input: The system clock that the transmit data is to be synchronized to be tied to this pin. Note that this clock must be locked to the master clock CLK IN. Acceptatble variation is +0.01%. In many modem applications this is not a problem. |
| 13 | TXDOUT | Transnmit Data Output: This output provides the serial data synchronous to the clock applied to TXCIN if TXEN is at a logic high. In an underspeed situation, all bits will be shortened. In an over- speed situation, all bits will be widened. If TXEN is at a logic low this output will provide a buffered version the data at TXD IN. The amount of delay is 30 ns. |
| 14 | $V_{DD}$ | Positive Supply: This input should be tied to 5 V $\pm$ 5%. A 0.1 $\mu$F decoupling capacitor should be adequate for decoupling any system noise to ground. |

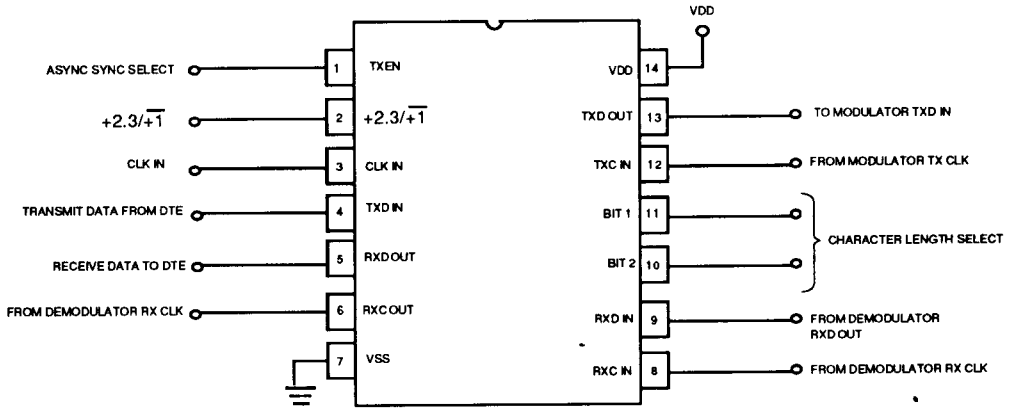
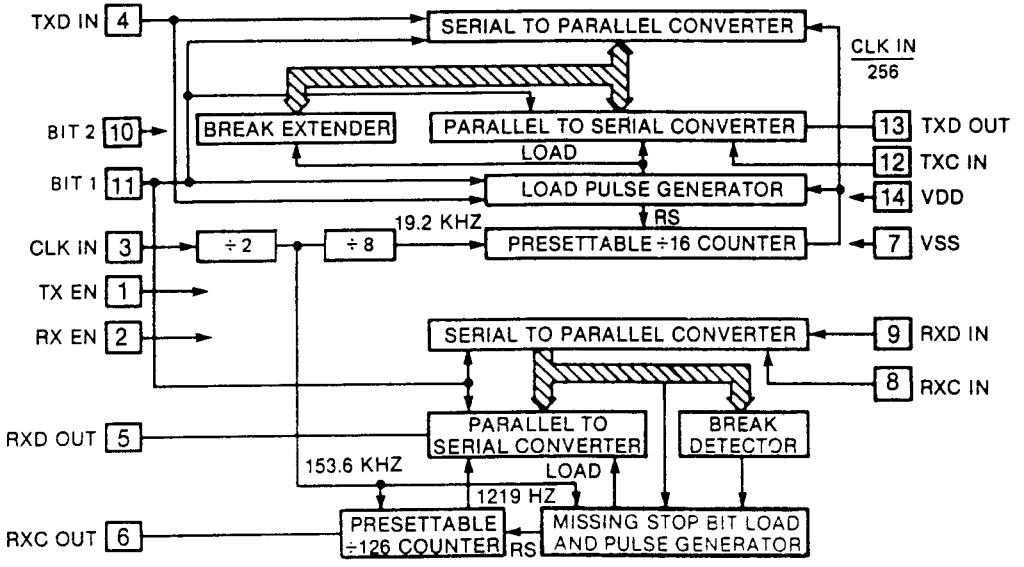



**Figure 1. Test Circuit**

| BIT 1 (11) | BIT 2 (10) | CHARACTER LENGTH |
|---|---|---|
| 0 | 0 | 8 Bit |
| 0 | 1 | 9 Bit |
| 1 | 0 | 10 Biit |
| 1 | 1 | 11 Bit |

**Table 2. Character Length Selection**




FREQUENCIES SHOWN ARE FOR 1200 BPS OPERATION,
CLK IN EQUALS 307.2 KHZ

**Figure 2. Equivalent Schematic Diagram**

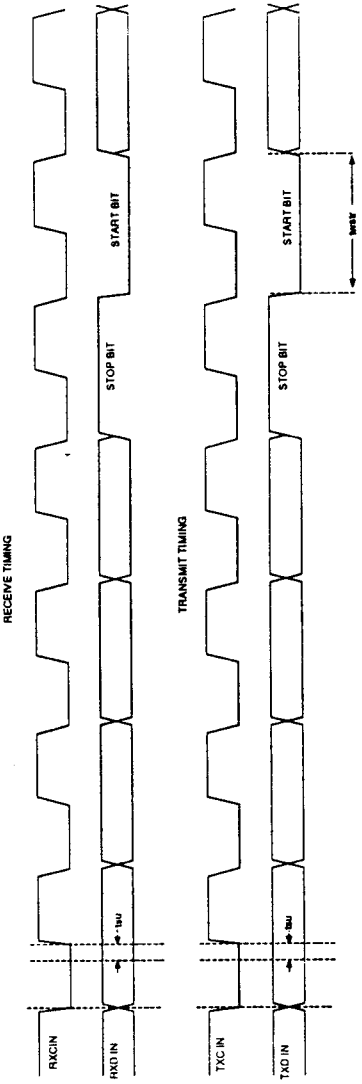



Figure 3. Transmit Receive Timing Characteristics

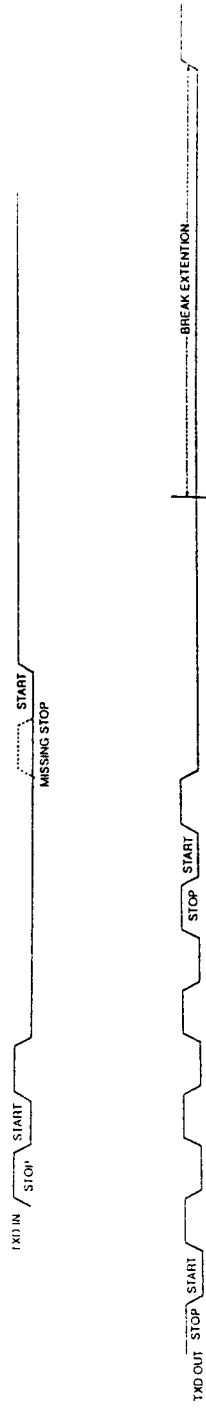



Figure 4. Break Extention and Data Delay Example at 8 Bit Word Length