

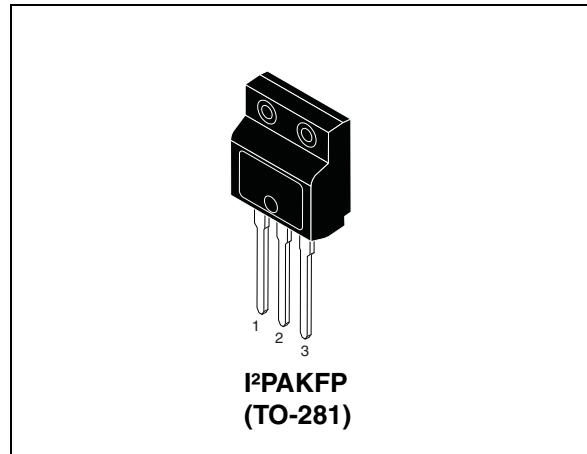
## N-channel 600 V, 0.135 $\Omega$ , 20 A MDmesh™ II Power MOSFET in I<sup>2</sup>PAKFP package

Datasheet — production data

### Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STFI26NM60N	600 V	< 0.165 $\Omega$	20 A

- Fully insulated and low profile package with increased creepage path from pin to heatsink plate
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance



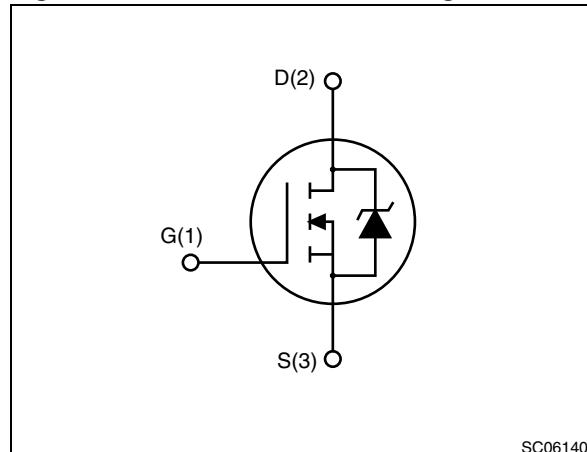
### Applications

- Switching applications

### Description

This device is an N-channel Power MOSFET developed using the second generation of MDmesh™ technology. This revolutionary Power MOSFET applies a new vertical structure to the company's strip layout to yield a device with one of the world's lowest on-resistance and gate charge, making it suitable for the most demanding high-efficiency converters.

Figure 1. Internal schematic diagram



SC06140

Table 1. Device summary

Order codes	Marking	Package	Packaging
STFI26NM60N	26NM60N	I <sup>2</sup> PAKFP (TO-281)	Tube

## Contents

<b>1</b>	<b>Electrical ratings</b>	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b>	<b>4</b>
2.1	Electrical characteristics (curves)	6
<b>3</b>	<b>Test circuits</b>	<b>8</b>
<b>4</b>	<b>Package mechanical data</b>	<b>9</b>
<b>5</b>	<b>Revision history</b>	<b>11</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	600	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25^\circ\text{C}$	20 <sup>(1)</sup>	A
$I_D$	Drain current (continuous) at $T_C = 100^\circ\text{C}$	12.6 <sup>(1)</sup>	A
$I_{DM}^{(2)}$	Drain current (pulsed)	80 <sup>(1)</sup>	A
$P_{TOT}$	Total dissipation at $T_C = 25^\circ\text{C}$	35	W
	Derating factor	0.28	W/ $^\circ\text{C}$
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t=1\text{ s}; T_C=25^\circ\text{C}$ )	2500	V
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Limited by maximum junction temperature.
2. Pulse width limited by safe operating area .
3.  $I_{SD} \leq 20\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{DSpeak} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\%$   $V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	3.6	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal resistance junction-ambient max	62.5	$^\circ\text{C}/\text{W}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AS}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	6	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j=25^\circ\text{C}$ , $I_D=I_{AS}$ , $V_{DD}=50\text{ V}$ )	610	mJ

## 2 Electrical characteristics

( $T_{CASE} = 25^\circ\text{C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0$	600			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 600 \text{ V}$ $V_{DS} = 600 \text{ V}, T_C = 125^\circ\text{C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25 \text{ V}$			$\pm 0.1$	$\mu\text{A}$
$V_{GS(\text{th})}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250 \mu\text{A}$	2	3	4	V
$R_{DS(\text{on})}$	Static drain-source on-resistance	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$		0.135	0.165	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance			1800		pF
$C_{oss}$	Output capacitance	$V_{DS} = 50 \text{ V}, f = 1 \text{ MHz}, V_{GS} = 0$	-	115	-	pF
$C_{rss}$	Reverse transfer capacitance			1.1		pF
$C_{oss \text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0 \text{ to } 480 \text{ V}$	-	310	-	pF
$Q_g$	Total gate charge	$V_{DD} = 480 \text{ V}, I_D = 20 \text{ A}, V_{GS} = 10 \text{ V}$		60		nC
$Q_{gs}$	Gate-source charge		-	8.5	-	nC
$Q_{gd}$	Gate-drain charge	(see Figure 15)		30		nC
$R_g$	Gate input resistance	f=1 MHz gate DC Bias=0 test signal level = 20 mV open drain	-	2.8	-	$\Omega$

1.  $C_{oss \text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time			13		ns
$t_r$	Rise time			25		ns
$t_{d(off)}$	Turn-off delay time	$V_{DD} = 300 \text{ V}, I_D = 10 \text{ A}$ $R_G = 4.7 \Omega, V_{GS} = 10 \text{ V}$	-	85	-	ns
$t_f$	Fall time	(see Figure 14)		50		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}^{(1)}$	Source-drain current Source-drain current (pulsed)		-		20 80	A A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 20 \text{ A}, V_{GS} = 0$	-		1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 20 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 16)	-	370 5.8 31.6		ns $\mu\text{C}$ A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD} = 20 \text{ A}, dI/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}, T_j = 150 \text{ }^\circ\text{C}$ (see Figure 16)	-	450 7.5 32.5		ns $\mu\text{C}$ A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

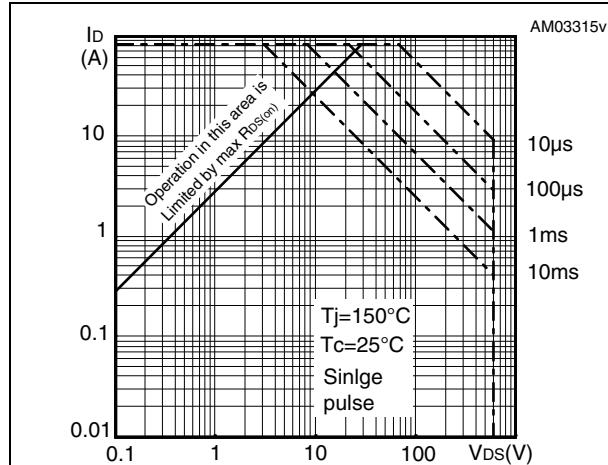


Figure 3. Thermal impedance

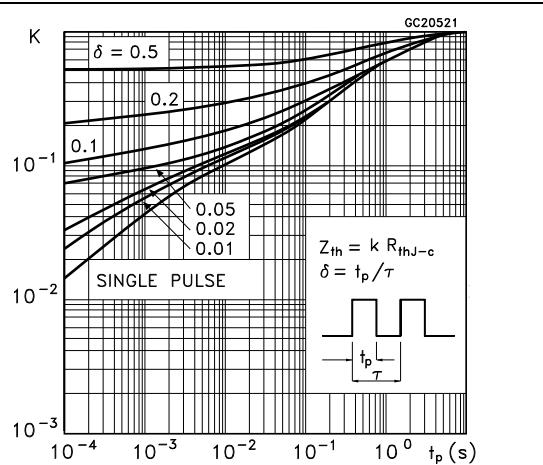


Figure 4. Output characteristics

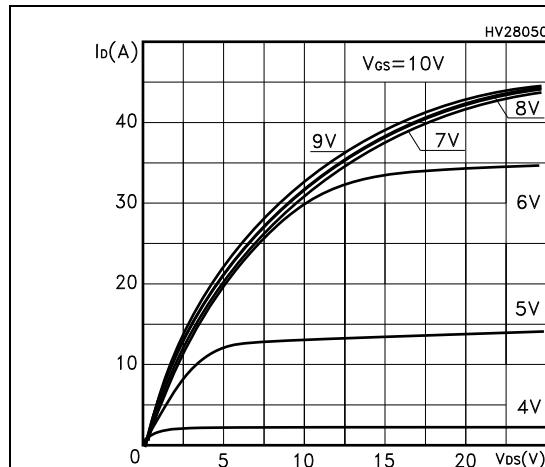


Figure 5. Transfer characteristics

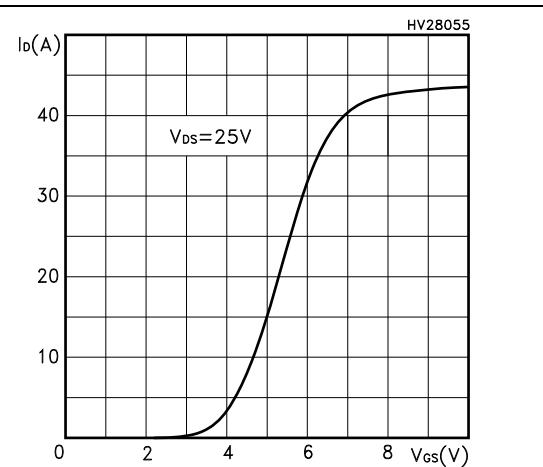


Figure 6. Transconductance

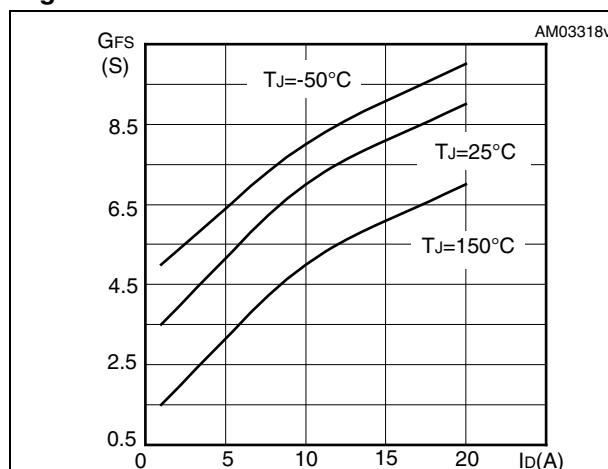
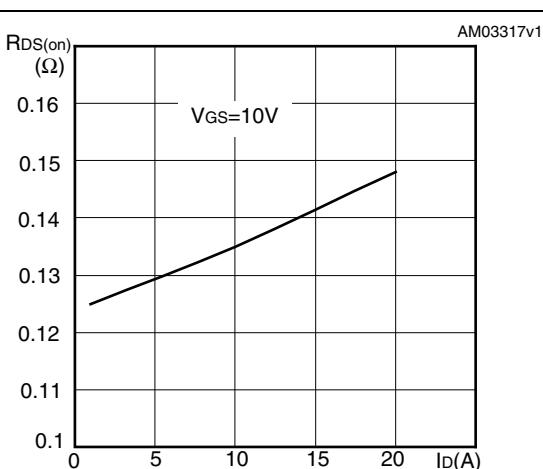
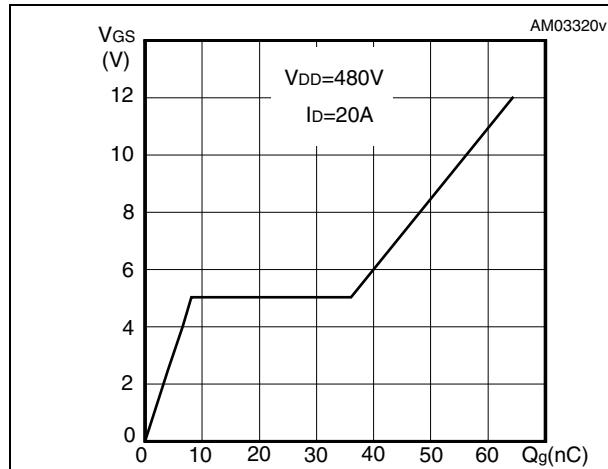
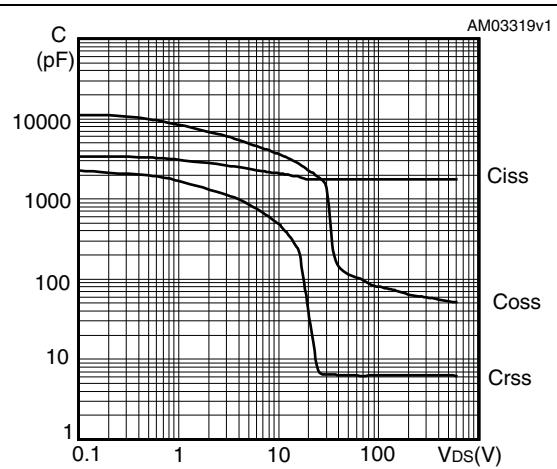
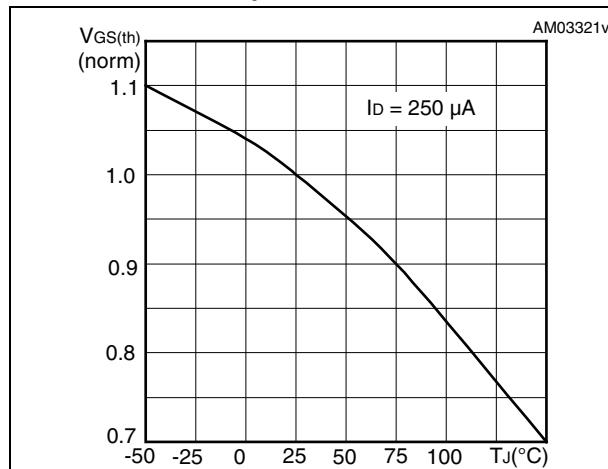
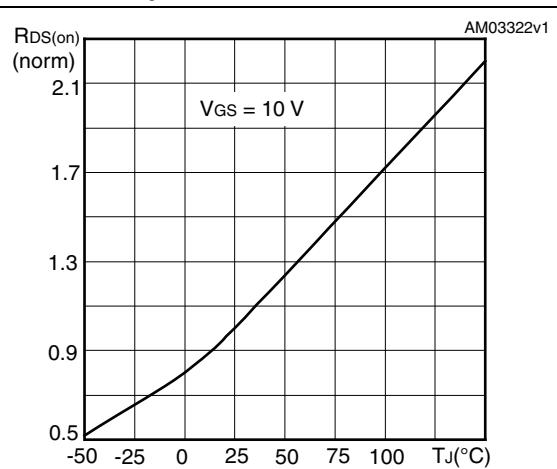
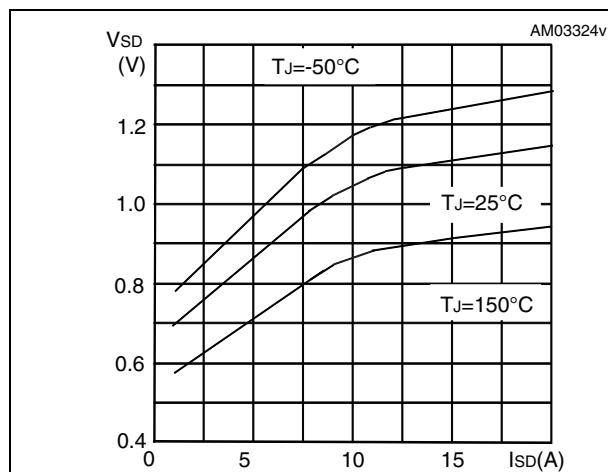
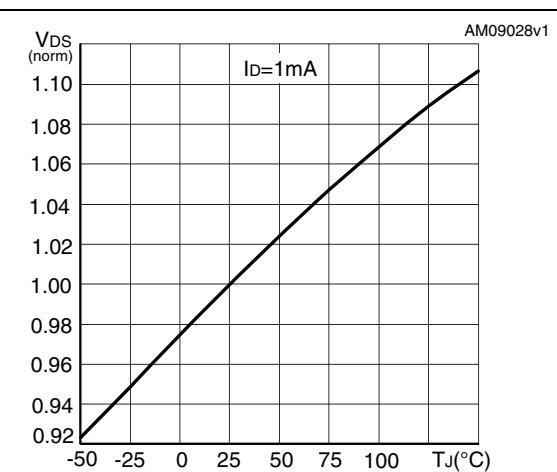


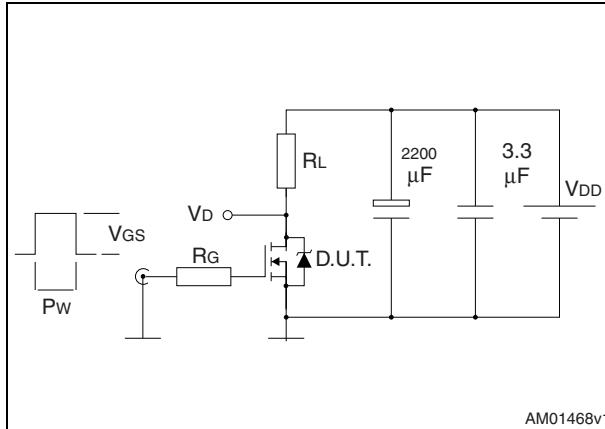
Figure 7. Static drain-source on-resistance



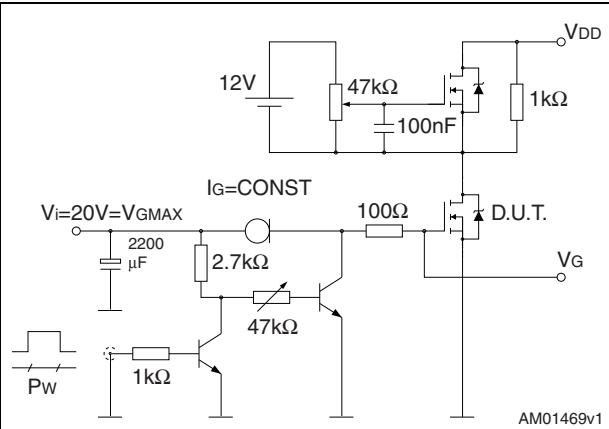
**Figure 8. Gate charge vs gate-source voltage****Figure 9. Capacitance variations****Figure 10. Normalized gate threshold voltage vs temperature****Figure 11. Normalized on resistance vs temperature****Figure 12. Source-drain diode forward characteristics****Figure 13. Normalized V<sub>DS</sub> vs temperature**

### 3 Test circuits

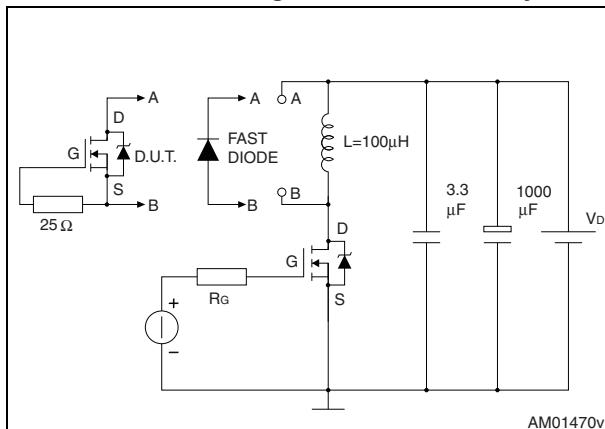
**Figure 14. Switching times test circuit for resistive load**



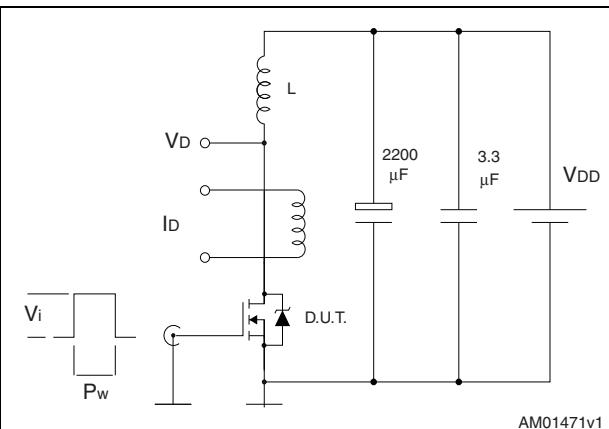
**Figure 15. Gate charge test circuit**



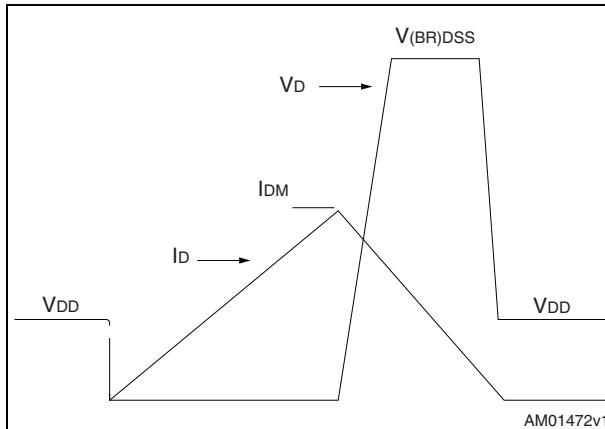
**Figure 16. Test circuit for inductive load switching and diode recovery times**



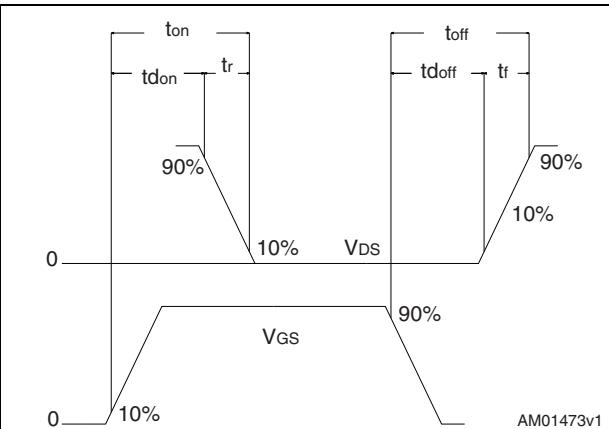
**Figure 17. Unclamped inductive load test circuit**



**Figure 18. Unclamped inductive waveform**



**Figure 19. Switching time waveform**

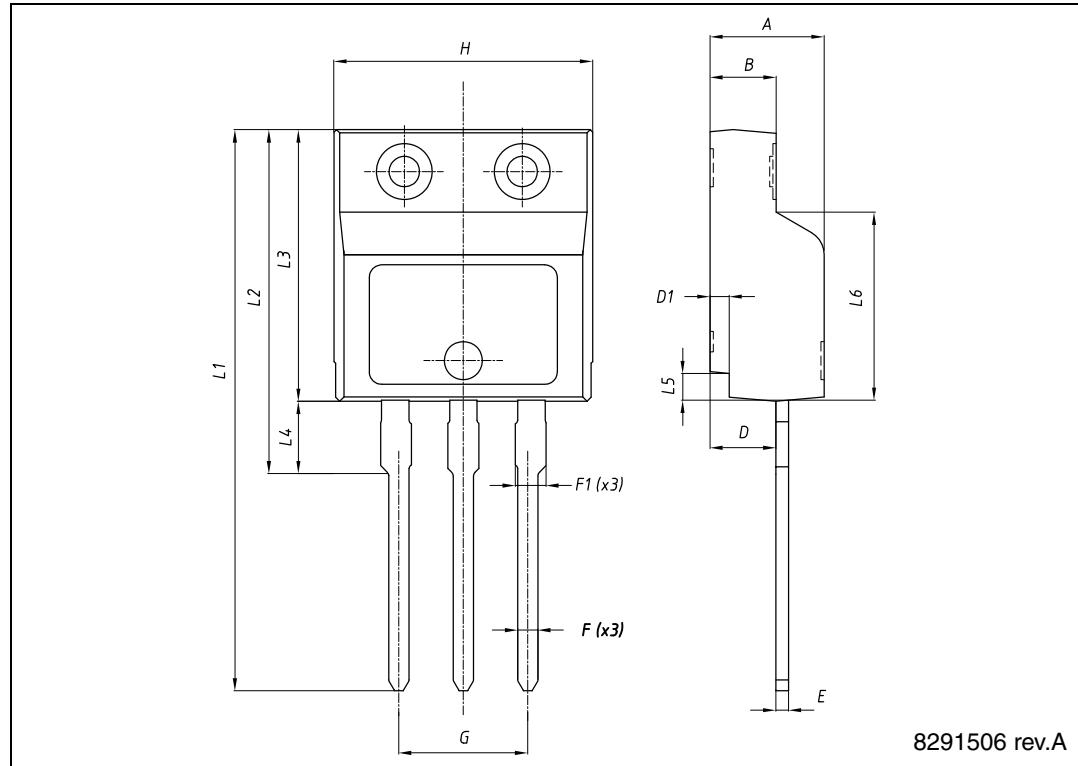


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

**Table 9.** I<sup>2</sup>PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

**Figure 20.** I<sup>2</sup>PAKFP (TO-281) drawing

## 5 Revision history

**Table 10. Document revision history**

Date	Revision	Changes
15-Nov-2011	1	First release.
04-Jun-2012	2	Document status promoted from preliminary data to production data. Updated $P_{TOT}$ and derating factor values in <i>Table 2: Absolute maximum ratings</i> , $R_{th-case}$ value in <i>Table 3: Thermal data</i> Package name has been updated.

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