Failsafe Watchdog

Features

- Failsafe watchdog function: timeout warning after 1st timeout period, reset after 2nd timeout period, reset remains active to avoid further failures
- Standard timeout period and power-on reset time (10 ms), externally programmable if required
- V_{IN} monitoring with 3 standard or programmable trigger voltages for: power-on reset initialization, advanced power-fail warning ($\overline{SAVE}$), reset at power-down ($\overline{RES}$)
- V_{DD} monitoring: power-on reset initialization enabled only if $V_{DD} \geq 3.5$ V
- Internal voltage reference
- Works down to 1.5 V supply voltage
- Push-pull or Open drain outputs
- Low current consumption
- Available for normal and extended temperature range
- DIP8 and SO8 package

Description

The H 6006 is a monolithic low power CMOS device combining a programmable digital timer and a series of voltage comparators on the same chip. The device is specially convenient for Watch-Dog functions such as microprocessor and supply voltage monitoring. The watchdog part is designed to be used in all applications where it is important that after the occurence of a malfunction the microprocessor system is stopped to avoid further damage. The timeout warning signal ($\overline{TO}$) can be used to try to reactivate the system before halting it. The voltage monitoring part provides double security by combining both unregulated voltage and regulated voltage monitoring simultaneously. The H 6006 initializes the power-on reset after V_{IN} reached V_{SH} and V_{DD} raises above 3.5 V. If V_{IN} drops below V_{SL}, the H 6006 gives an advanced warning signal for register saving and if the voltage drops further below V_{RL}, $\overline{RES}$ goes active. The H 6006 functions at any supply voltage down to 1.5V and is therefore particularly suited for start-up and shut-down control of microprocessor systems

Applications

- Microprocessor and microcontroller systems
- Point of sales equipment
- Telecom products
- Automotive subsystems

Typical Operating Configuration

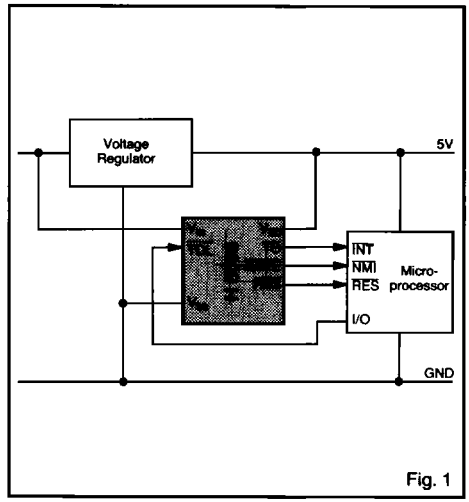


Fig. 1

Pin Assignment

DIP8 / SO8

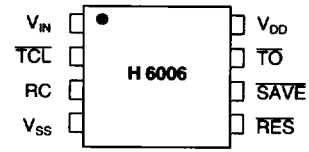


Fig. 2

Absolute Maximum Ratings

Parameter	Symbol	Conditions
Voltage V_{DD} to V_{SS}	V_{DD}	−0.3 to +8V
Voltage at any pin to V_{SS}	V_{MIN}	−0.3
Voltage at any pin to V_{DD} (except V_{IN})	V_{MAX}	+0.3
Voltage at V_{IN} to V_{SS}	V_{INMAX}	+15V
Current at any output	I_{MAX}	±10mA
Storage temperature	T_{STO}	−65...+150°C

Table 1

Stresses above these listed maximum ratings may cause permanent damage to the device. Exposure beyond specified operating conditions may affect device reliability or cause malfunction.

Handling Procedures

This device has built-in protection against high static voltages or electric fields; however, anti-static precautions must be taken as for any other CMOS component.

Unless otherwise specified, proper operation can only occur when all terminal voltages are kept within the supply voltage range. Unused inputs must always be tied to a defined logic voltage level.

Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Units
Operating temperature					
Industrial	T_{AI}	−40		+85	°C
Extended	T_{AX}	−40		+125	°C
Supply voltage	V_{DD}	1.5		5.5	V
Comparator input voltage					
Version A2, A3, B2, B3	V_{IN}	0		V_{DD}	V
Version A1, B1	V_{IN}	0		12	V
RC-oscillator programming (see Fig. 15)					
External capacitance	C1			100	nF
External resistance	R1	10			kΩ

Table 2

Electrical Characteristics

V_{DD} = 5.0 V, T_A = −40 to +85°C (−40 to +125°C for extended temperature range version), unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
V_{DD} activation threshold	V_{ON}	T_A = 25°C	3		3.5	V
V_{DD} deactivation threshold	V_{OFF}	T_A = 25°C		V_{ON}−1.5		V
Supply current	I_{DD}	RC open, TCL=5V, V_{IN}=0V		50	140	µA
Input V_{IN}, $\overline{TCL}$						
Leakage current	I_{IP}	$V_{SS} \le V_{IP} \le V_{DD}$; T_A = 85°C		0.005	1	µA
Input current on pin V_{IN}	I_{IN}	Versions A1, B1; V_{IN} = 10V		100	180	µA
$\overline{TCL}$ input low level	V_{IL}				0.8	V
$\overline{TCL}$ input high level	V_{IH}		2.4			V
$\overline{TO}$, $\overline{SAVE}$, $\overline{RES}$ Outputs						
Leakage current	I_{OLK}	Versions A1, A2, A3; $V_{OUT} = V_{DD}$		0.05	1	µA
Drive currents (all versions)	I_{OL}	V_{OL} = 0.4V	3.2	8		mA
	I_{OL}	V_{DD} = 3.5V; V_{OL} = 0.4V	2			mA
	I_{OL}	V_{DD} = 1.6V; V_{OL} = 0.4V	80			µA
Drive currents (versions B1, B2, B3)[1]	I_{OH}	V_{OH} = 4.0V	3.2	8		mA
	I_{OH}	V_{DD} = 3.5V; $V_{OH} \ge$ 2.8V	2			mA
	I_{OH}	V_{DD} = 1.6V; $V_{OH} = V_{DD}$−0.4	80			µA

[1] Versions: An = open drain outputs; Bn = push-pull outputs

Table 3

V_{IN} Surveillance

Voltage thresholds at T_A = 25°C

Version[1]	Comparator Reference	Input Resistance R_{VIN}	Thresholds	Threshold Tolerance	Ratio Tolerance[3]
A1, B1	V_{DD}	100kΩ	9.00 8.00 7.00[2]	± 5%	± 2%
A2, B2	V_{DD}	~100MΩ	2.25 2.00 1.75[2]	± 5%	± 2%
A3, B3	Band-gap reference	~100MΩ	2.00 1.95 1.90	±10%	± 2%

[1] Versions: An = open drain outputs; Bn = push-pull outputs

[2] at V_{DD} = 5V

[3] Threshold ratio as V_{SH}/V_{SL} or V_{SL}/V_{RL}

Table 4

Timing Characteristics

V_{DD} = 5.0 V, T_A = −40°C to +85°C (−40 to +125°C for extended temperature range version), unless otherwise specified

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Units
Propagation delays						
$\overline{TCL}$ to output pins	T_{DIDO}			250	500	ns
V_{IN} to output pins	T_{AIDO}	Excluding debounce time T_{DB}		4	10	µs
Logic transition times on all output pins	T_{TR}	Load 10kΩ, 100pF		30	100	ns
Timeout period	T_{TO}	RC open, unshielded, T_A = 25°C	6	10	16	ms
	T_{TO}	RC open, unshielded (not tested)	4.5		20	ms
T_{TCL} input pulse width	T_{TCL}		150			ns
Power-on reset debounce	T_{DB}			$T_{TO/32}$		ms

Table 5

Timing Waveforms

Voltage reaction: V_{DD} Monitoring

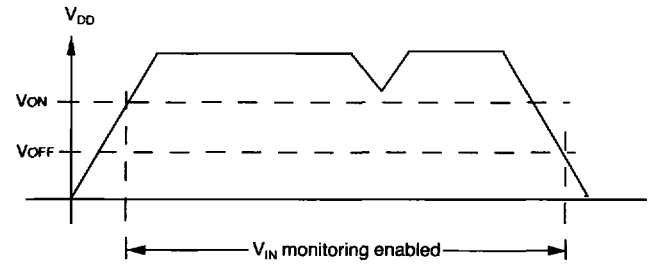


Fig. 3

Voltage Reaction: V_{IN} Monitoring

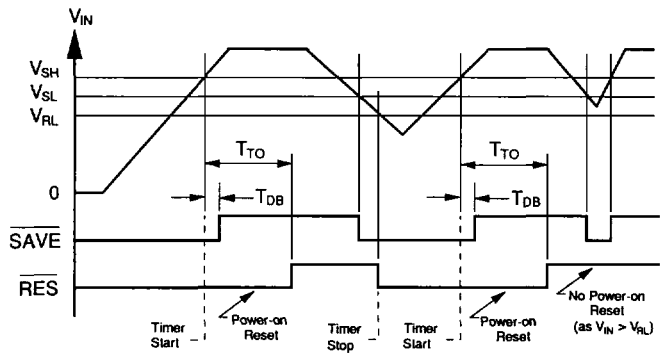
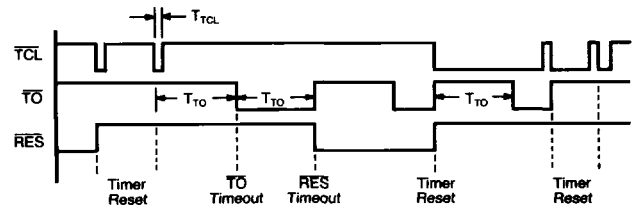


Fig. 4

Timer Reaction



Conditions:
$V_{IN} > V_{RL}$ after power-up sequence.

Fig. 5

Combined Voltage and Timer Reaction

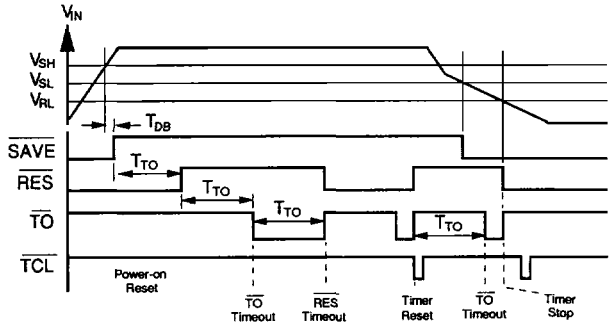
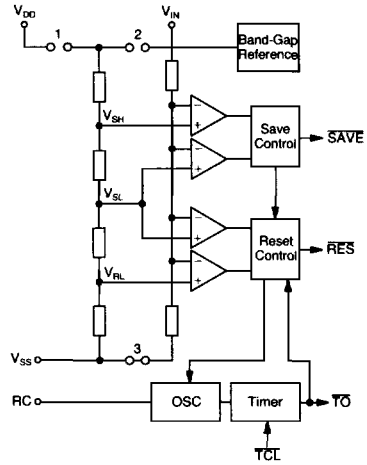


Fig. 6

Block Diagram



Version	Connections
A1, B1	1 and 3
A2, B2	1
A3, B3	2

Fig. 7

Pin Description

Pin	Name	Function
1	V_{IN}	Voltage monitoring input
2	$\overline{TCL}$	Timer clear input signal
3	RC	RC oscillator tuning input
4	V_{SS}	GND terminal
5	$\overline{RES}$	Reset output
6	$\overline{SAVE}$	Save output
7	$\overline{TO}$	Timer output signal
8	V_{DD}	Positive supply voltage terminal

Table 6

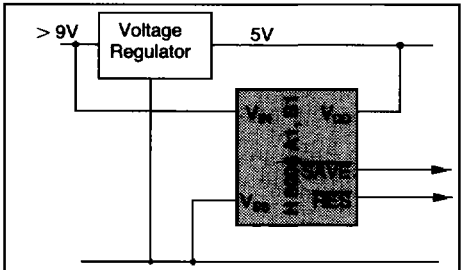
Functional Description

Supply Lines
The circuit is powered through the V_{DD} and V_{SS} pins. It monitors both its own V_{DD} supply and a voltage applied to the V_{IN} input.

V_{DD} Monitoring
During power-up the V_{IN} monitoring is disabled and $\overline{RES}$ and $\overline{SAVE}$ stay active low as long as V_{DD} is below V_{ON} (3.5V). As soon as V_{DD} reaches the V_{ON} level, the state of the outputs depend on the watchdog timer and the voltage at V_{IN} relative to the thresholds (see Fig. 3 and 4). If the supply voltage V_{DD} falls back below V_{OFF} (1.5V) the watchdog timer and the V_{IN} monitoring are disabled and the outputs $\overline{SAVE}$ and $\overline{RES}$ are active low. The V_{DD} line should be free of spikes.

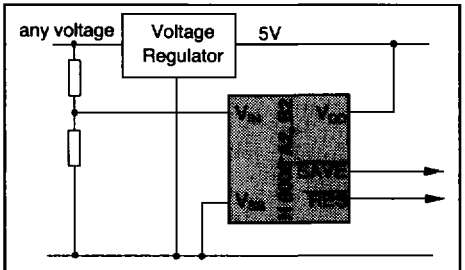
V_{IN} Monitoring
The analog voltage comparators compare the voltage applied to V_{IN} (typically connected to the input of the voltage regulator) with the stabilized supply voltage V_{DD} (versions A1, B1, A2, B2) or with the bandgap voltage (versions A3, B3) (see Fig. 7). At power-up, when V_{DD} reached V_{ON} and V_{IN} reaches the V_{SH} level, the $\overline{SAVE}$ output goes high, and the timer starts running, setting $\overline{RES}$ high after the time T_{TO} (see Fig. 4). If V_{IN} falls below V_{SL}, the $\overline{SAVE}$ output goes low and stays low until V_{IN} rises again above V_{SH}. If V_{IN} falls below the voltage V_{RL}, the $\overline{RES}$ output will go low and the on-chip timer will stop. When V_{IN} rises again above V_{SH}, the timer will initiate a power-up sequence. The $\overline{RES}$ output may however be influenced independently of the voltage V_{IN} by the timer action, see section „Combined Voltage and Timer Action". Monitoring the rough DC side of the regulator as shown in Fig. 12 is the only way to have advanced warning at power-down. Spikes on V_{IN} should be filtered if they are likely to drop below V_{SL}.
The combination of V_{IN} and V_{DD} monitoring provide high system security: if V_{IN} rises much faster than V_{DD}, then the device starts the power-on sequence only when V_{DD} reached V_{ON} (Fig. 3). Short circuits on the regulated supply voltage can be detected.

Voltage Thresholds on V_{IN}
The H 6006 is available with 3 different sets of thresholds:
Version A1, B1: with internal voltage divider, resulting in thresholds for direct monitoring of the unregulated voltage without external components.



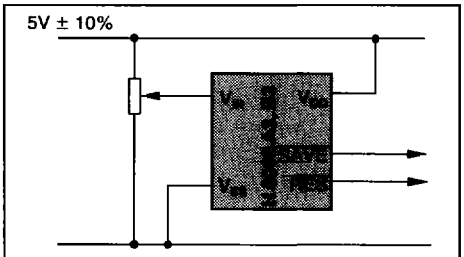
Note: The threshold levels are 9/8/7 V normally. These are divided internally by 4 to give internal thresholds of 2.25 / 2 / 1.75 V. V_{DD} = 5V (thresholds dependent on V_{DD}). R_{VIN} = ~ 100kΩ Fig. 8

Version A2, B2: for monitoring of all unregulated voltage, where custom programming is required. Fix resistor values can be used for programming.



Note: the internal threshold levels are 2.25/2.00/1.75V at V_{DD} = 5V (threshold dependent on V_{DD}) R_{VIN} = ~100MΩ Fig. 9

Version A3, B3: for monitoring of regulated voltage, where no unregulated voltage is available (the tolerance is ± 10%, see Tabel 4. For tighter tolerances, trimming can be used, see Fig. 10).



Note: the internal threshold levels are 2.00/1.95/1.90V (threshold dependent on the internal bandgap reference) R_{VIN} = ~100MΩ Fig. 10

Monitoring of the unregulated voltage require versions A1, B1, A2 and B2. The versions are based on the principle that V_{DD} rises with V_{IN} on power-up and V_{DD} holds up for a certain time after V_{IN} starts dropping on power-down. The version A1 and B1 have a 100kΩ nominal resistance from V_{IN} to V_{SS} (internal voltage divider). The versions A2, B2, A3 and B3 have high impedance V_{IN} inputs (see Fig. 7 and Table 4) for external threshold voltage programming by a voltage divider on pin V_{IN}. The levels obtained are proportional to the internal levels V_{SH}, V_{SL} and V_{RL} on the chip itself (see Electrical Specifications).

Timer Programming

With pin RC unconnected, the on-chip RC oscillator together with its divider chain give a timeout T_{TO} of typically 10ms. For programming a different T_{TO}, an approximation for calculating component values is given by the formula:

$$T_{TO} = \left[0.75 + \frac{(32 + C_1) \cdot 1.6}{5.5 + \frac{V_{DD} - 0.8}{R_1}} \right] \cdot 1.024$$

$R_{1\,min.} = 10\ k\Omega$, $C_{1\,max.} = 1\ \mu F$

If R_1 is in MΩ and C_1 in pF, T_{TO} will be in ms.

Thus, a resistor decreases and a capcitor increases the interval to timeout. By using both external components, excellent temperature stability of T_{TO} can be achieved. With $\overline{TCL}$ tied to either V_{DD} or V_{SS}, a precise square wave of period 2 x T_{TO} is generated at the output $\overline{TO}$. The oscillator and watchdog timer run so long as the chip is powered with at least the minimum positive supply voltage specified (V_{ON}), and so long as V_{IN} remains above the level V_{RL} after a power-up sequence. If the timer function is not required, input $\overline{TCL}$ should be tied to output $\overline{TO}$ to give a simple voltage monitor (see Fig. 14).

Timer Clearing and $\overline{RES}$ Action

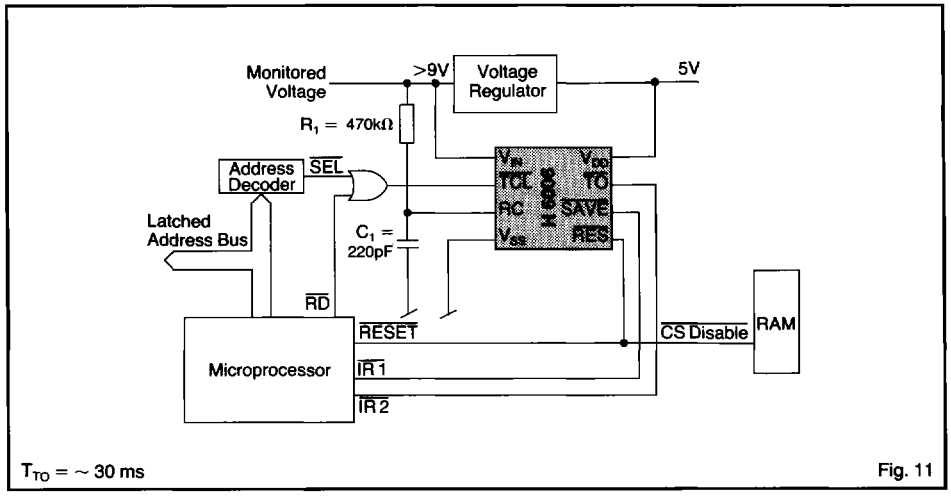
A negative edge or a negative pulse at the $\overline{TCL}$ input longer than 150ns will reset the timer and set $\overline{TO}$ high. If a further $\overline{TCL}$ signal edge or pulse is applied before T_{TO} timeout, $\overline{TO}$ will stay high and the timer will again be reset to zero (see Fig. 5). If no $\overline{TCL}$ signal is applied before the T_{TO} timeout, $\overline{TO}$ will start to generate a square wave of period 2 x T_{TO} starting with a low state. If no $\overline{TCL}$ signal is applied during the first low state of $\overline{TO}$, then the $\overline{RES}$ output will go low and stay low until the next $\overline{TCL}$ signal, or until a fresh power-up sequence.

Combined Voltage and Timer Action

The combination of voltage and timer action is illustrated by the sequence of events shown in Fig. 6. One timeout period after V_{IN} reached V_{SH}, during power-up, $\overline{RES}$ goes inactive high. No $\overline{TCL}$ pulse will have any effect until this power-on reset delay is completed. After completing the power-up sequence the watchdog timer starts acting. If no $\overline{TCL}$ pulse occurs, the timeout warning $\overline{TO}$ goes active low after one timeout period T_{TO}. After each subsequent timeout period without a timer clear pulse $\overline{TCL}$, $\overline{TO}$ changes its polarity providing a square wave signal. $\overline{RES}$ activates at the end of the first low state of the $\overline{TO}$ signal. A $\overline{TCL}$ pulse clears the watchdog timer and resets the $\overline{TO}$ and $\overline{RES}$ output inactive high again. A voltage drop below the V_{RL} level overrides the timer and immediately forces $\overline{RES}$ and $\overline{SAVE}$ active low and disables $\overline{TO}$. Any further $\overline{TCL}$ pulse has no effect until the next power-up sequence has completed.

Typical Applications

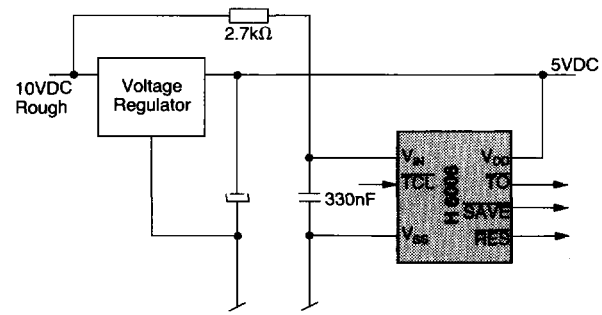
Microprocessor Watchdog with Power-On Reset and Voltage Monitor



T_{TO} = ~ 30 ms

Fig. 11

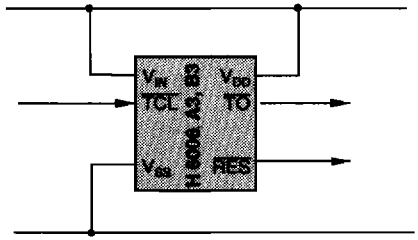
Voltage Monitor with Spike Suppression



Version A1 or B1

Fig. 12

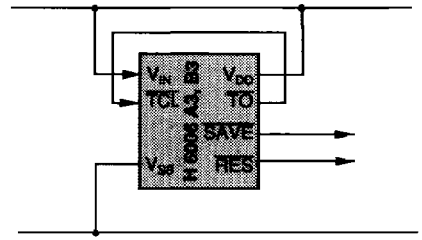
Watchdog and Power-On Reset



If only V_{DD} monitoring is used, (i.e. V_{IN} and V_{DD} common) then the version A3 or B3 with its constant thresholds are recommended. The power-on reset function is still available as the V_{DD} monitoring is active.

Fig. 13

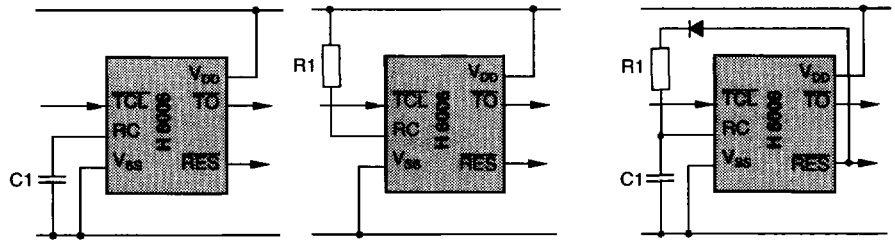
V_{DD} Monitoring and Power-On Reset



V_{IN} monitoring and watchdog function not used. Versions A3 and B3 only.

Fig. 14

External Programming of RC Oscillator



C1 increases T_{TO}

R1 shortens T_{TO}

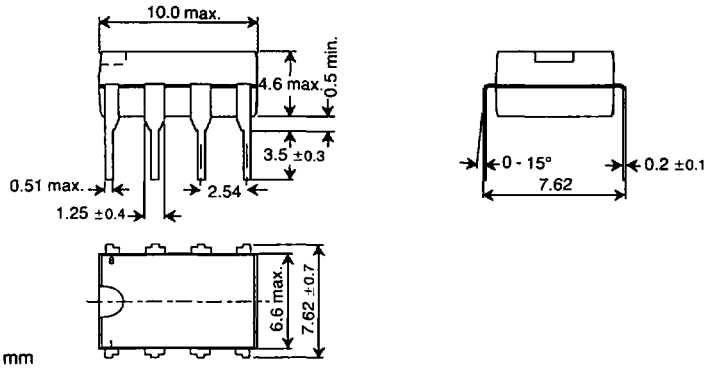
This circuit provides independent programming of both timeout period and power-on reset delay.

Note: using both external components R1 and C1 allows to achieve tighter timeout period tolerances.

Fig. 15

Package and Ordering Information

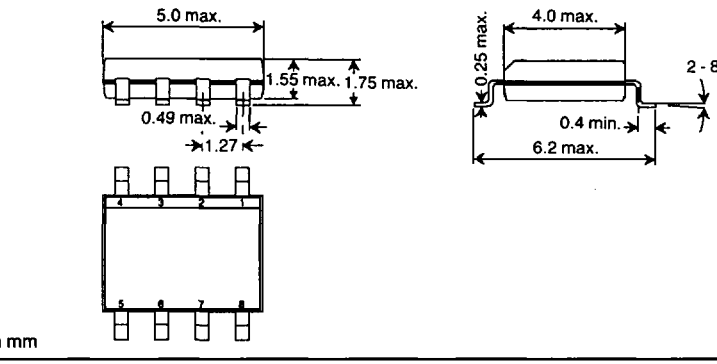
Dimensions of DIP8 Package



Dimensions in mm

Fig. 16

Dimensions of SO8 Package



Dimensions in mm

Fig. 17

Ordering Information

Industrial temperature range (−40 to +85°C)

Type[1]	Package
H 6006 nn 8P	DIP8
H 6006 nn 8S	SO8

Extended temperature range (−40 to +125°C)

Type[1]	Package
H 6006 nnX 8P	DIP8*
H 6006 nnX 8S	SO8*

[1] nn stands for the versions A1*, B1, A2, B2, A3, B3

* Non-stock items

Chip form on request

The H 6006 standard versions are as shown in the electrical specifications:

H 6006 n1
H 6006 n2
H 6006 n3

The device has the option of open drain or push-pull outputs:

H 6006 An	open drain outputs
H 6006 Bn	push-pull outputs

When ordering please specify complete part number.