

## Features

- **Wide 5V to 12V Supply Voltage**
- **Power-On-Reset Monitoring on VCC**
- **Excellent Output Voltage Regulations**
  - **0.6V Internal Reference**
  - **±0.6% Over-Temperature Range**
- **Integrated Soft-Start**
- **Voltage Mode PWM Operation with External Compensation**
- **Up to 90% Duty Ratio for Fast Transient Response**
- **Constant Switching Frequency**
  - **300kHz ±10%**
- **Integrated Bootstrap Forward P-CH MOSFET**
- **50% Under-Voltage Protection**
- **125% Over-Voltage Protection**
- **Adjustable Over-Current Protection Threshold**
  - **Using the  $R_{DS(ON)}$  of Low-Side MOSFET**
- **Shutdown Control by COMP**
- **Power Good Monitoring (TDFN-10 3mmx3mm Package Only)**
- **Remote Feedback Sense for Excellent Output Voltage (TDFN-10 3mmx3mm Package Only)**
- **TDFN3x3-10 Package**
- **Lead Free and Green Devices Available (RoHS Compliant)**

## Applications

- **Graphic Cards**
- **DSL, Switch HUB**
- **Wireless Lan**
- **Notebook Computer**
- **Mother Board**
- **LCD Monitor/TV**

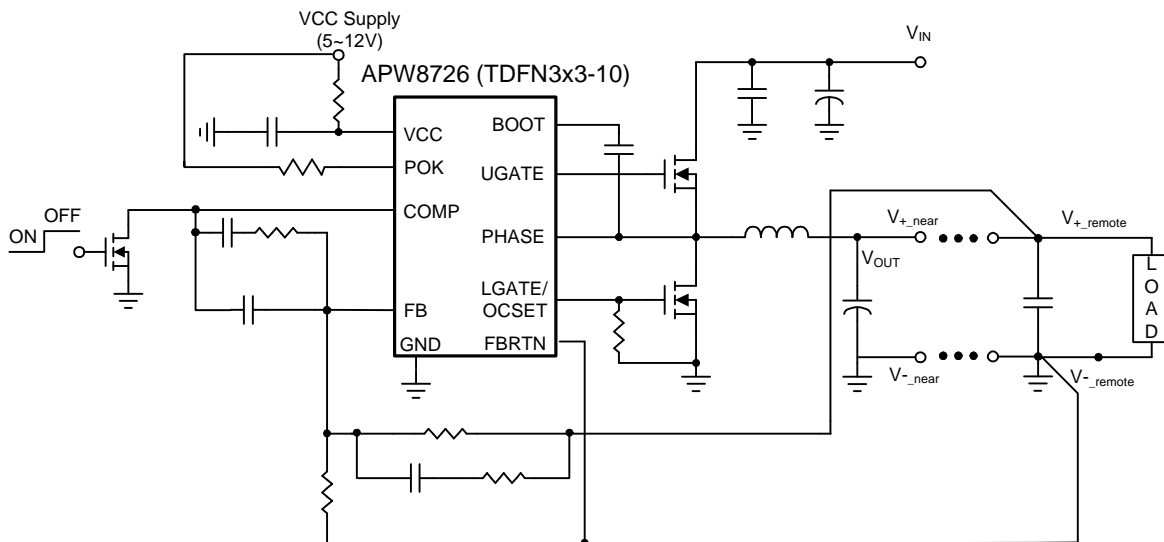
## General Description

The APW8726 is a voltage mode, fixed 300kHz switching frequency, synchronous buck converter. The APW8726 allows wide input voltage that is either a single 5-12V or two supply voltage(s) for various applications. A power-on-reset (POR) circuit monitors the VCC supply voltage to prevent wrong logic controls. A built-in soft-start circuit prevents the output voltages from overshoot as well as limits the input current. An internal 0.6V temperature-compensated reference voltage with high accuracy is designed to meet the requirement of low output voltage applications. The APW8726 provides excellent output voltage regulations against load current variation. APW8726 is built in remote sense function for applications that require remote sense. (TDFN-10 3mmx3mm Package Only)

The controller's over-current protection monitors the output current by using the voltage drop across the RDS (ON) of low-side MOSFET, eliminating the need for a current sensing resistor that features high efficiency and low cost. In addition, the APW8726 also integrates excellent protection functions. The over-voltage protection (OVP), under-voltage protection (UVP). OVP circuit which monitors the FB voltage to prevent the PWM output from over voltage, and UVP circuit which monitors the FB voltage to prevent the PWM output from under voltage or short circuit. The APW8726 is available in TDFN3x3-10 packages

ANPEC reserves the right to make changes to improve reliability or manufacturability without notice, and advise customers to obtain the latest version of relevant information to verify before placing orders.

## Simplified Application Circuit

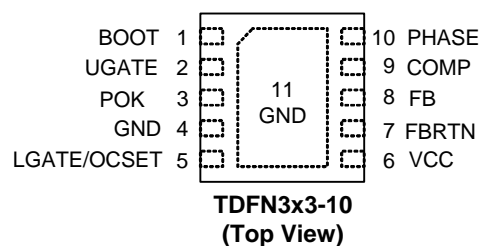


## Ordering and Marking Information

<p>APW8726    □□□ - □□□</p> <p>Assembly Material</p> <p>Handling Code</p> <p>Temperature Range</p> <p>Package Code</p>	<p>Package Code QB : TDFN3x3-10</p> <p>Operating Ambient Temperature Range I : -40 to 85 °C</p> <p>Handling Code TR : Tape &amp; Reel</p> <p>Assembly Material G : Halogen and Lead Free Device</p>
<p>APW8726 QB :</p> <div style="border: 1px solid black; padding: 2px; display: inline-block;"> <p>APW 8726 XXXXX</p> </div>	<p>XXXXX - Date Code</p>

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

## Pin Configuration



## Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Rating	Unit	
V <sub>VCC</sub>	VCC Supply Voltage (VCC to GND)	-0.3 ~ 16	V	
V <sub>BOOT</sub>	BOOT Supply Voltage (BOOT to PHASE)	-0.3 ~ 16	V	
	BOOT Supply Voltage (BOOT to GND)	-0.3 ~ 32	V	
V <sub>UGATE</sub>	UGATE Voltage (UGATE to PHASE)	> 20ns	-0.3 ~ V <sub>BOOT</sub> +0.3	V
		< 20ns	-5 ~ V <sub>BOOT</sub> +5	V
V <sub>LGATE</sub>	LGATE Voltage (LGATE to GND)	> 20ns	-0.3 ~ V <sub>VCC</sub> +0.3	V
		< 20ns	-5 ~ V <sub>VCC</sub> +5	V
V <sub>PHASE</sub>	PHASE Voltage (PHASE to GND)	> 20ns	-0.3 ~ 16	V
		< 20ns	-5 ~ 25	V
	FB ,COMP and FBRTN to GND	-0.3 ~ 7	V	
	POK to GND	-0.3~V <sub>CC</sub> +0.3	V	
T <sub>J</sub>	Maximum Junction Temperature	150	°C	
T <sub>STG</sub>	Storage Temperature	-65 ~ 150	°C	
T <sub>SDR</sub>	Maximum Lead Soldering Temperature, 10 Seconds	260	°C	

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Thermal Characteristics

Symbol	Parameter	Typical Value	Unit
θ <sub>JA</sub>	Thermal Resistance -Junction to Ambient <sup>(Note 2)</sup> TDFN3x3-10	55	°C/W

Note 2: θ<sub>JA</sub> is measured with the component mounted on a high effective thermal conductivity test board in free air.

## Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V <sub>VCC</sub>	VCC Supply Voltage (VCC to GND)	4.5 ~ 13.2	V
V <sub>OUT</sub>	Converter Output Voltage for APW8726	0.6 ~ 5	V
V <sub>IN</sub>	Converter Input Voltage	3~13.2	V
I <sub>OUT</sub>	Converter Output Current	0 ~ 25	A
T <sub>A</sub>	Ambient Temperature	-40 ~ 85	°C
T <sub>J</sub>	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the application circuit for further information.

## Electrical Characteristics

Refer to the typical application circuit. These specifications apply over  $V_{VCC} = 12V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = 25^{\circ}C$ .

Symbol	Parameter	Test Conditions	APW8726			Unit
			Min.	Typ.	Max.	
<b>INPUT SUPPLY VOLTAGE AND CURRENT</b>						
$I_{VCC}$	VCC Supply Current (Shutdown Mode)	UGATE and LGATE open; COMP=GND	-	-	550	$\mu A$
	VCC Supply Current	UGATE and LGATE open	-	2.5	10	mA
<b>POWER-ON-RESET(POR)</b>						
	Rising VCC POR Threshold		3.8	4.1	4.4	V
	VCC POR Hysteresis		0.3	0.5	0.6	V
<b>OSCILLATOR</b>						
$F_{OSC}$	Oscillator Frequency		270	300	330	kHz
$\Delta V_{OSC}$	Oscillator Sawtooth Amplitude <sup>(Note 4)</sup>	(1.2V~2.7V typical)	-	1.5	-	V
$D_{MAX}$	Maximum Duty Cycle		-	-	90	%
<b>REFERENCE</b>						
$V_{REF}$	Reference Voltage	$T_A = -40 \sim 85^{\circ}C$	0.596	0.6	0.604	V
<b>ERROR AMPLIFIER</b>						
	Open-Loop GAIN <sup>(Note 4)</sup>	$R_L = 10k\Omega$ , $C_L = 10pF$	-	90	-	dB
	Open-Loop Bandwidth <sup>(Note 4)</sup>	$R_L = 10k\Omega$ , $C_L = 10pF$	-	20	-	MHz
	FB Input Leakage Current	$V_{FB} = 0.6V$	-	-	0.1	$\mu A$
<b>GATE DRIVERS</b>						
	High-side Gate Driver Source Current	$V_{BOOT} = 12V$ , $V_{UGATE-PHASE} = 6V$	-	1.0	-	A
	High-side Gate Driver Sink Current	$V_{BOOT} = 12V$ , $V_{UGATE-PHASE} = 6V$	-	1.1	-	
	Low-side Gate Driver Source Current	$V_{VCC} = 12V$ , $V_{LGATE-GND} = 6V$	-	1.8	-	
	Low-side Gate Driver Sink Current	$V_{VCC} = 12V$ , $V_{LGATE-GND} = 6V$	-	2.0	-	
$T_D$	Dead-time <sup>(Note 4)</sup>		-	30	-	ns
<b>PROTECTIONS</b>						
$V_{FB\_UV}$	FB Under-Voltage Protection Trip Point	Percentage of $V_{REF}$	45	50	55	%
	Under-Voltage Debounce Interval		-	2	-	$\mu s$
	Under-Voltage Protection Enable Delay		-	4	-	ms
$V_{FB\_OV}$	FB Over-Voltage Protection Rising Threshold	$V_{FB}$ rising	120	125	130	%
	FB Over-Voltage Protection Falling Threshold	$V_{FB}$ falling	100	105	110	%
	Over-Voltage Debounce Interval		-	2	-	$\mu s$
$V_{OCP\_MAX}$	Built-in Maximum OCP Voltage		-	1200	-	mV
$I_{OCSET}$	OCSET Current Source		23	25	27	$\mu A$
<b>SOFT-START</b>						
$V_{DISABLE}$	Shutdown Threshold of $V_{COMP}$		-	-	0.4	V
$T_{SS}$	Internal Soft-Start Interval		-	4	-	ms

## Electrical Characteristics (Cont.)

Refer to the typical application circuit. These specifications apply over  $V_{VCC} = 12V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$ , unless otherwise noted. Typical values are at  $T_A = 25^{\circ}C$ .

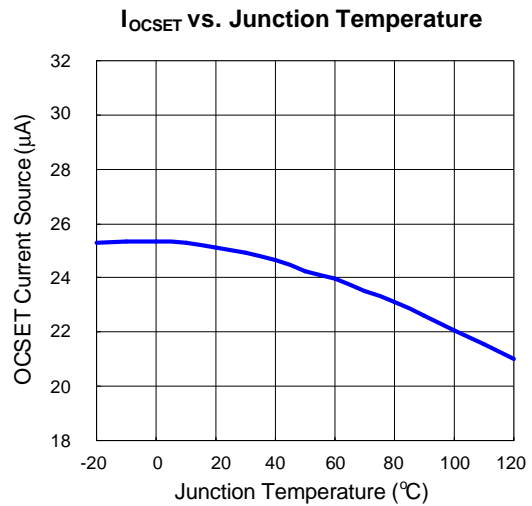
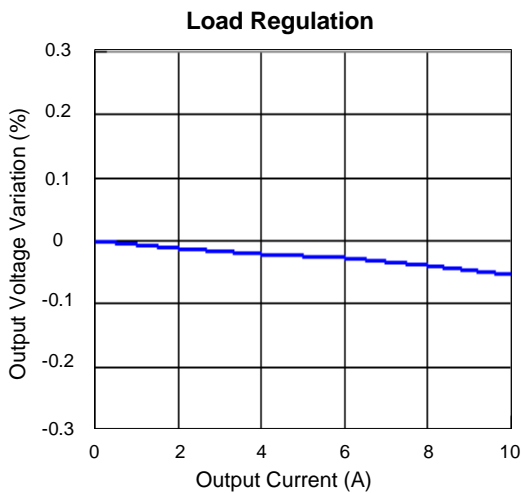
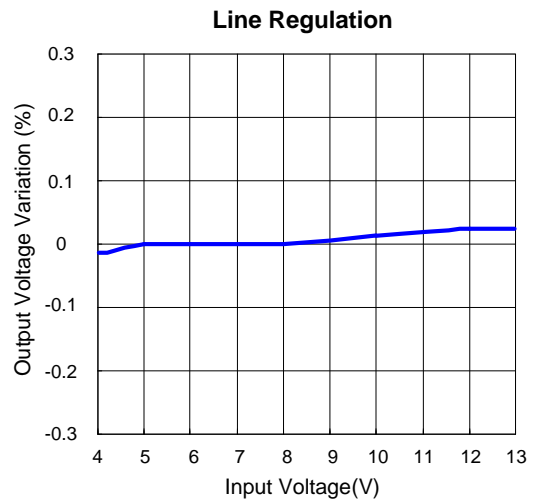
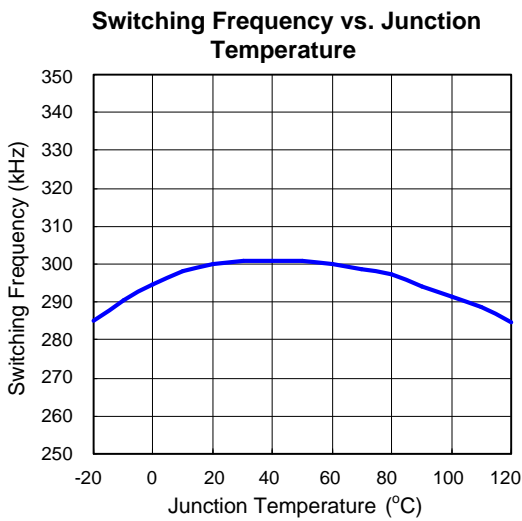
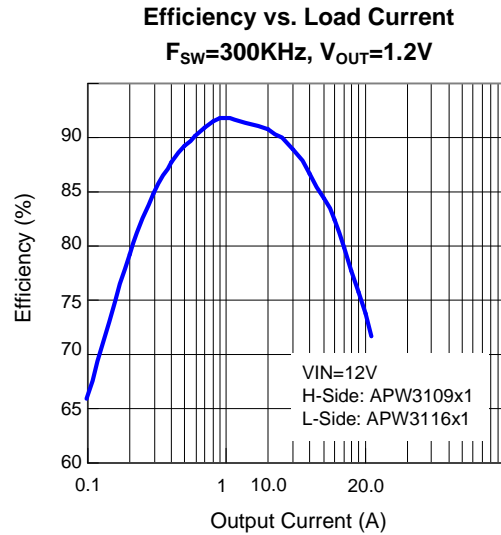
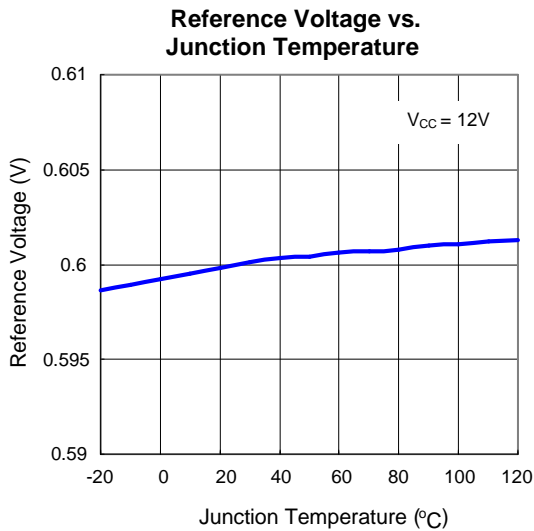
Symbol	Parameter	Test Conditions	APW8726			Unit
			Min.	Typ.	Max.	
<b>Remote Sense</b>						
$I_{FBRTN}$	Remote sense source current		-	12	-	$\mu A$
<b>POWER GOOD (Only for TDFN3 8-10 Package)</b>						
$I_{POK}$	POK Leakage Current	$V_{POK}=5V$	-	0.1	1	$\mu A$
	POK Threshold	VFB is from low to target value (POK Goes High)	85	90	95	%
		VFB Falling, POK Goes Low	45	50	55	%
		VFB Rising, POK Goes Low	120	125	130	%
	POK Delay Time		-	3	-	ms

Note 4: Guaranteed by design, not production tested.

## Pin Description

PIN		FUNCTION
NO.	NAME	
TDFN3x3-10		
1	BOOT	This pin provides the bootstrap voltage to the high-side gate driver for driving the N-channel MOSFET. An external capacitor from PHASE to BOOT, an internal switch generates the bootstrap voltage for the high-side gate driver (UGATE).
2	UGATE	High-side Gate Driver Output. This pin is the gate driver for high-side MOSFET.
4	GND	Signal and Power ground. Connecting this pin to system ground.
5	LGATE/O CSET	Low-side Gate Driver Output and Over-Current Setting Input. This pin is the gate driver for low-side MOSFET. It also used to set the maximum inductor current. Refer to the section in "Function Description" for detail.
6	VCC	Power Supply Input. Connect a nominal 5V to 12V power supply voltage to this pin. A power-on reset function monitors the input voltage at this pin. It is recommended that a decoupling capacitor (1 to 10 $\mu$ F) be connected to GND for noise decoupling.
8	FB	Feedback Input of Converter. The converter senses feedback voltage via FB and regulates the FB voltage at 0.6V/0.8V. Connecting FB with a resistor-divider from the output sets the output voltage of the converter.
9	COMP	This is a multiplexed pin. During soft-start and normal converter operation, this pin represents the output of the error amplifier. It is used to compensate the regulation control loop in combination with the FB pin. Pulling COMP low ( $V_{\text{DISABLE}} = 0.4\text{V max.}$ ) will shut down the controller. When the pull-down device is released, the COMP pin will start to rise. When the COMP pin rises above the $V_{\text{DISABLE}}$ trip point, the APW8726 will begin a new initialization and soft-start cycle.
10	PHASE	This pin is the return path for the high-side gate driver. Connecting this pin to the high-side MOSFET source and connect a capacitor to BOOT for the bootstrap voltage. This pin is also used to monitor the voltage drop across the low-side MOSFET for over-current protection.
3	POK	POK is an open drain output used to indicate the status of the output voltage. Connect the POK pin to 5 to 12V through a pull-high resistor.
7	FBRTN	FB Return Ground. This pin is the negative node of the remote voltage sensing.
11 (Exposed Pad)	GND	Thermal Pad. Connect this pad to the system ground plan for good thermal conductivity.

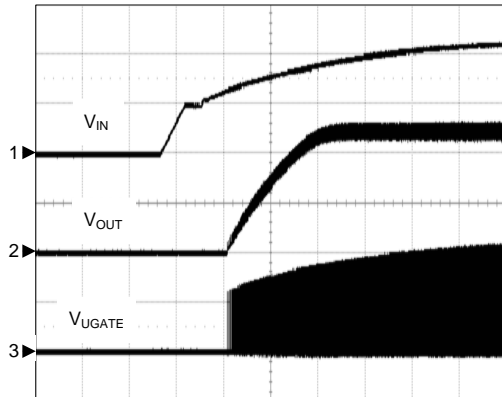
## Typical Operating Characteristics



## Operating Waveforms

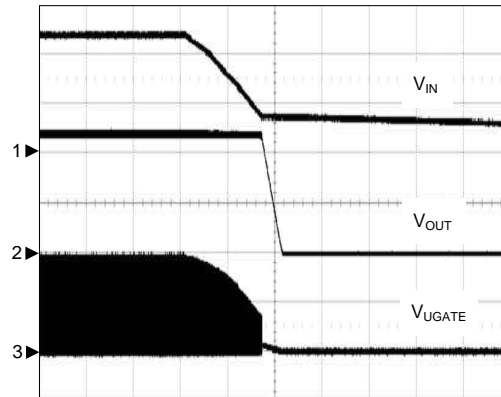
Refer to the typical application circuit. The test condition is  $V_{IN}=12V$ ,  $T_A=25^{\circ}C$  unless otherwise specified.

Power On



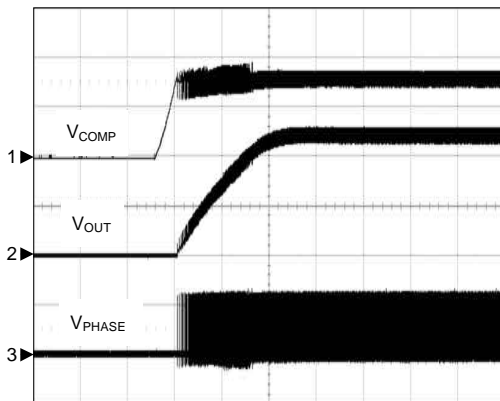
CH1:  $V_{IN}$ , 5V/Div  
 CH2:  $V_{OUT}$ , 500mV/Div  
 CH3:  $V_{UGATE}$ , 10V/Div  
 TIME: 1ms/Div

Power Off



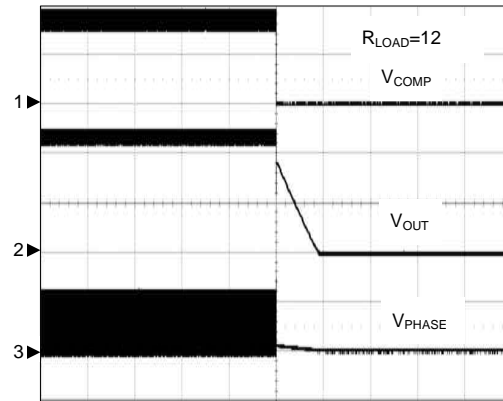
CH1:  $V_{IN}$ , 5V/Div  
 CH2:  $V_{OUT}$ , 500mV/Div  
 CH3:  $V_{UGATE}$ , 10V/Div  
 TIME: 50ms/Div

Enable



CH1:  $V_{COMP}$ , 1V/Div  
 CH2:  $V_{OUT}$ , 500mV/Div  
 CH3:  $V_{PHASE}$ , 10V/Div  
 TIME: 1ms/Div

Shutdown



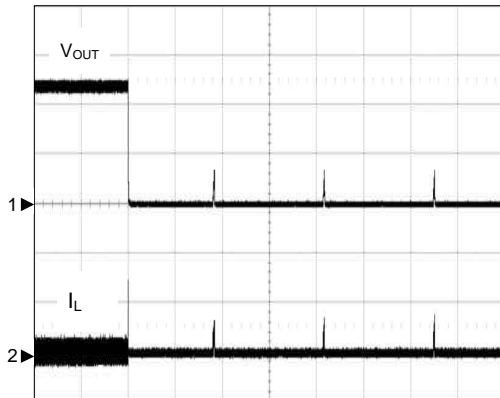
CH1:  $V_{COMP}$ , 1V/Div  
 CH2:  $V_{OUT}$ , 500mV/Div  
 CH3:  $V_{PHASE}$ , 10V/Div  
 TIME: 10ms/Div



## Operating Waveforms

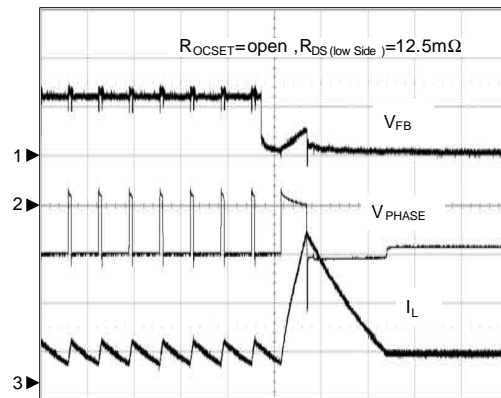
Refer to the typical application circuit. The test condition is  $V_{IN}=12V$ ,  $T_A=25^{\circ}C$  unless otherwise specified.

Over-Current Protection



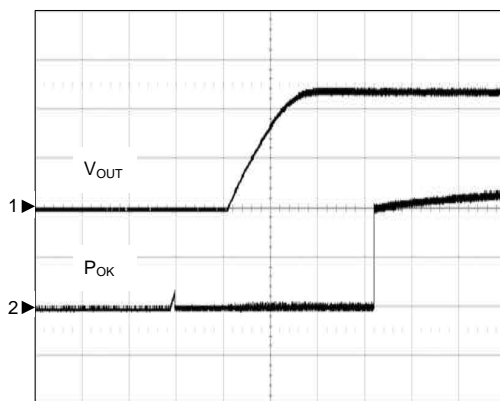
CH1:  $V_{OUT}$ , 500mV/Div  
 CH2:  $I_L$ , 10A/Div  
 TIME: 20ms/Div

Under-Voltage Protection



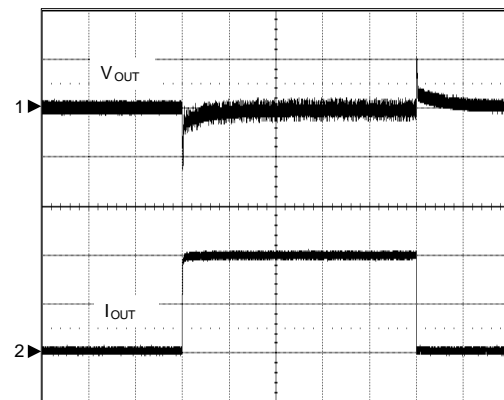
CH1:  $V_{FB}$ , 200mV/Div  
 CH2:  $V_{PHASE}$ , 10V/Div  
 CH3:  $I_L$ , 10A/Div  
 TIME: 10us/Div

Power OK



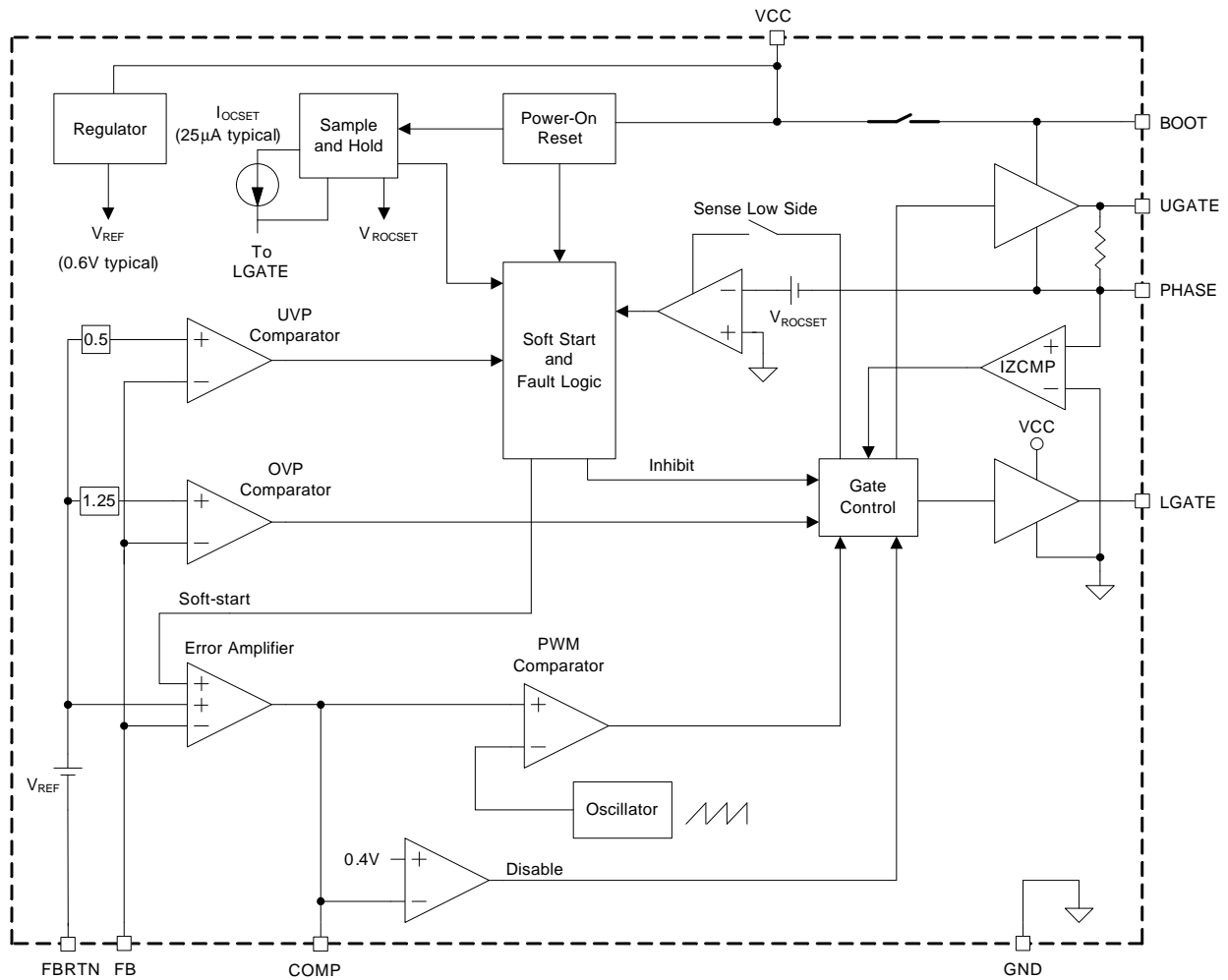
CH1:  $V_{OUT}$ , 500mV/Div  
 CH1:  $P_{OK}$ , 5V/Div  
 TIME: 1ms/Div

Load Transient

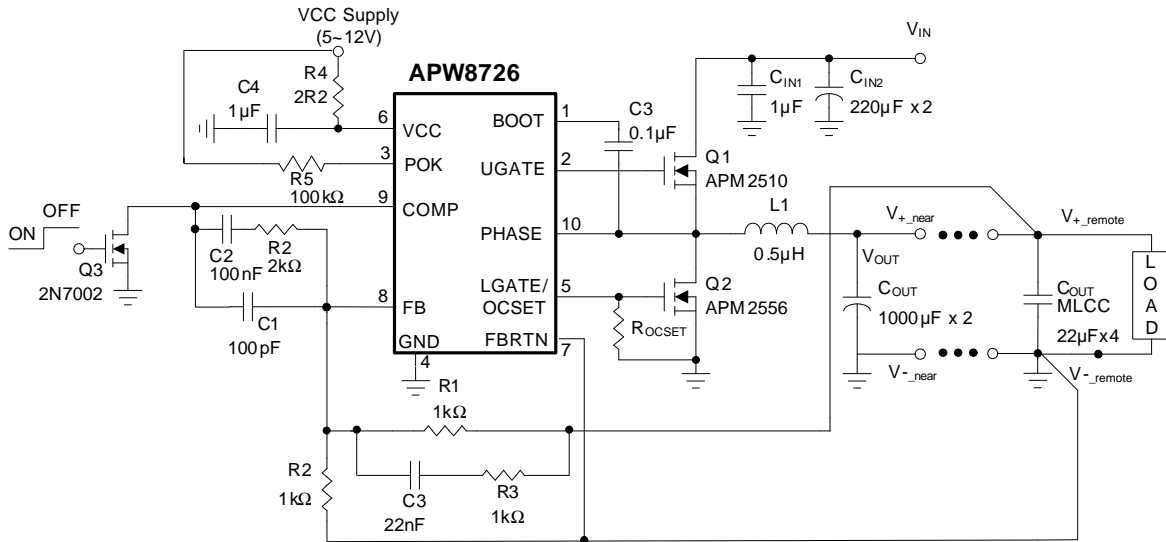


CH1:  $V_{OUT}$ , 50mV/Div, AC  
 CH2:  $I_{OUT}$ , 5A/Div  
 TIME: 200us/Div

Block Diagram



## Typical Application Circuit



Note: Power OK Indicator (POK) (only for TDFN3x3-10 package).

## Function Description

### Power-On-Reset (POR)

The Power-On-Reset (POR) function of APW8726 continually monitors the input supply voltage (VCC) and ensures that the IC has sufficient supply voltage and can work well. The POR function initiates a soft-start process while the VCC voltage just exceeds the POR threshold; the POR function also inhibits the operations of the IC while the VCC voltage falls below the POR threshold.

### Soft-Start

The APW8726 builds in a soft-start function about 1.5ms (Typ.) interval, which controls the output voltage rising as well as limiting the current surge at the start-up. During soft-start, an internal ramp voltage connected to the one of the positive inputs of the error amplifier replaces the reference voltage (0.6V typical) until the ramp voltage reaches the reference voltage. The soft-start circuit interval is shown as figure 1.

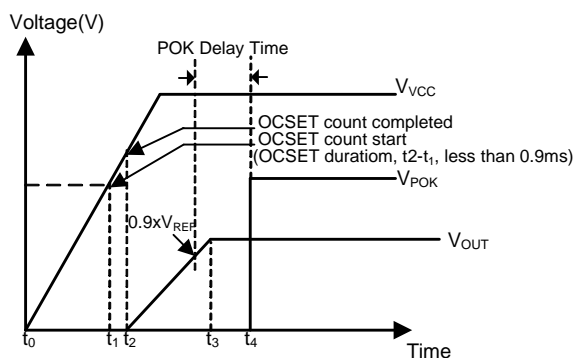


Figure 1. Soft-Start Interval

### Over-Current Protection of the PWM Converter

The over-current function protects the switching converter against over-current or short-circuit conditions. The controller senses the inductor current by detecting the drain-to-source voltage which is the product of the inductor's current and the on-resistance of the low-side MOSFET during its on-state. This method enhances the converter's efficiency and reduces cost by eliminating a current sensing resistor required.

A resistor ( $R_{OCSET}$ ), connected from the LGATE/OCSET to GND, programs the over-current trip level. Before the IC initiates a soft-start process, an internal current source,  $I_{OCSET}$  (25 $\mu$ A typical), flowing through the  $R_{OCSET}$  develops a voltage ( $V_{ROCSET}$ ) across the  $R_{OCSET}$ . The device holds  $V_{ROCSET}$  and stops the current source  $I_{OCSET}$  during normal operation. When the voltage across the low-side MOSFET exceeds the  $V_{ROCSET}$ , the APW8726 turns off the high-side and low-side MOSFET, and the device will enter hiccup mode until the over-current phenomenon is released.

For avoid large inductor current occurring in short circuit before power on, the controller reduces internal current source,  $I_{OCSET}$ , to half during soft start time. It means that when APW8726 is in soft start interval, the internal current source,  $I_{OCSET}$ , is only 12.5 $\mu$ A (typical).

The APW8726 has an internal OCP voltage,  $V_{OCP\_MAX}$ , and the value is 1.2V (typical). When the  $R_{OCSET} \times I_{OCSET}$  exceed 1.2V or the  $R_{OCSET}$  is floating or not connected, the  $V_{ROCSET}$  will be the default value 1.2V. The over current threshold would be 1.2V across low-side MOSFET. The threshold of the valley inductor current-limit is therefore given by:

$$I_{LIMIT} = \frac{2 \times I_{OCSET} \times R_{OCSET}}{R_{DS(ON)}(low - side)}$$

For the over-current is never occurred in the normal operating load range, the variation of all parameters in the above equation should be considered:

- The  $R_{DS(ON)}$  of low-side MOSFET is varied by temperature and gate to source voltage. Users should determine the maximum  $R_{DS(ON)}$  by using the manufacturer's datasheet.
- The minimum  $I_{OCSET}$  (23 $\mu$ A) and minimum  $R_{OCSET}$  should be used in the above equation.
- Note that the  $I_{LIMIT}$  is the current flow through the low-side MOSFET;  $I_{LIMIT}$  must be greater than valley inductor current which is output current minus the half of inductor ripple current.

$$I_{LIMIT} > I_{OUT(MAX)} - \frac{\Delta I}{2}$$

Where  $\Delta I$  = output inductor ripple current

- The overshoot and transient peak current also should be considered.

## Function Description (Cont.)

### Under-Voltage Protection

The under-voltage function monitors the voltage on FB ( $V_{FB}$ ) by Under-Voltage (UV) comparator to protect the PWM converter against short-circuit conditions. When the  $V_{FB}$  falls below the falling UVP threshold ( $50\% V_{REF}$ ), a fault signal is internally generated and the device turns off high-side and low-side MOSFETs. The device will enter hiccup mode until the under-voltage phenomenon is released.

### Over-Voltage Protection (OVP) of the PWM Converter

The over-voltage protection monitors the FB voltage to prevent the output from over-voltage condition. When the output voltage rises above 125% of the nominal output voltage, the APW8726 turns off the high-side MOSFET and turns on the low-side MOSFET until the output voltage falls below the falling below 105%, the OVP comparator is disengaged and both high-side and low-side drivers turn off.

This OVP scheme only clamps the voltage overshoot and does not invert the output voltage when otherwise activated with a continuously high output from low-side MOSFET driver. It is a common problem for OVP schemes with a latch. Once an over-voltage fault condition is set, it can be reset by releasing COMP or toggling VCC power-on-reset signal.

### Shutdown and Enable

The APW8726 can be shut down or enabled by pulling low the voltage on COMP. The COMP is a dual-function pin. During normal operation, this pin represents the output of the error amplifier. It is used to compensate the regulation control loop in combination with the FB pin.

Pulling the COMP low ( $V_{DISABLE} = 0.4V$  maximum) places the controller into shutdown mode which UGATE and LGATE are pulled to PHASE and GND respectively.

When the pull-down device is released, the COMP voltage will start to rise. When the COMP voltage rises above the  $V_{DISABLE}$  threshold, the APW8726 will begin a new initialization and soft-start process.

### Adaptive Shoot-Through Protection of the PWM Converter

The gate drivers incorporate an adaptive shoot-through protection to prevent high-side and low-side MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to rise.

During turn-off the low-side MOSFET, the LGATE voltage is monitored until it is below 1.5V threshold, at which time the UGATE is released to rise after a constant delay. During turn-off of the high-side MOSFET, the UGATE-to-PHASE voltage is also monitored until it is below 1.5V threshold, at which time the LGATE is released to rise after a constant delay.

### Remote Sense

APW8726 has a FBRTN pin for applications that require remote sense. In some applications where high current, low voltage and accurate output voltage regulation are needed, FBRTN can sense the negative terminal of remote load capacitor directly, and improve output voltage drop which is due to the board interconnection loss.

### Power OK Indicator

The APW8726 features an open-drain POK output pin to indicate one of the IC's working statuses including soft-start, under-voltage fault, over-current fault.

In normal operation, when the output voltage rises 90% of its target value, the POK goes high. When the output voltage outruns 50% or 125% of the target voltage, POK signal will be pulled low immediately.

## Application Information

### Output Voltage Selection

The output voltage can be programmed with a resistive divider. Use 1% or better resistors for the resistive divider is recommended. The FB pin is the inverter input of the error amplifier, and the reference voltage is 0.6V. The output voltage is determined by:

$$V_{OUT} = 0.6 \times \left( 1 + \frac{R_1}{R_2} \right)$$

Where R1 is the resistor connected from V<sub>OUT</sub> to FB and R2 is the resistor connected from FB to the GND.

### Output Capacitor Selection

The selection of C<sub>OUT</sub> is determined by the required effective series resistance (ESR) and voltage rating rather than the actual capacitance requirement. Therefore, selecting high performance low ESR capacitors is intended for switching regulator applications. In some applications, multiple capacitors have to be paralleled to achieve the desired ESR value. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

### Input Capacitor Selection

The input capacitor is chosen based on the voltage rating and the RMS current rating. For reliable operation, select the capacitor voltage rating to be at least 1.3 times higher than the maximum input voltage. The maximum RMS current rating requirement is approximately I<sub>OUT</sub>/2 where I<sub>OUT</sub> is the load current. During power up, the input capacitors have to handle large amount of surge current. If tantalum capacitors are used, make sure they are surge tested by the manufactures. If in doubt, consult the capacitors manufacturer.

For high frequency decoupling, a ceramic capacitor between 0.1µF to 1µF can connect between VCC and ground pin.

### Inductor Selection

The inductance of the inductor is determined by the output voltage requirement. The larger the inductance, the lower the inductor's current ripple. This will translate into

lower output ripple voltage. The ripple current and ripple voltage can be approximated by:

$$I_{RIPPLE} = \frac{V_{IN} - V_{OUT}}{F_{SW} \times L} \times \frac{V_{OUT}}{V_{IN}}$$

where Fs is the switching frequency of the regulator.

$$\Delta V_{OUT} = I_{RIPPLE} \times ESR$$

A tradeoff exists between the inductor's ripple current and the regulator load transient response time. A smaller inductor will give the regulator a faster load transient response at the expense of higher ripple current and vice versa. The maximum ripple current occurs at the maximum input voltage. A good starting point is to choose the ripple current to be approximately 30% of the maximum output current.

Once the inductance value has been chosen, selecting an inductor is capable of carrying the required peak current without going into saturation. In some types of inductors, especially core that is make of ferrite, the ripple current will increase abruptly when it saturates. This will result in a larger output ripple voltage.

### PWM Compensation

The output LC filter of a step down converter introduces a double pole, which contributes with -40dB/decade gain slope and 180 degrees phase shift in the control loop. A compensation network among COMP, FB, and V<sub>OUT</sub> should be added. The compensation network is shown in Figure 5. The output LC filter consists of the output inductor and output capacitors. The transfer function of the LC filter is given by:

$$F_{ESR} = \frac{1}{2 \times \pi \times ESR \times C_{OUT}}$$

The F<sub>LC</sub> is the double poles of the LC filter, and F<sub>ESR</sub> is the zero introduced by the ESR of the output capacitor.

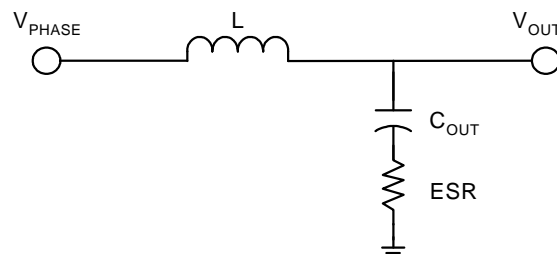


Figure 2. The Output LC Filter

### Application Information(Cont.)

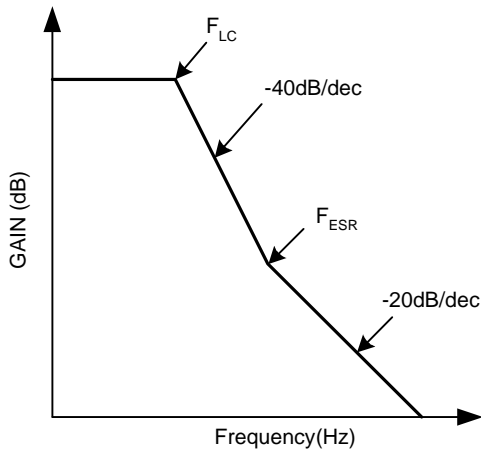


Figure 3. The LC Filter GAIN and Frequency

The PWM modulator is shown in Figure 4. The input is the output of the error amplifier and the output is the PHASE node. The transfer function of the PWM modulator is given by:

$$GAIN_{PWM} = \frac{V_{IN}}{\Delta V_{OSC}}$$

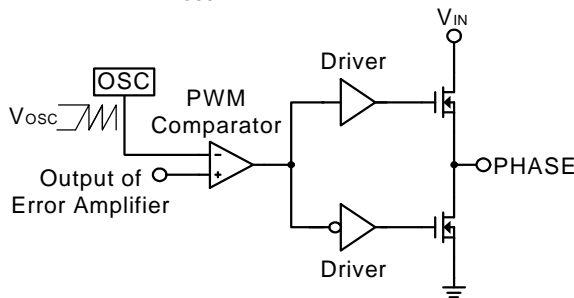


Figure 4. The PWM Modulator

The compensation network is shown in Figure 5. It provides a close loop transfer function with the highest zero crossover frequency and sufficient phase margin. The transfer function of error amplifier is given by:

$$GAIN_{AMP} = \frac{V_{COMP}}{V_{OUT}} = \frac{1}{sC1} // \left( R2 + \frac{1}{sC2} \right) / \left( R1 // \left( R3 + \frac{1}{sC3} \right) \right)$$

$$= \frac{R1+R3}{R1 \times R3 \times C1} \times \left( s + \frac{1}{R2 \times C2} \right) \times \left( s + \frac{1}{(R1+R3) \times C3} \right) / \left( s \left( s + \frac{C1+C2}{R2 \times C1 \times C2} \right) \times \left( s + \frac{1}{R3 \times C3} \right) \right)$$

The poles and zeros of the transfer function are:

$$F_{Z1} = \frac{1}{2 \times \pi \times R2 \times C2}$$

$$F_{Z2} = \frac{1}{2 \times \pi \times (R1+R3) \times C3}$$

$$F_{P1} = \frac{1}{2 \times \pi \times R2 \times \left( \frac{C1 \times C2}{C1+C2} \right)}$$

$$F_{P2} = \frac{1}{2 \times \pi \times R3 \times C3}$$

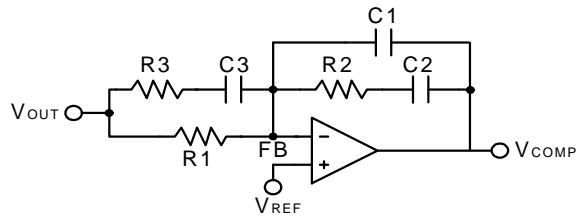


Figure 5. Compensation Network

The closed loop gain of the converter can be written as:

$$GAIN_{LC} \times GAIN_{PWM} \times GAIN_{AMP}$$

Figure 6. shows the asymptotic plot of the closed loop converter gain, and the following guidelines will help to design the compensation network. Using the below guidelines should give a compensation similar to the curve plotted. A stable closed loop has a -20dB/decade slope and a phase margin greater than 45 degree.

1. Choose a value for R1, usually between 1K and 5K.
2. Select the desired zero crossover frequency

$$F_O: (1/5 \sim 1/10) \times F_s > F_O > F_{ESR}$$

Use the following equation to calculate R2:

$$R2 = \frac{\Delta V_{OSC}}{V_{IN}} \times \frac{F_O}{F_{LC}} \times R1$$

3. Place the first zero  $F_{Z1}$  before the output LC filter double pole frequency  $F_{LC}$ .

$$F_{Z1} = 0.75 \times F_{LC}$$

Calculate the C2 by the equation:

$$C2 = \frac{1}{2 \times \pi \times R2 \times F_{LC} \times 0.75}$$

### Application Information(Cont.)

4. Set the pole at the ESR zero frequency  $F_{ESR}$ :

$$F_{P1} = F_{ESR}$$

Calculate the C1 by the equation:

$$C1 = \frac{C2}{2 \times \pi \times R2 \times C2 \times F_{ESR} - 1}$$

5. Set the second pole  $F_{P2}$  at the half of the switching frequency and also set the second zero  $F_{Z2}$  at the output LC filter double pole  $F_{LC}$ . The compensation gain should not exceed the error amplifier open loop gain, check the compensation gain at  $F_{P2}$  with the capabilities of the error amplifier.

$$F_{P2} = 0.5 \times F_s$$

$$F_{Z2} = F_{LC}$$

Combine the two equations will get the following component calculations:

$$GAIN_{LC} = \frac{1 + s \times ESR \times C_{OUT}}{s^2 \times L \times C_{OUT} + s \times ESR \times C_{OUT} + 1}$$

The poles and zero of this transfer functions are:

$$F_{LC} = \frac{1}{2 \times \pi \times \sqrt{L \times C_{OUT}}}$$

$$R3 = \frac{R1}{\frac{F_s}{2 \times F_{LC}} - 1}$$

$$C3 = \frac{1}{\pi \times R3 \times F_s}$$

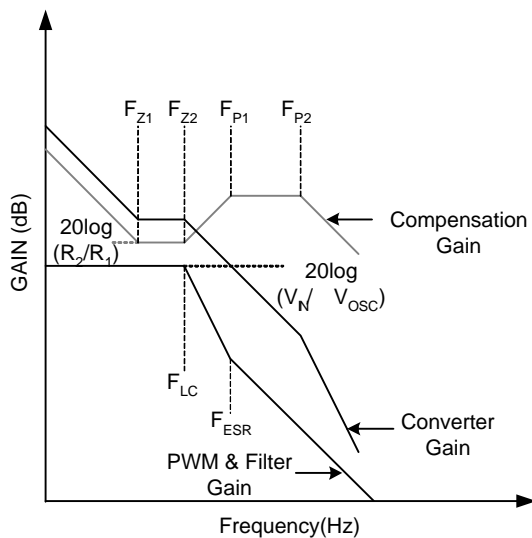


Figure 6. Converter Gain and Frequency

### MOSFET Selection

The selection of the N-channel power MOSFETs is determined by the  $R_{DS(ON)}$ , reverse transfer capacitance ( $C_{RSS}$ ), and maximum output current requirement. The losses in the MOSFETs have two components: conduction loss and transition loss. For the upper and lower MOSFET, the losses are approximately given by the following equations:

$$P_{UPPER} = I_{OUT}^2 (1 + TC)(R_{DS(ON)})D + (0.5)(I_{out})(V_{IN})(t_{sw})F_{SW}$$

$$P_{LOWER} = I_{OUT}^2 (1 + TC)(R_{DS(ON)})(1-D)$$

where  $I_{OUT}$  is the load current

TC is the temperature dependency of  $R_{DS(ON)}$

$F_{SW}$  is the switching frequency

$t_{sw}$  is the switching interval

D is the duty cycle

Note that both MOSFETs have conduction losses while the upper MOSFET includes an additional transition loss. The switching interval,  $t_{sw}$ , is the function of the reverse transfer capacitance  $C_{RSS}$ . Figure 7 illustrates the switching waveform internal of the MOSFET.

The  $(1+TC)$  term factors in the temperature dependency of the  $R_{DS(ON)}$  and can be extracted from the " $R_{DS(ON)}$  vs Temperature" curve of the power MOSFET.

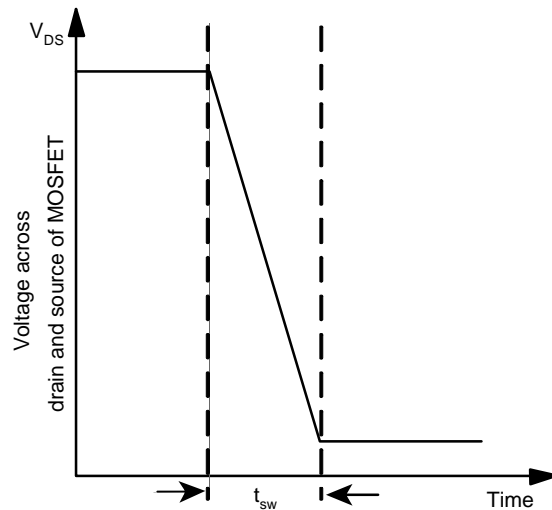


Figure 7. Switching Waveform Across MOSFET



## Application Information (Cont.)

### Layout Consideration

In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at 300kHz, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is free-wheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separate till combined using ground plane construction or single point grounding. Figure 8. illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed close together. Below is a checklist for your layout:

- The drain of the MOSFETs ( $V_{IN}$  and PHASE nodes) should be a large plane for heat sinking.
- The  $R_{OCSET}$  resistance should be placed near the IC as close as possible.

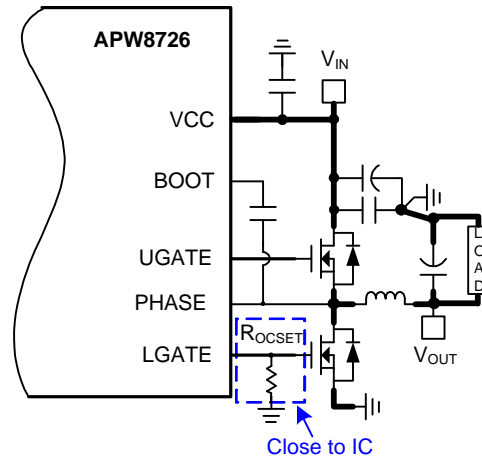
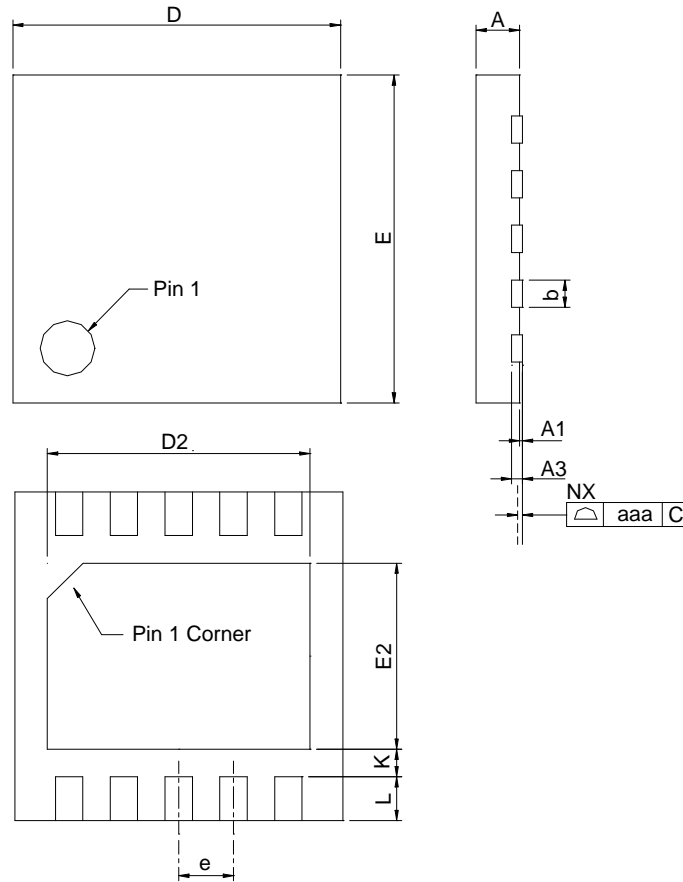


Figure 8. Layout Guidelines

- Keep the switching nodes (UGATE, LGATE, and PHASE) away from sensitive small signal nodes since these nodes are fast moving signals. Therefore, keep traces to these nodes as short as possible.
- The traces from the gate drivers to the MOSFETs (UG and LG) should be short and wide.
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.
- Decoupling capacitor, compensation component, the resistor dividers, and boot capacitors should be close their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placed near the drain).
- The input capacitor should be near the drain of the upper MOSFET; the output capacitor should be near the loads. The input capacitor GND should be close to the output capacitor GND and the lower MOSFET GND.

Package Information

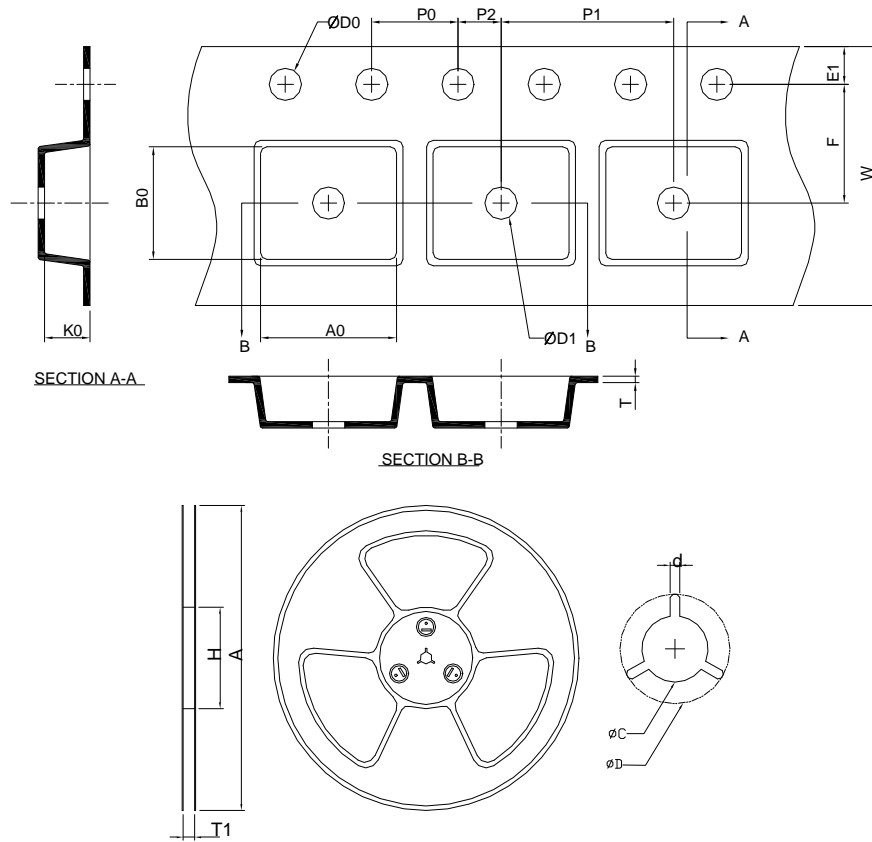
TDFN3x3-10



DIMENSIONS	TDFN3x3-10			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D2	2.20	2.70	0.087	0.106
E	2.90	3.10	0.114	0.122
E2	1.40	1.75	0.055	0.069
e	0.50 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-229 VEED-5.

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
TDFN3x3-10	330.0 ±0.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0 ±0.30	1.75 ±0.10	5.5 ±0.05
	P0	P1	P2	D0	D1	T	A0	B0	K0
	4.0 ±0.10	8.0 ±0.10	2.0 ±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30 ±0.20	3.30 ±0.20	1.30 ±0.20

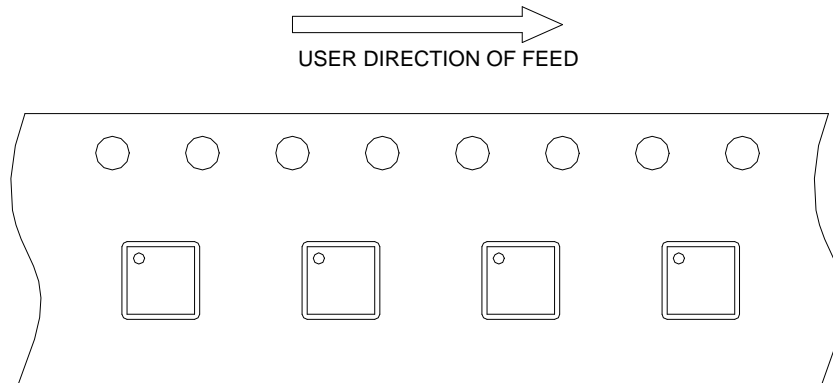
(mm)

Devices Per Unit

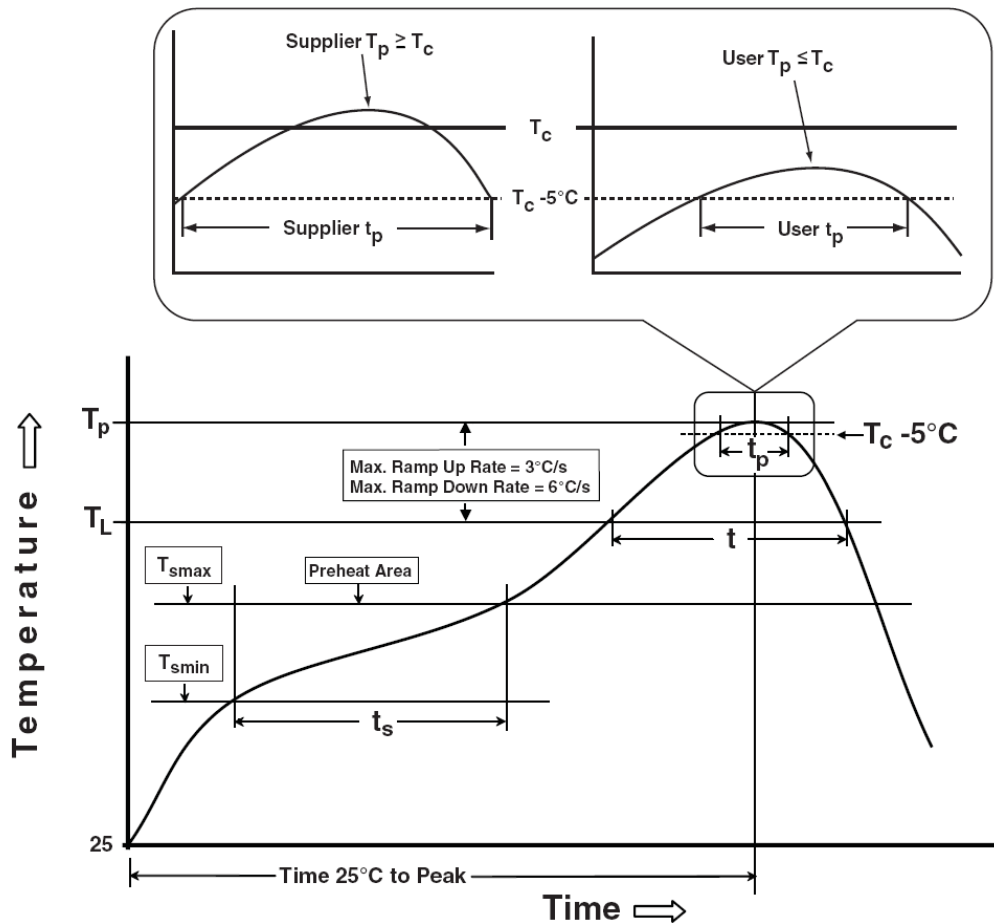
Package Type	Unit	Quantity
TDFN3x3-10	Tape & Reel	3000

# Taping Direction Information

TDFN3x3-10



## Classification Profile



## Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
<b>Preheat &amp; Soak</b>		
Temperature min ( $T_{smin}$ )	100 °C	150 °C
Temperature max ( $T_{smax}$ )	150 °C	200 °C
Time ( $T_{smin}$ to $T_{smax}$ ) ( $t_s$ )	60-120 seconds	60-120 seconds
Average ramp-up rate ( $T_{smax}$ to $T_p$ )	3 °C/second max.	3 °C/second max.
Liquidous temperature ( $T_L$ )	183 °C	217 °C
Time at liquidous ( $t_L$ )	60-150 seconds	60-150 seconds
Peak package body Temperature ( $T_p$ )*	See Classification Temp in table 1	See Classification Temp in table 2
Time ( $t_p$ )** within 5°C of the specified classification temperature ( $T_c$ )	20** seconds	30** seconds
Average ramp-down rate ( $T_p$ to $T_{smax}$ )	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature ( $T_p$ ) is defined as a supplier minimum and a user maximum.		
** Tolerance for time at peak profile temperature ( $t_p$ ) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures ( $T_c$ )

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> ≥350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures ( $T_c$ )

Package Thickness	Volume mm <sup>3</sup> <350	Volume mm <sup>3</sup> 350-2000	Volume mm <sup>3</sup> >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

## Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ $T_j=125^\circ\text{C}$
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM 2KV
MM	JESD-22, A115	VMM 200V
Latch-Up	JESD 78	10ms, 1 <sub>tr</sub> 100mA

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