MP111FD

FEATURES

- LOW COST
- HIGH VOLTAGE - 100 VOLTS
- HIGH OUTPUT CURRENT- 50 AMP PULSE OUTPUT, 15 AMP CONTINUOUS
- 170 WATT DISSIPATION CAPABILITY
- 130 V/uS SLEW RATE
- 500kHz POWER BANDWIDTH

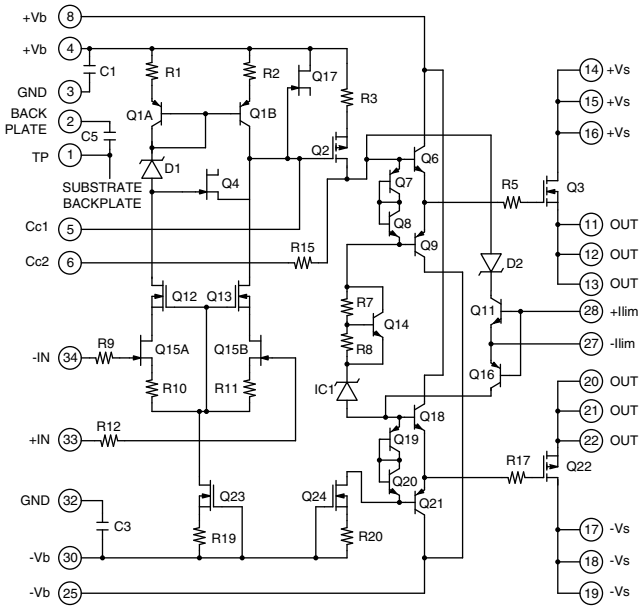
APPLICATIONS

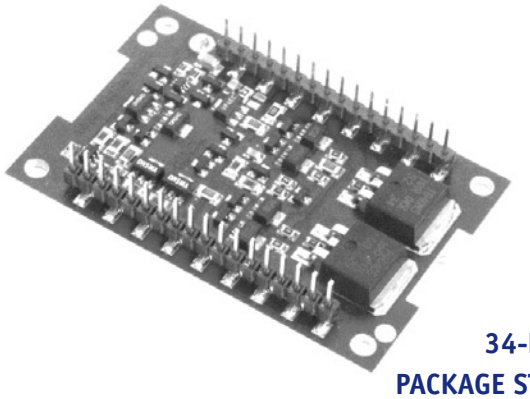
- INKJET PRINTER HEAD DRIVE
- PIEZO TRANSDUCER DRIVE
- INDUSTRIAL INSTRUMENTATION
- REFLECTOMETERS
- ULTRA-SOUND TRANSDUCER DRIVE

DESCRIPTION

The MP111FD operational amplifier is a surface mount constructed component that provides a cost-effective solution in many industrial applications. The MP111FD offers outstanding performance that rivals much more expensive hybrid components yet has a footprint of only 4 sq in. The MP111FD has many optional features such as four-wire current limit sensing and external compensation. The 500 kHz power bandwidth and 15 amp continuous and 50A pulse output of the MP111FD makes it a good choice for piezo transducer drive applications. The MP111FD is built on a thermally conductive but electrically insulating substrate that can be mounted to a heat sink.

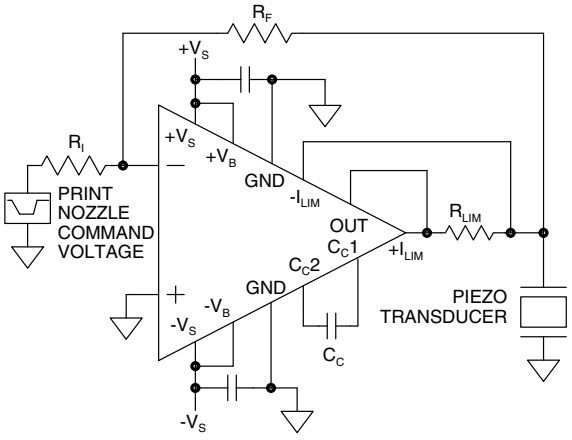
EQUIVALENT CIRCUIT DIAGRAM





34-PIN DIP
PACKAGE STYLE FD

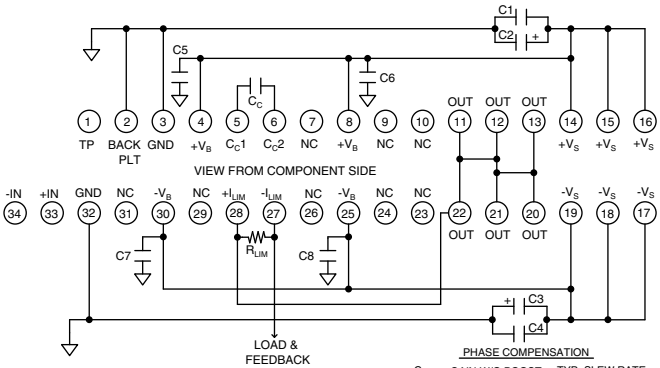
TYPICAL APPLICATION



INKJET NOZZLE DRIVE

The MP111FD's fast slew rate and wide power bandwith make it an ideal nozzle driver for industrial inkjet printers. The 50 amp pulse output capability can drive hundreds of inkjet nozzles simultaneously.

EXTERNAL CONNECTIONS



NOTES:
C_C IS NPO (COG) RATED FOR FULL SUPPLY VOLTAGE $+V_S$ TO $-V_S$.
BOTH PINS 3 AND 32 REQUIRED CONNECTED TO SIGNAL GROUND.
C2 AND C3 ELECTROLYTIC ≥ 10µF PER AMP OUTPUT CURRENT.
C1, C4, C5-8 HIGH QUALITY CERAMIC ≥ 0.1µF.
ALL OUTPUT PINS MUST BE TIED TOGETHER.
SEE PACKAGE OUTLINE FD IN THE OUTLINE DIMENSIONS DATASHEET.

PHASE COMPENSATION

C_C	GAIN W/O BOOST	TYP. SLEW RATE
100pF	≥1	55 V/µS
68pF	≥4	60 V/µS
33pF	≥10	130 V/µS

C_C	GAIN W BOOST	TYP. SLEW RATE
470pF	≥3	12 V/µS
220pF	≥6	27 V/µS
100pF	≥10	55 V/µS

ABSOLUTE MAXIMUM RATINGS

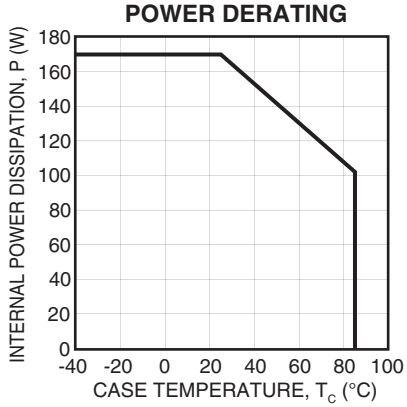
SUPPLY VOLTAGE, $+V_S$ to $-V_S$	100V
SUPPLY VOLTAGE, $+V_B$	$+V_S$ + 15V[6]
SUPPLY VOLTAGE, $-V_B$	$-V_S$ – 15V[6]
OUTPUT CURRENT, peak	50A, within SOA
POWER DISSIPATION, internal, DC	170W
INPUT VOLTAGE	$+V_B$ to $-V_B$
DIFFERENTIAL INPUT VOLTAGE	±25V
TEMPERATURE, pin solder, 10s	225°C.
TEMPERATURE, junction[2]	175°C.
TEMPERATURE RANGE, storage	-40 to 105°C.
OPERATING TEMPERATURE, case	-40 to 85°C.

SPECIFICATIONS

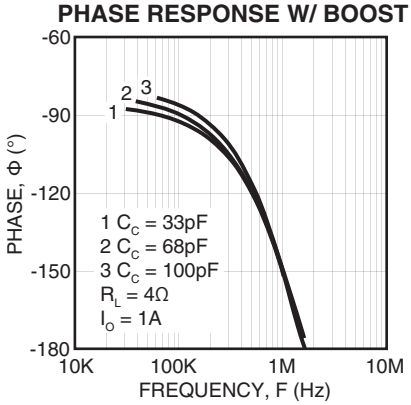
PARAMETER	TEST CONDITIONS[1]	MIN	TYP	MAX	UNITS
INPUT					
OFFSET VOLTAGE			1	5	mV
OFFSET VOLTAGE vs. temperature	Full temperature range		20	50	µV/°C
OFFSET VOLTAGE vs. supply				20	µV/V
BIAS CURRENT, initial[3]				100	pA
BIAS CURRENT vs. supply				0.1	pA/V
OFFSET CURRENT, initial				50	pA
INPUT RESISTANCE, DC			10^{11}		Ω
INPUT CAPACITANCE			4		pF
COMMON MODE VOLTAGE RANGE				$+V_B$ - 15	V
COMMON MODE VOLTAGE RANGE				$-V_B$ + 15	V
COMMON MODE REJECTION, DC		92			dB
NOISE	1MHz bandwidth, 1kΩ R_S		10		µV RMS
GAIN					
OPEN LOOP @ 15Hz	R_L = 10KΩ, C_C = 33pF	96			dB
GAIN BANDWIDTH PRODUCT @ 1MHz	C_C = 33pF		6		MHz
PHASE MARGIN	Full temperature range	45			degrees
OUTPUT					
VOLTAGE SWING	I_O = 15A	$+V_S$ - 10	$+V_S$ - 8.4		V
VOLTAGE SWING	I_O = -15A	$-V_S$ + 10	$-V_S$ + 5.8		V
VOLTAGE SWING	I_O = 15A, $+V_B$ = $+V_S$ +10V	$+V_S$ - 0.8			V
VOLTAGE SWING	I_O = -15A, $-V_B$ = $-V_S$ -10V	$-V_S$ + 1.0			V
CURRENT, continuous, DC		15			A
SLEW RATE, A_V = -20	C_C = 33pF	100	130		V/µS
SETTLING TIME, to 0.1%	2V Step		1		µS
RESISTANCE	No load, DC		3		Ω
POWER BANDWIDTH 80V_{P-P}	C_C = 33pF, $+V_S$ = 50V, $-V_S$ = -50V		500		kHz
POWER SUPPLY					
VOLTAGE		±15	±45	±50	V
CURRENT, quiescent			142	157	mA
THERMAL					
RESISTANCE, AC, junction to case[5]	Full temperature range, f ≥ 60Hz			.65	°C/W
RESISTANCE, DC, junction to case	Full temperature range, f < 60Hz			.88	°C/W
RESISTANCE, junction to air	Full temperature range			13	°C/W
TEMPERATURE RANGE, case		-40		85	°C

NOTES:
1. Unless otherwise noted: T_C=25°C, compensation C_C=100pF, DC input specifications are value given, power supply voltage is typical rating.
2. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTBF.
3. Doubles for every 10°C of case temperature increase.
4. $+V_S$ and $-V_S$ denote the positive and negative supply voltages to the output stage. $+V_B$ and $-V_B$ denote the positive and negative supply voltages to the input stages.
5. Rating applies if the output current alternates between both output transistors at a rate faster than 60Hz.
6. Power supply voltages $+V_B$ and $-V_B$ must not be less than $+V_S$ and $-V_S$ respectively.

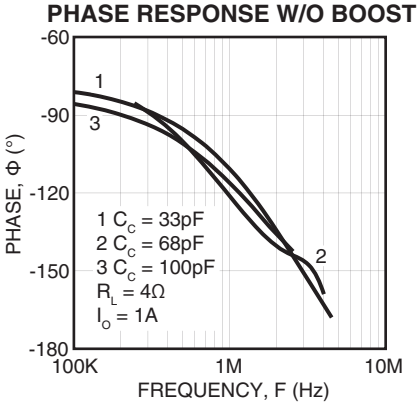
POWER DERATING



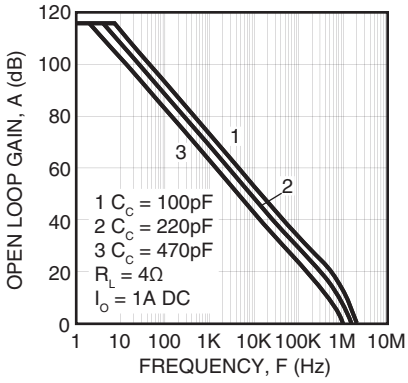
PHASE RESPONSE W/ BOOST



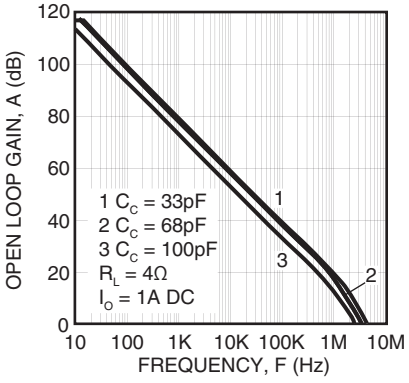
PHASE RESPONSE W/O BOOST



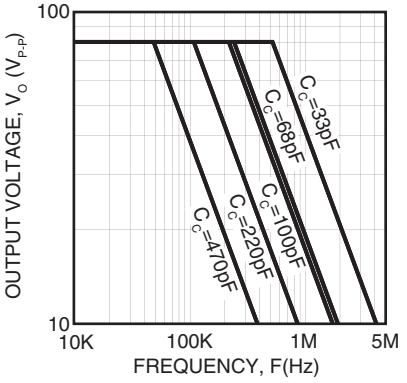
SMALL SIGNAL RESPONSE W/ BOOST



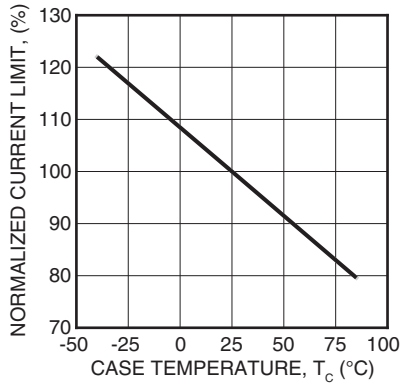
SMALL SIGNAL RESPONSE W/O BOOST



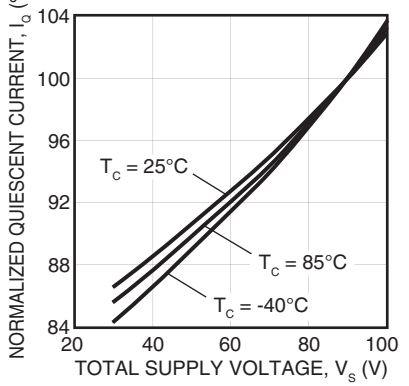
POWER RESPONSE



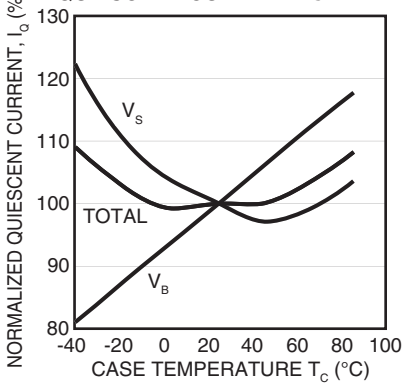
CURRENT LIMIT



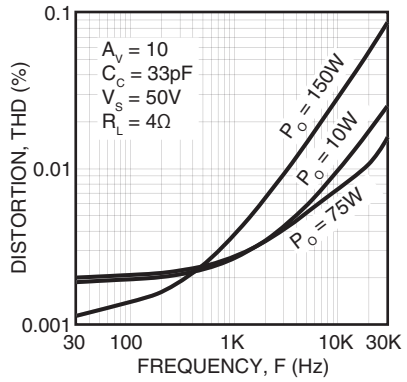
QUIESCENT CURRENT vs. SUPPLY



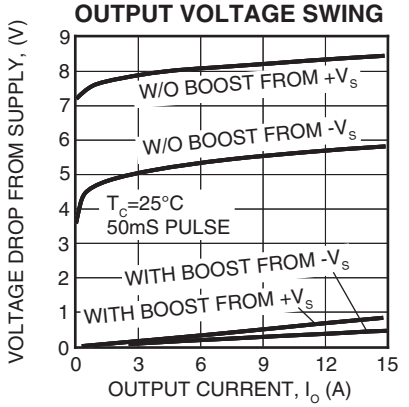
QUIESCENT CURRENT vs. TEMP.



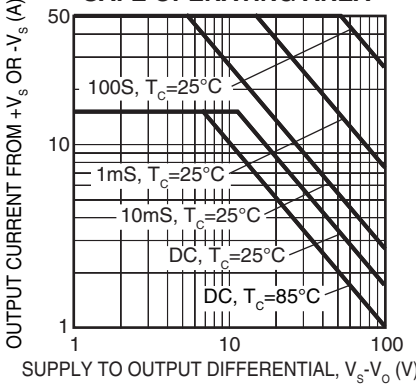
HARMONIC DISTORTION



OUTPUT VOLTAGE SWING



SAFE OPERATING AREA



GENERAL

Please read Application Note 1 "General Operating Considerations" which covers stability, power supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexmicrotech.com for design tools that help automate tasks such as calculations for stability, internal power dissipation, current limit, heat sink selection, Apex's complete Application Notes library, Technical Seminar Workbook and Evaluation Kits.

GROUND PINS

The MP111FD has two ground pins (pins 3, 32). These pins provide a return for the internal capacitive bypassing of the small signal portions of the MP111FD. The two ground pins are not connected together on the substrate. Both of these pins are required to be connected to the system signal ground.

SAFE OPERATING AREA

The MOSFET output stage of the MP111FD is not limited by second breakdown considerations as in bipolar output stages. Only thermal considerations and current handling capabilities limit the SOA (see Safe Operating Area graph on previous page). The output stage is protected against transient flyback by the parasitic body diodes of the output stage MOSFET structure. However, for protection against sustained high energy flyback external fast-recovery diodes must be used.

COMPENSATION

The external compensation capacitor C_C is connected between pins 5 and 6. Unity gain stability can be achieved with any capacitor value larger than 100pF for a minimum phase margin of 45 degrees. At higher gains more phase shift can usually be tolerated in most designs and the compensation capacitor value can be reduced resulting in higher bandwidth and slew rate. Use the typical operating curves as a guide to select C_C for the application. An NPO (COG) type capacitor is required rated for the full supply voltage (100V).

OVERVOLTAGE PROTECTION

Although the MP111FD can withstand differential input voltages up to ±25V, additional external protection is recommended. In most applications 1N4148 signal diodes connected anti-parallel across the input pins is sufficient. In more demanding applications where bias current is important diode connected JFETs such as 2N4416 will be required. See Q1 and Q2 in Figure 1. In either case the differential input voltage will be clamped to ±0.7V. This is usually sufficient overdrive to produce the maximum power bandwidth. Some applications will also need over voltage protection devices connected to the power supply rails. Unidirectional zener diode transient suppressors are recommended. The zeners clamp transients to voltages within the power supply rating and also clamp power supply reversals to ground. Whether the zeners are used or not the system power supply should be evaluated for transient performance including power-on overshoot and power-off polarity reversals as well as line regulation. See Z1 and Z2 in Figure 1.

POWER SUPPLY BYPASSING

Bypass capacitors to power supply terminals $+V_S$ and $-V_S$ must be connected physically close to the pins to prevent local parasitic oscillation in the output stage of the MP111FD. Use electrolytic capacitors at least 10µF per output amp required. Bypass the electrolytic capacitors with high quality ceramic capacitors (X7R) 0.1µF or greater. In most applications power supply terminals +Vb and -Vb will be connected to $+V_S$ and $-V_S$ respectively. Supply voltages +Vb and -Vb are bypassed internally but both ground pins 3 and 32 must be connected to the system signal ground to be effective. In all cases power to the buffer amplifier stage of the MP111FD at pins 8 and 25 must be connected to +Vb and

-Vb at pins 4 and 30 respectively. Provide local bypass capacitors at pins 8 and 25. See the external connections diagram on page 1.

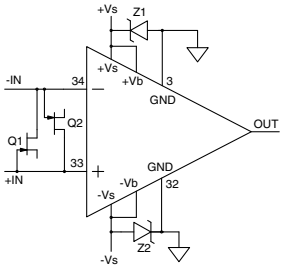


FIGURE 1
OVERVOLTAGE PROTECTION

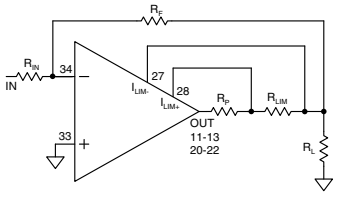


FIGURE 2
4 WIRE CURRENT LIMIT

CURRENT LIMIT

The two current limit sense lines are to be connected directly across the current limit sense resistor. For the current limit to work correctly pin 28 must be connected to the amplifier output side and pin 27 connected to the load side of the current limit resistor R_{LIM} as shown in Figure 2. This connection will bypass any parasitic resistances R_P, formed by socket and solder joints as well as internal amplifier losses. The current limiting resistor may not be placed anywhere in the output circuit except where shown in Figure 2. The value of the current limit resistor can be calculated as follows: $R_{LIM} = .65/I_{LIMIT}$

BOOST OPERATION

With the boost feature the small signal stages of the amplifier are operated at a higher supply voltages than the amplifier's high current output stage. +Vb (pins 4,8) and -Vb (pins 25,30) are connected to the small signal stages and $+V_S$ (pins 14-16) and $-V_S$ (pins 17-19) are connected to the high current output stage. An additional 10V on the +Vb and -Vb pins is sufficient to allow the small signal stages to drive the output stage into the triode region and improve the output voltage swing for extra efficient operation when required. When the boost feature is not needed $+V_S$ and $-V_S$ are connected to the +Vb and -Vb pins respectively. The +Vb and -Vb pins must not be operated at supply voltages less than $+V_S$ and $-V_S$ respectively.

BACKPLATE GROUNDING

The substrate of the MP111FD is an insulated metal substrate. It is required that it be connected to signal ground. Connect pin 2 (back plate) to signal ground. The back plate will then be AC grounded to signal ground through a 1µF capacitor.